MJF44H11 (NPN), MJF45H11 (PNP)

Preferred Devices

Complementary Power Transistors

For Isolated Package Applications

Complementary power transistors are for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

Features

- Low Collector−Emitter Saturation Voltage − $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs
- Pb−Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous − Peak	I_C	10 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 36 0.288	 W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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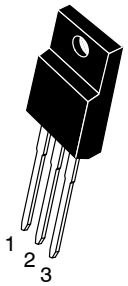
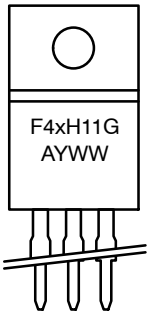
SILICON POWER TRANSISTORS
10 AMPERES
80 VOLTS, 36 WATTS



ISOLATED TO−220
CASE 221D
STYLE 2

MARKING DIAGRAM



F4xH11 = Specific Device Code
x = 4 or 5
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJF44H11	TO−220 FULLPACK	50 Units/Rail
MJF44H11G	TO−220 FULLPACK (Pb−Free)	50 Units/Rail
MJF45H11	TO−220 FULLPACK	50 Units/Rail
MJF45H11G	TO−220 FULLPACK (Pb−Free)	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 30 mA, I_B = 0)		$V_{CEO(sus)}$	80	–	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	–	–	1.0	μA
Emitter Cutoff Current (V_{EB} = 5 Vdc)		I_{EBO}	–	–	10	μA
ON CHARACTERISTICS						
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	–	–	1.0	Vdc
Base−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
DC Current Gain (V_{CE} = 1 Vdc, I_C = 2 Adc)		h_{FE}	60	–	–	–
DC Current Gain (V_{CE} = 1 Vdc, I_C = 4 Adc)			40	–	–	
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	MJF44H11 MJF45H11	C_{cb}	– –	130 230	– –	pF
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	MJF44H11 MJF45H11	f_T	– –	50 40	– –	MHz
SWITCHING TIMES						
Delay and Rise Times (I_C = 5 Adc, I_{B1} = 0.5 Adc)	MJF44H11 MJF45H11	$t_d + t_r$	– –	300 135	– –	ns
Storage Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJF44H11 MJF45H11	t_s	– –	500 500	– –	ns
Fall Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJF44H11 MJF45H11	t_f	– –	140 100	– –	ns

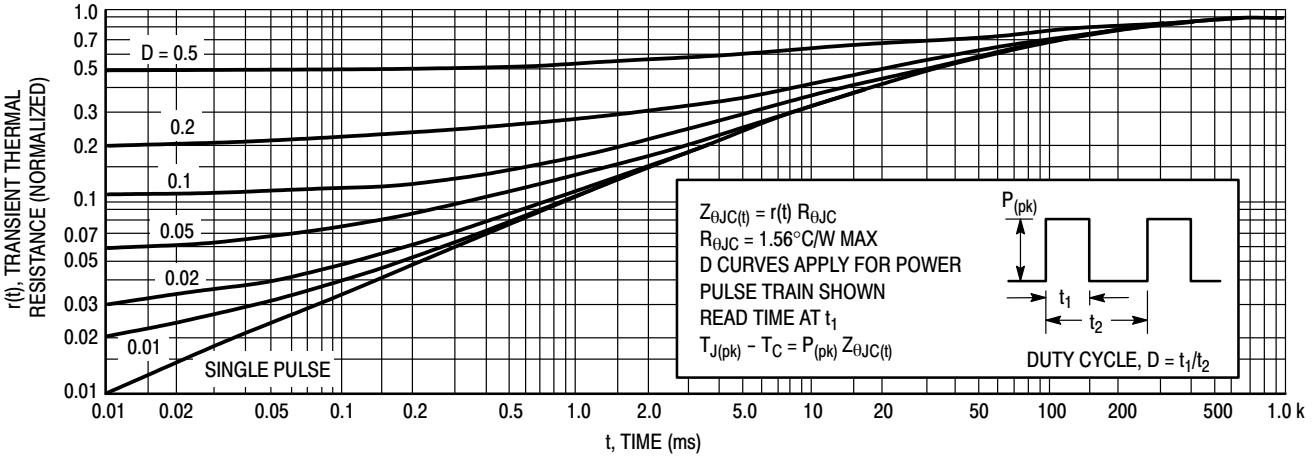


Figure 1. Thermal Response

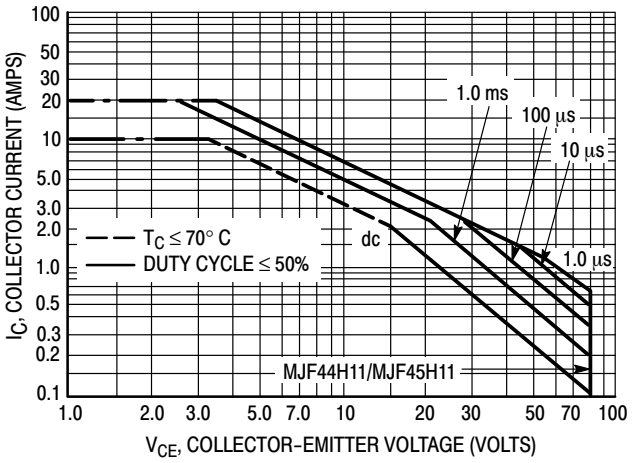


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

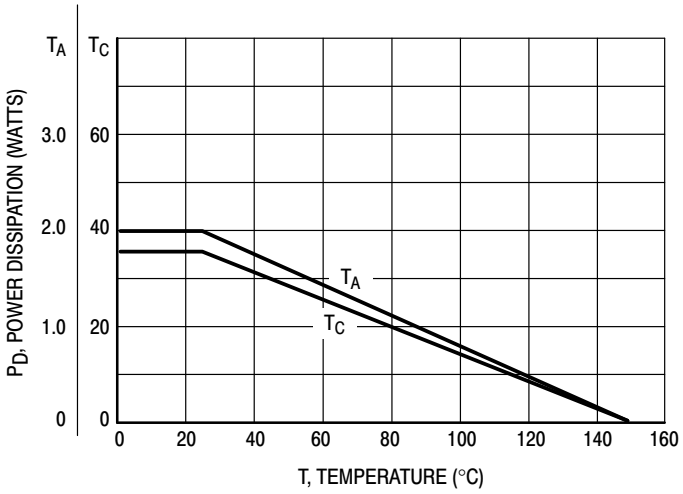


Figure 3. Power Derating

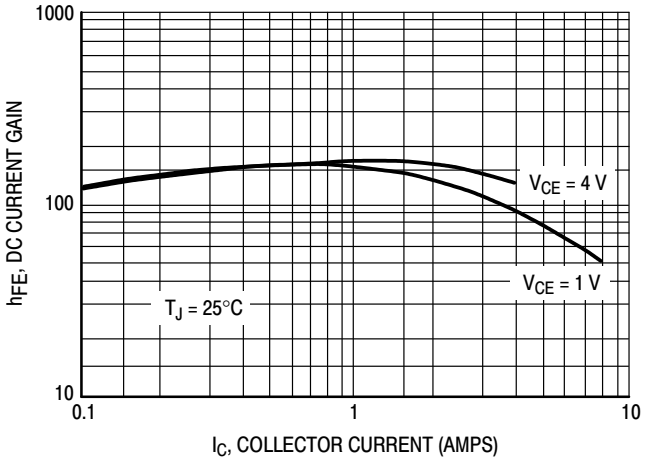


Figure 4. MJF44H11 DC Current Gain

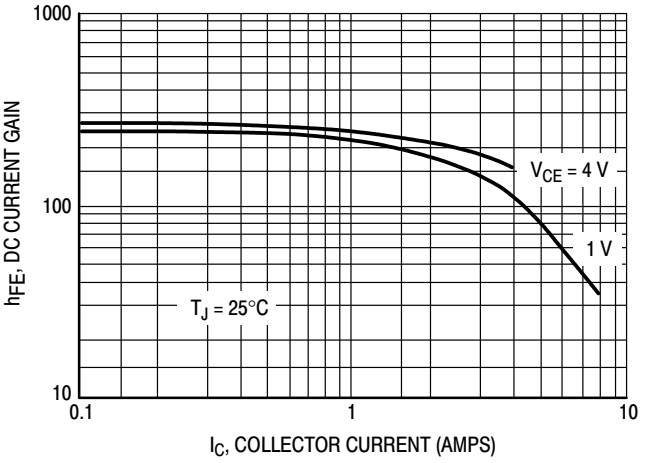


Figure 5. MJF45H11 DC Current Gain

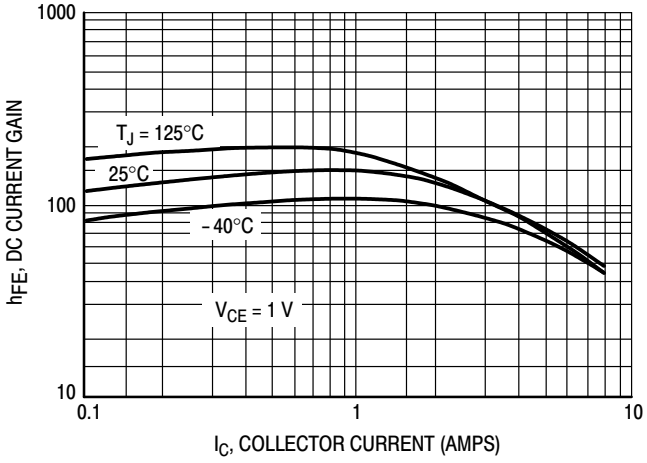


Figure 6. MJF44H11 Current Gain versus Temperature

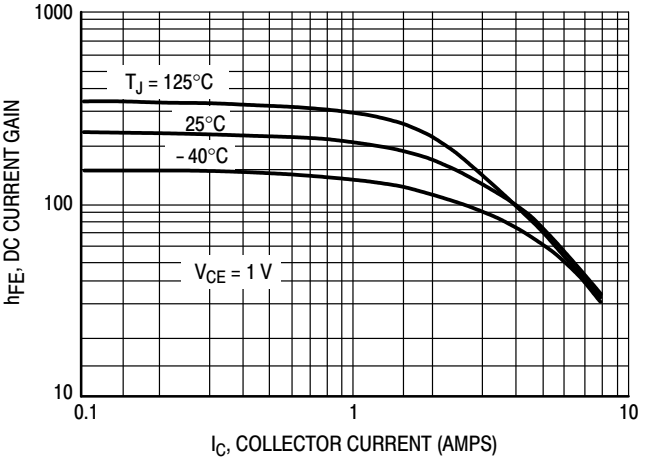


Figure 7. MJF45H11 Current Gain versus Temperature

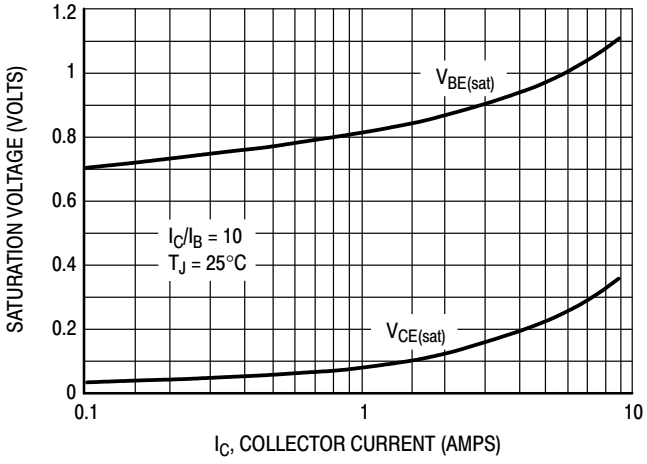


Figure 8. MJF44H11 On−Voltages

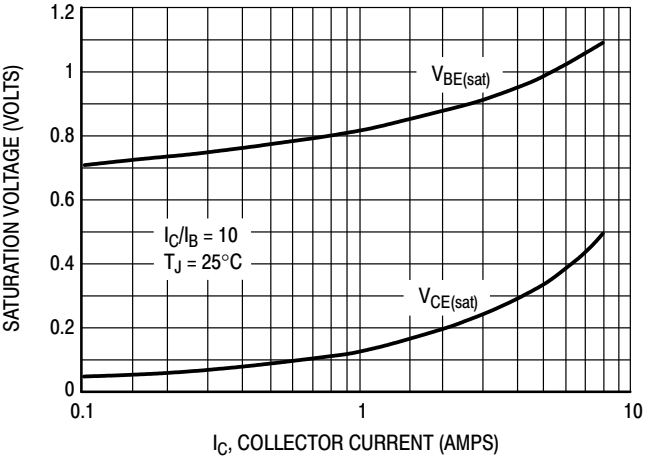


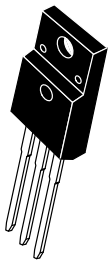
Figure 9. MJF45H11 On−Voltages

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

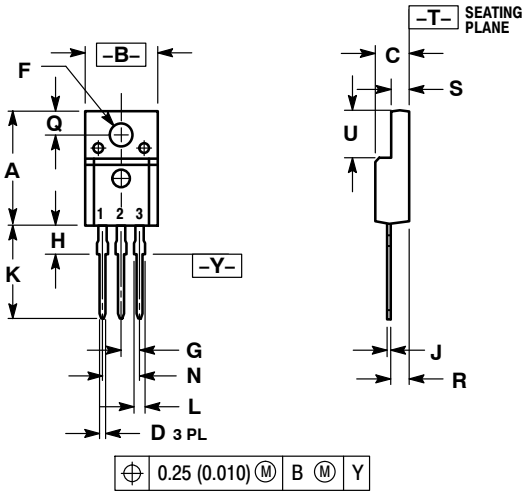
ON Semiconductor®

TO−220 FULLPAK
CASE 221D−03
ISSUE K

DATE 27 FEB 2009



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D−01 THRU 221D−02 OBSOLETE, NEW STANDARD 221D−03.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

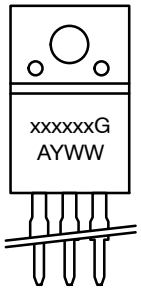
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE

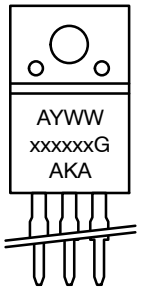
STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE

MARKING DIAGRAMS



Bipolar



Rectifier

xxxxxx	= Specific Device Code
G	= Pb−Free Package
A	= Assembly Location
Y	= Year
WW	= Work Week

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Y	= Year
WW	= Work Week
xxxxxx	= Device Code
G	= Pb−Free Package
AKA	= Polarity Designator

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