



Ultralow Offset Voltage Operational Amplifiers

OP07

FEATURES

Low V_{OS} : 75 μV Max
Low V_{OS} Drift: 1.3 $\mu\text{V}/^\circ\text{C}$ Max
Ultra-Stable vs. Time: 1.5 $\mu\text{V}/\text{Month}$ Max
Low Noise: 0.6 μV p-p Max
Wide Input Voltage Range: ± 14 V
Wide Supply Voltage Range: 3 V to 18 V
Fits 725,108A/308A, 741, AD510 Sockets
125°C Temperature-Tested Dice

APPLICATIONS

Wireless Base Station Control Circuits
Optical Network Control Circuits
Instrumentation
Sensors and Controls
Thermocouples
RTDs
Strain Bridges
Shunt Current Measurements
Precision Filters

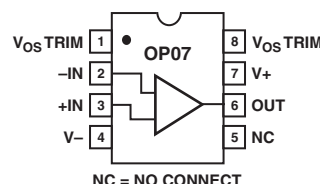
GENERAL DESCRIPTION

The OP07 has very low input offset voltage (75 μV max for OP07E) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP07 also features low input bias current (± 4 nA for OP07E) and high open-loop gain (200 V/mV for OP07E). The low offsets and high open-loop gain make the OP07 particularly useful for high-gain instrumentation applications.

The wide input voltage range of ± 13 V minimum combined with high CMRR of 106 dB (OP07E) and high input impedance provides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at

PIN CONNECTIONS

Epoxy Mini-Dip (P-Suffix)
8-Pin SO (S-Suffix)



high closed-loop gains. Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP07, even at high gain, combined with the freedom from external nulling have made the OP07 an industry standard for instrumentation applications.

The OP07 is available in two standard performance grades. The OP07E is specified for operation over the 0°C to 70°C range, and OP07C over the -40°C to $+85^\circ\text{C}$ temperature range.

The OP07 is available in epoxy 8-lead Mini-DIP and 8-lead SOIC. It is a direct replacement for 725,108A, and OP05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer. For improved specifications, see the OP177 or OP1177. For ceramic DIP and TO-99 packages and standard micro circuit (SMD) versions, see the OP77.

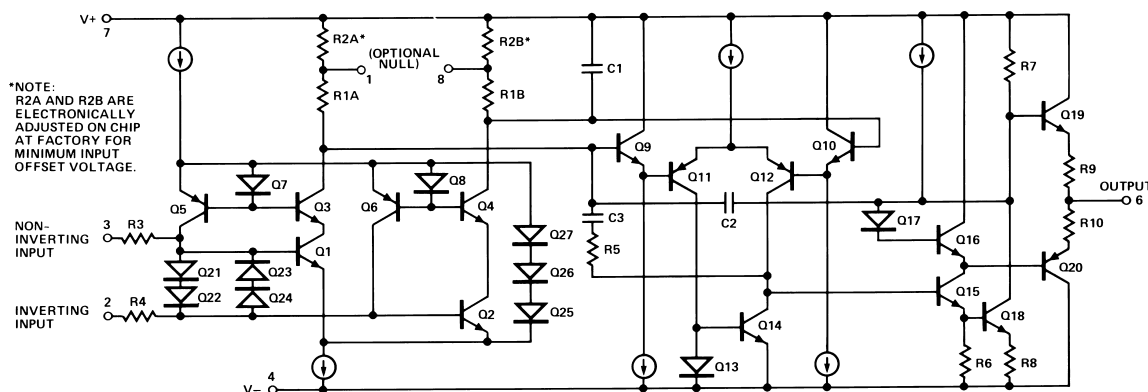


Figure 1. Simplified Schematic

REV. A

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OP07—SPECIFICATIONS

OP07E ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage ¹	V _{OS}			30	75	μV
Long-Term V _{OS} Stability ²	V _{OS} /Time			0.3	1.5	μV/Mo
Input Offset Current	I _{OS}			0.5	3.8	nA
Input Bias Current	I _B			±1.2	±4.0	nA
Input Noise Voltage	e _n p-p	0.1 Hz to 10 Hz ³		0.35	0.6	μV p-p
Input Noise Voltage Density	e _n	f _O = 10 Hz		10.3	18.0	nV/√Hz
		f _O = 100 Hz ³		10.0	13.0	nV/√Hz
		f _O = 1 kHz		9.6	11.0	nV/√Hz
				14	30	pA p-p
Input Noise Current	I _n p-p	f _O = 10 Hz		0.32	0.80	pA/√Hz
Input Noise Current Density	I _n	f _O = 100 Hz ³		0.14	0.23	pA/√Hz
		f _O = 1 kHz		0.12	0.17	pA/√Hz
Input Resistance—Differential Mode ⁴	R _{IN}		15	50		mΩ
Input Resistance—Common-Mode	R _{INCM}			160		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±13 V	106	123		dB
Power Supply Rejection Ratio	PSRR	V _S = ±3 V to ±18 V		5	20	μV/V
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2 kΩ, V _O = ±10 V	200	500		V/mV
		R _L ≥ 500 Ω, V _O = ±0.5 V,				
		V _S = ±3 V ⁴	150	400		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V _O	R _L ≥ 10 kΩ	±12.5	±13.0		V
		R _L ≥ 2 kΩ	±12.0	±12.8		V
		R _L ≥ 1 kΩ	±10.5	±12.0		V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R _L ≥ 2 kΩ ³	0.1	0.3		V/μs
Closed-Loop Bandwidth	BW	A _{VOL} = 1 ⁵	0.4	0.6		MHz
Closed-Loop Output Resistance	R _O	V _O = 0, I _O = 0		60		Ω
Power Consumption	P _d	V _S = ±15 V, No Load		75	120	mW
		V _S = ±13 V, No Load		4	6	mW
Offset Adjustment Range		R _p = 20 kΩ		±4		mV

NOTES

¹Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

²Long-term input offset voltage stability refers to the averaged trend time of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 μV refer to the typical performance curves. Parameter is sample tested.

³Sample tested.

⁴Guaranteed by design.

⁵Guaranteed but not tested.

Specifications subject to change without notice.

OP07C ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage ¹	V _{OS}			60	150	μV
Long-Term V _{OS} Stability ²	V _{OS} /Time			0.4	2.0	μV/Mo
Input Offset Current	I _{OS}			0.8	6.0	nA
Input Bias Current	I _B			±1.8	±7.0	nA
Input Noise Voltage	e _n p-p	0.1 Hz to 10 Hz ³		0.38	0.65	μV p-p
Input Noise Voltage Density	e _n	f _O = 10 Hz		10.5	20.0	nV√Hz
		f _O = 100 Hz ³		10.2	13.5	nV√Hz
		f _O = 1 kHz		9.8	11.5	nV√Hz
Input Noise Current	I _n p-p			15	35	pA p-p
Input Noise Current Density	I _n	f _O = 10 Hz		0.35	0.90	pA√Hz
		f _O = 100 Hz ³		0.15	0.27	pA√Hz
		f _O = 1 kHz		0.13	0.18	pA√Hz
Input Resistance- Differential Mode ⁴	R _{IN}		8	33		mΩ
Input Resistance- Common-Mode	R _{INCM}			120		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±13 V	100	120		dB
Power Supply Rejection Ratio	PSRR	V _S = ±3 V to ±18 V		7	32	μV/V
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2 kΩ, V _O = ±10 V	120	400		V/mV
		R _L ≥ 500 Ω, V _O = ±0.5 V, V _S = ±3 V ⁴	100	400		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V _O	R _L ≥ 10 kΩ	±12.0	±13.0		V
		R _L ≥ 2 kΩ	±11.5	±12.8		V
		R _L ≥ 1 kΩ		±12.0		V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R _L ≥ 2 kΩ ³	0.1	0.3		V/μs
Closed-Loop Bandwidth	BW	A _{VOL} = 1 ⁵	0.4	0.6		MHz
Closed-Loop Output Resistance	R _O	V _O = 0, I _O = 0		60		Ω
Power Consumption	P _d	V _S = ±15 V, No Load		80	150	mW
		V _S = ±13 V, No Load		4	8	mW
Offset Adjustment Range		R _p = 20 kΩ		±4		mV

NOTES

¹Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

²Long-term input offset voltage stability refers to the averaged trend time of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 μV refer to the typical performance curves. Parameter is sample tested.

³Sample tested.

⁴Guaranteed by design.

⁵Guaranteed but not tested.

Specifications subject to change without notice.

OP07—SPECIFICATIONS

OP07E ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\text{ V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage ¹	V_{OS}	$R_P = 20\text{ k}\Omega$		45	130	μV
Voltage Drift without External Trim ²	TCV_{OS}			0.3	1.3	$\mu\text{V}/^\circ\text{C}$
Voltage Drift with External Trim ³	TCV_{OSN}			0.3	1.3	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}			0.9	5.3	nA
Input Offset Current Drift	TCI_{OS}			8	35	$\text{pA}/^\circ\text{C}$
Input Bias Current	I_B			± 1.5	± 5.5	nA
Input Bias Current Drift	TCI_B			13	35	$\text{pA}/^\circ\text{C}$
Input Voltage Range	IVR		± 13	± 13.5		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{ V}$	103	123		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$		7	32	$\mu\text{V/V}$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	180	450		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	$R_L \geq 10\text{ k}\Omega$	± 12	± 12.6		V

NOTES

¹Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

²Guaranteed by design.

³Sample tested.

Specifications subject to change without notice.

($V_S = \pm 15\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.)

OP07C ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage ¹	V_{OS}	$R_P = 20\text{ k}\Omega$		85	250	μV
Voltage Drift without External Trim ²	TCV_{OS}			0.5	1.8	$\mu\text{V}/^\circ\text{C}$
Voltage Drift with External Trim ³	TCV_{OSN}			0.4	1.8	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}			1.6	8.0	nA
Input Offset Current Drift	TCI_{OS}			12	50	$\text{pA}/^\circ\text{C}$
Input Bias Current	I_B			± 2.2	± 9.0	nA
Input Bias Current Drift	TCI_B			18	50	$\text{pA}/^\circ\text{C}$
Input Voltage Range	IVR		± 13	± 13.5		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{ V}$	97	120		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$		10	51	$\mu\text{V/V}$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	100	400		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	$R_L \geq 10\text{ k}\Omega$	± 11	± 12.6		V

NOTES

¹Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

²Guaranteed by design.

³Sample tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_S)	± 22 V
Input Voltage*	± 22 V
Differential Input Voltage	± 30 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
S, P Packages	-65°C to $+125^{\circ}\text{C}$
Operating Temperature Range	
OP07E	0°C to 70°C
OP07C	-40°C to $+85^{\circ}\text{C}$
Junction Temperature Range	150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

*For supply voltages less than ± 22 V, the absolute maximum input voltage is equal to the supply voltage.

Package Type	θ_{JA}^*	θ_{JC}	Units
8-Lead Plastic DIP (P)	103	43	$^{\circ}\text{C}/\text{W}$
8-Lead SOIC (S)	158	43	$^{\circ}\text{C}/\text{W}$

* θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package, θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE

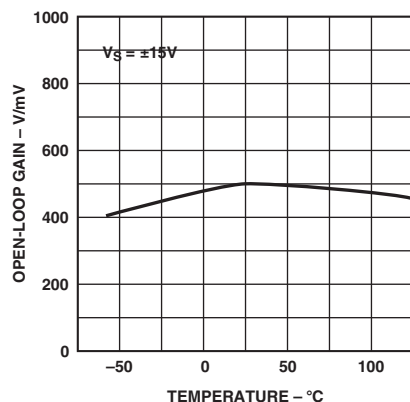
Model	Temperature Range	Package Description	Package Option	Branding Information
OP07EP	0°C to 70°C	8-Lead Epoxy DIP	P-8	
OP07CP	-40°C to 85°C	8-Lead Epoxy DIP	P-8	
OP07CS	-40°C to 85°C	8-Lead SOIC	S-8	

CAUTION

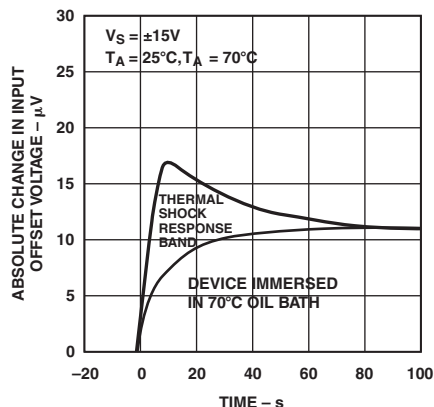
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP07 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



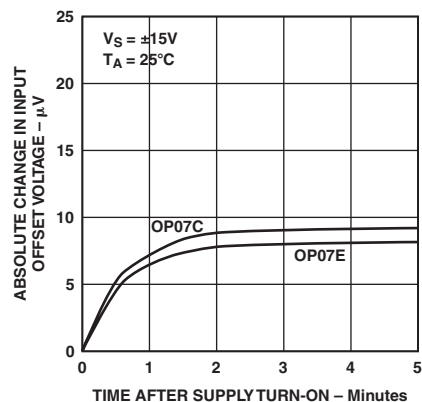
OP07 – Typical Performance Characteristics



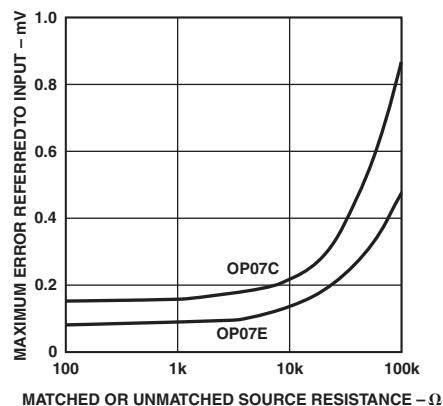
TPC 1. Open-Loop Gain vs. Temperature



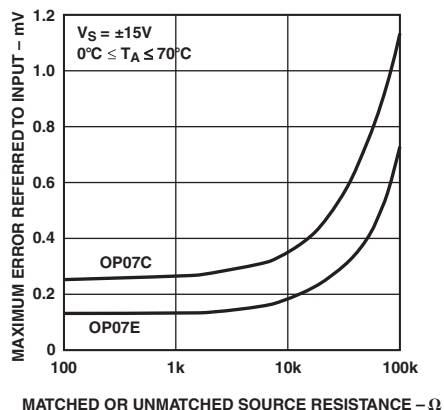
TPC 2. Offset Voltage Change Due to Thermal Shock



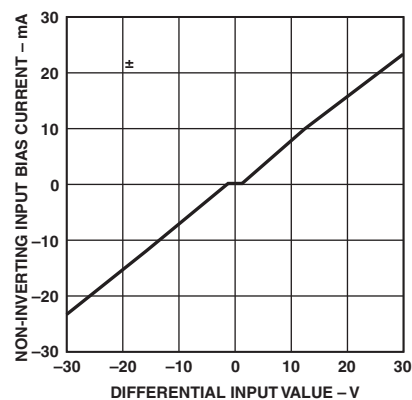
TPC 3. Warm-Up Drift



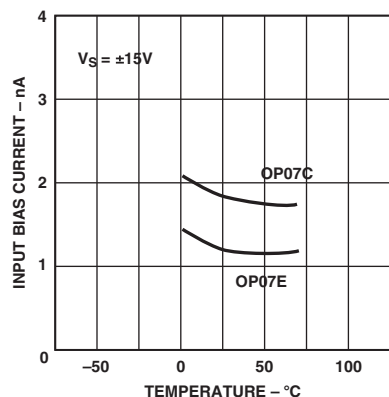
TPC 4. Maximum Error vs. Source Resistance



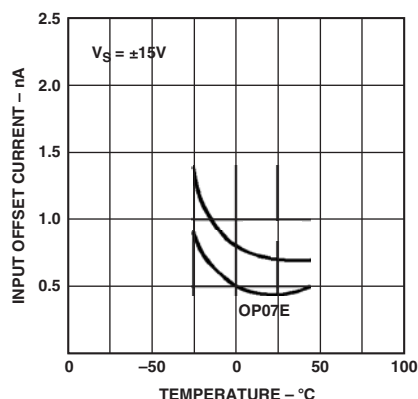
TPC 5. Maximum Error vs. Source Resistance



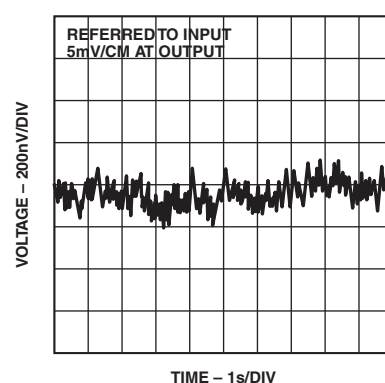
TPC 6. Input Bias Current vs. Differential Input Voltage



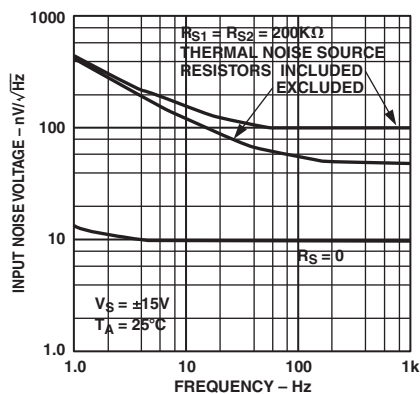
TPC 7. Input Bias Current vs. Temperature



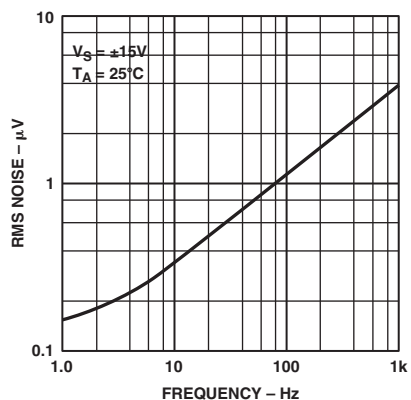
TPC 8. Input Offset Current vs. Temperature



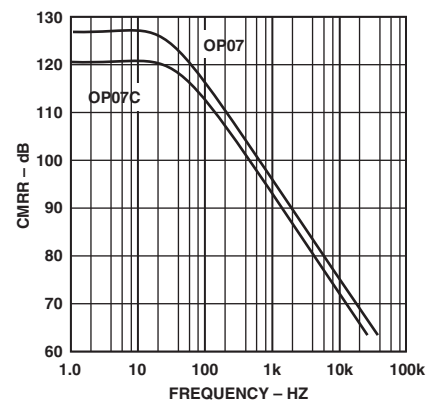
TPC 9. Low Frequency Noise



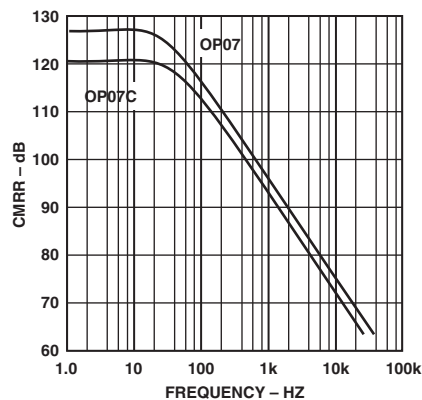
TPC 10. Total Input Noise Voltage vs. Frequency



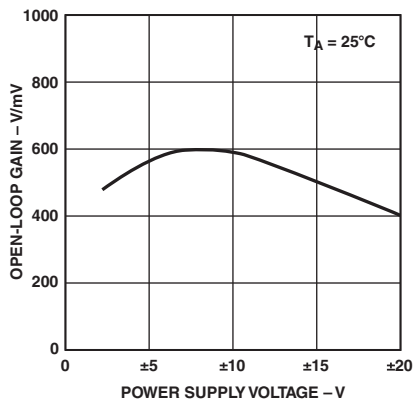
TPC 11. Input Wideband Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)



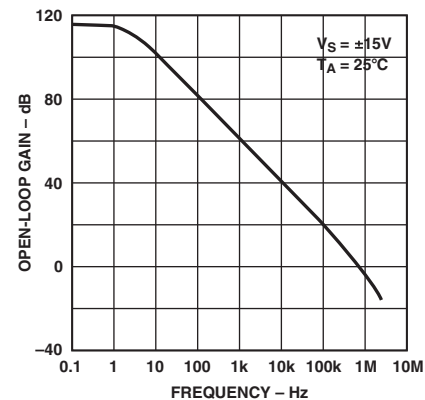
TPC 12. CMRR vs. Frequency



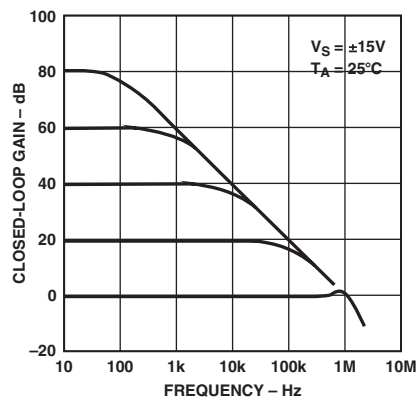
TPC 13. PSRR vs. Frequency



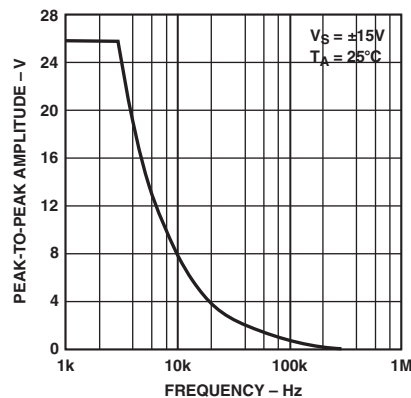
TPC 14. Open-Loop Gain vs. Power Supply Voltage



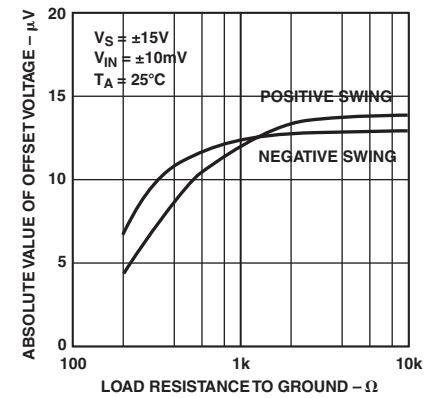
TPC 15. Open-Loop Frequency Response



TPC 16. Closed-Loop Response for Various Gain Configurations

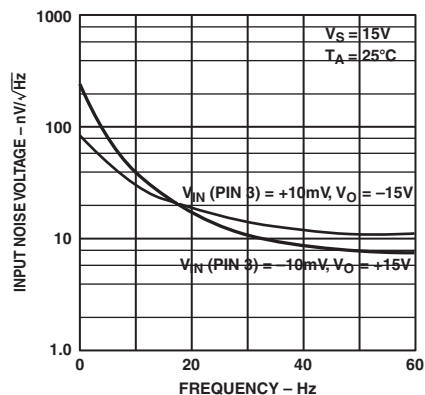


TPC 17. Maximum Output Swing vs. Frequency

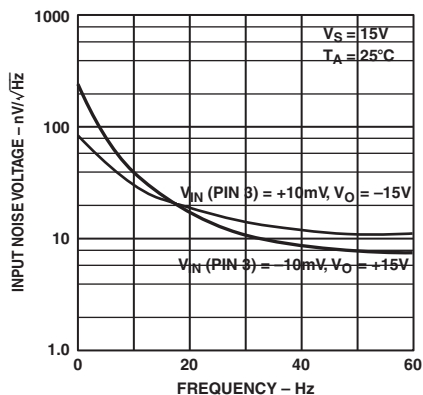


TPC 18. Maximum Output Voltage vs. Load Resistance

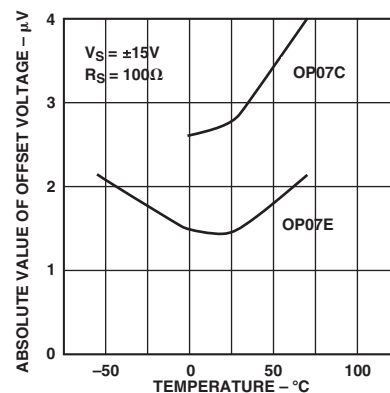
OP07



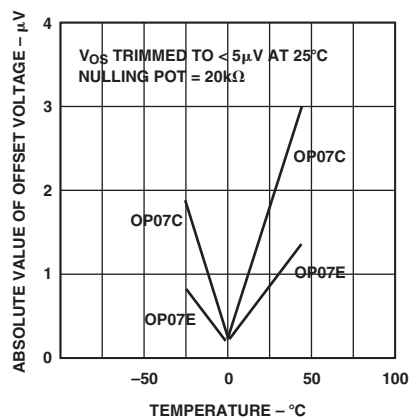
TPC 19. Power Consumption vs. Power Supply



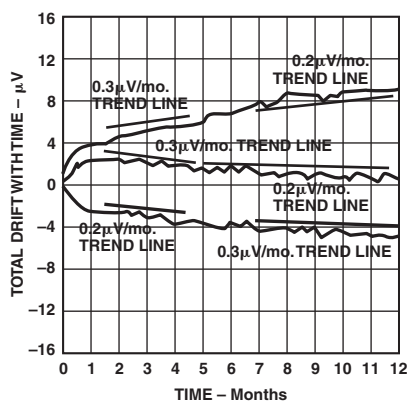
TPC 20. Output Short-Circuit Current vs. Time



TPC 21. Untrimmed Offset Voltage vs. Temperature



TPC 22. Trimmed Offset Voltage vs. Temperature



TPC 23. Offset Voltage Stability vs. Time

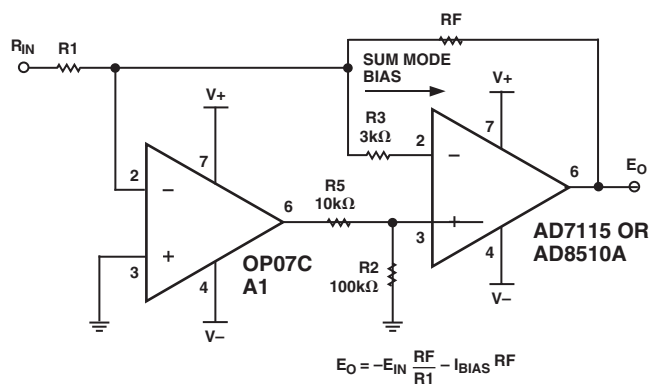


Figure 2. Typical Offset Voltage Test Circuit

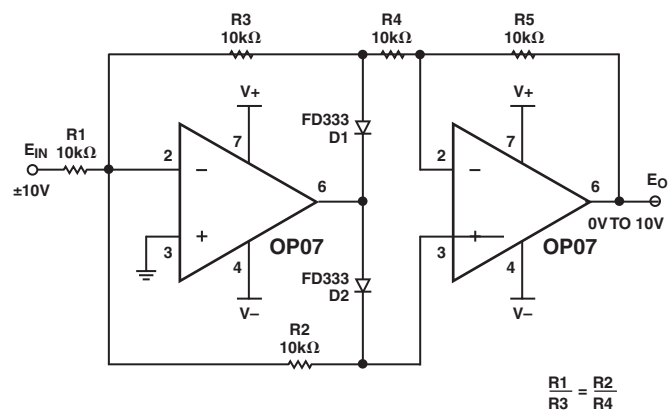


Figure 5. Burn-In circuit

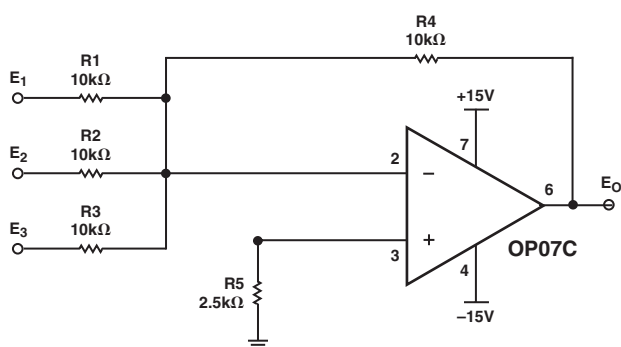
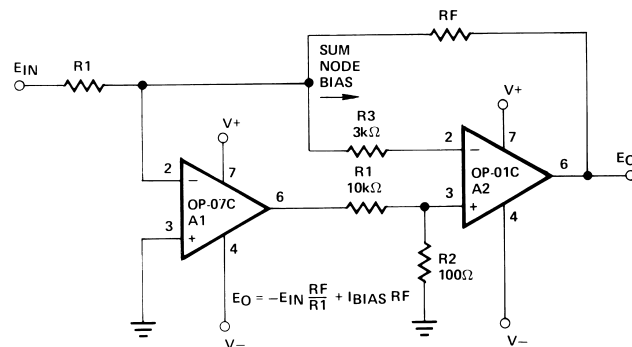


Figure 3. Typical Low-Frequency Noise Circuit



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 6. High-Speed, Low VOS Composite Amplifier

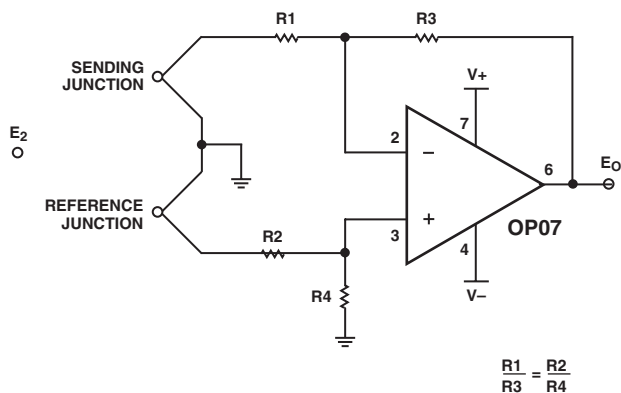
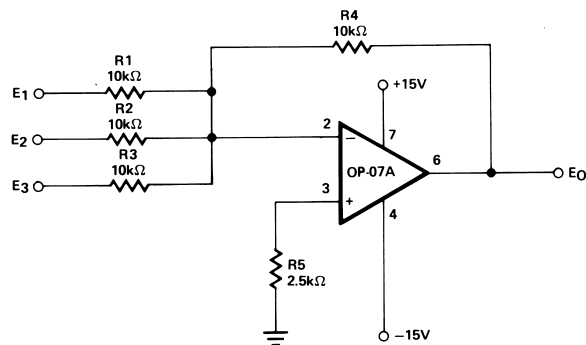


Figure 4. Optional Offset Nulling Circuit

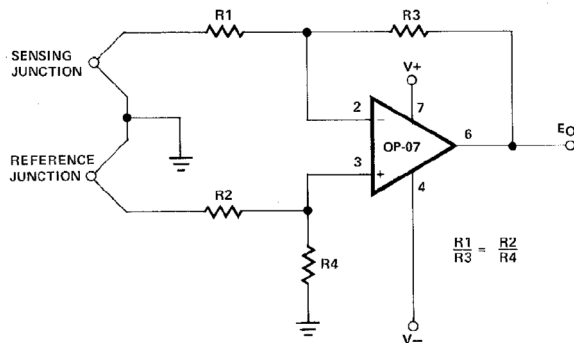


PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 7. Adjustment-Free Precision Summing Amplifier

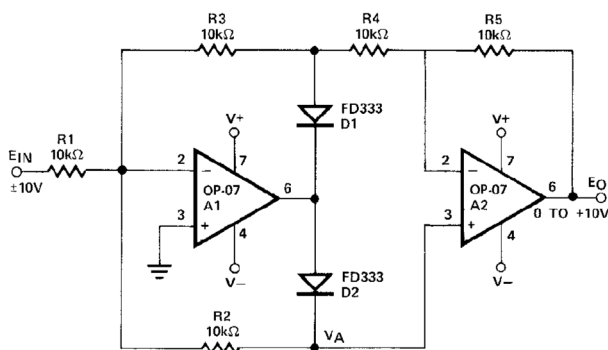
OP07

TYPICAL APPLICATIONS



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 8. High-Stability Thermocouple Amplifier



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 9. Precision Absolute-Value Circuit

APPLICATIONS INFORMATION

OP07 series units may be substituted directly into 725, 108A/308A* and OP05 sockets with or without removal of external compensation or nulling components. Additionally, the OP07 may be used in unnullled 741 type sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP07 operation. OP07 offset voltage may be nulled to zero through use of a potentiometer (see offset nulling circuit diagram).

PRECISION ABSOLUTE-VALUE CIRCUIT

The OP07 provides stable operation with load capacitance of up to 500 pF and ± 10 V swings; larger capacitances should be decoupled with a 50 Q decoupling resistor.

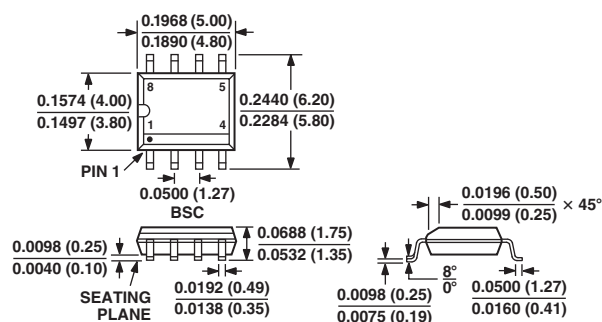
Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

*TO-99 Package only

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SO DIP (S-Suffix)



Revision History

Location	Page
Data Sheet changed from REV. 0 to REV. A.	
Edits to FEATURES	1
Edits to ORDERING GUIDE	1
Edits to PIN CONNECTION drawings	1
Edits to ABSOLUTE MAXIMUM RATINGS	2
Deleted ELECTRICAL CHARACTERISTICS	2-3
Deleted OP07D Column from ELECTRICAL CHARACTERISTICS	4-5
Edits to TPCs	7-9
Edits to HIGH-SPEED, LOW V_{OS} COMPOSITE AMPLIFIER	9