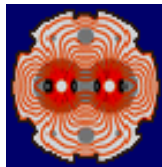


CERN

CH-1211 Geneva 23
Switzerland



The
**Large
Hadron
Collider**
Project

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Engineering Specification

DIAGNOSTIC INTERFACE MODULE FOR POWER CONVERTERS

Abstract

This document describes the physical and electrical properties of the Diagnostic Interface Module (DIM).

Prepared by :
**Christophe Martin
David Nisbet
John Keith Stay**

Checked by :
**André Beuret
Jean-Paul Burnet
Gunnar Fernqvist
Quentin King
Valérie Montabonnet
Jean-Pierre Royer
Hugues Thiesen**

Approved by :
Frédéric Bordry

History of Changes

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0.1 draft	2001-10-26	15	First draft for review.
0.2 draft	2001-10-30	14	Second draft, minor text changes made.
0.3 draft	2001-10-31	14	Third draft,
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3.0	2002-11-28	30	Changed to reflect new connector type. First official release (for P/N AB-685-5092-550).
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3.1	2003-04-15	32	Missing Figure 4-7 physical layout of PCB added.
3.2 draft	2003-10-06	32	Correction to Table 5-1 P/N for "Matching Connector Type. Section 3 "Triggered Acquisition" updated to provide better explanation of the function and timing. AMP connector Data Sheet on page 32 replaced.
3.3	2003-10-20	32	Additional comments from Q. King (page 8 + 28) and V. Montabonnet (page 6) incorporated. Figure 4-7 replaced with Version 2.3 PCB layout. Note added to Section 1.1 regarding signal naming and usage.

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1. PURPOSE

This document describes the physical and electrical properties of the **Diagnostic Interface Module (DIM)** for Power Converters.

The module has been developed for the remote collection of digital and analog information by the Function Generator Controller (FGC) developed by the AB-PO-CC section. While the data source will normally be a power converter, other external equipment may also interface to the system.

Warning

The Diagnostic Interface Module shall under no circumstances be inserted or removed from the host equipment when this is under power. Failure to observe this warning may result in damage to or destruction of the module.

1.1 SUMMARY OF CHANGES

Please note that previous versions of this document and of the hardware described a different type of connector for mating the DIM to its host. The latest document (from Rev. 3.2 onwards) specifies connectors with an integrated extraction mechanism. This change is electrically transparent to the user as the host connector positions and pin-out remains identical. However, the new connectors facilitate easier insertion and removal of the module from its host equipment.

Some other small changes have also been implemented and are listed below:

- change for users in the DIM physical size and height clearance requirement above the host, which are now as follows (see **Figure 4-8**):
Old dimensions L = 99.10mm W = 47.00mm Height = 17.0mm
New dimensions L = 97.79mm W = 53.34mm Height = 20.0mm
- DIAGNOSTIC_SPARE+/- and DIAGNOSTIC_DATA+/- pairs were shorted at the termination. The DIAGNOSTIC_SPARE+/- shall now be looped back to the DIAGNOSTIC_DATA+/- inputs respectively, as shown in Section 4.
- The Digital Input Specification in **Table 5-5** has been modified to show the Sink Current Requirement rather than Input Impedance and the TRIGGER Rise Time requirement has been added.

Note:-The pin connections labelled with the name "SPARE", or including the word "SPARE" are **reserved** for CERN test purposes and or future development and shall not be used for any other purpose in the host equipment.

Using these pins, the loop back installed at the last module in the daisy chain as specified in Section 4.3, allows a continuity check to be carried out of the serial data bus.

1.2 MODULE DEVELOPMENT HISTORY

The development hardware module has been designed by the AB-PO-CC section and carries the following designation:

AB-685-5091-550

A pre-production hardware version carries the following designation:

AB-685-5092-550

The final hardware version for series production will carry the designation:

AB-685-5093-550

The latter designation will also change to the use of the LHC Equipment Identification code for this final version (HCRFBKA____-).

This specification is valid for all of the above versions except as noted in Section 1.1.

2. SCOPE

The purpose of the document is to provide sufficient information to a CERN or Industry user, to facilitate the physical and electrical incorporation of one or more of the Diagnostic Interface Modules into their design.

3. DESCRIPTION

The Diagnostic Interface Module (DIM) is designed for installation in any equipment, for the remote collection of digital and analog information. The module is powered by the user equipment in which it is installed. There are no control functions or hand-shake requirements for the acquisition of data.

Each module functions as a slave device, connected to a serial diagnostic data bus that is controlled by a master device. Each bus may have any number of diagnostic modules (to a maximum of 15) connected in a "daisy-chain". One or two buses are available depending on the user requirements.

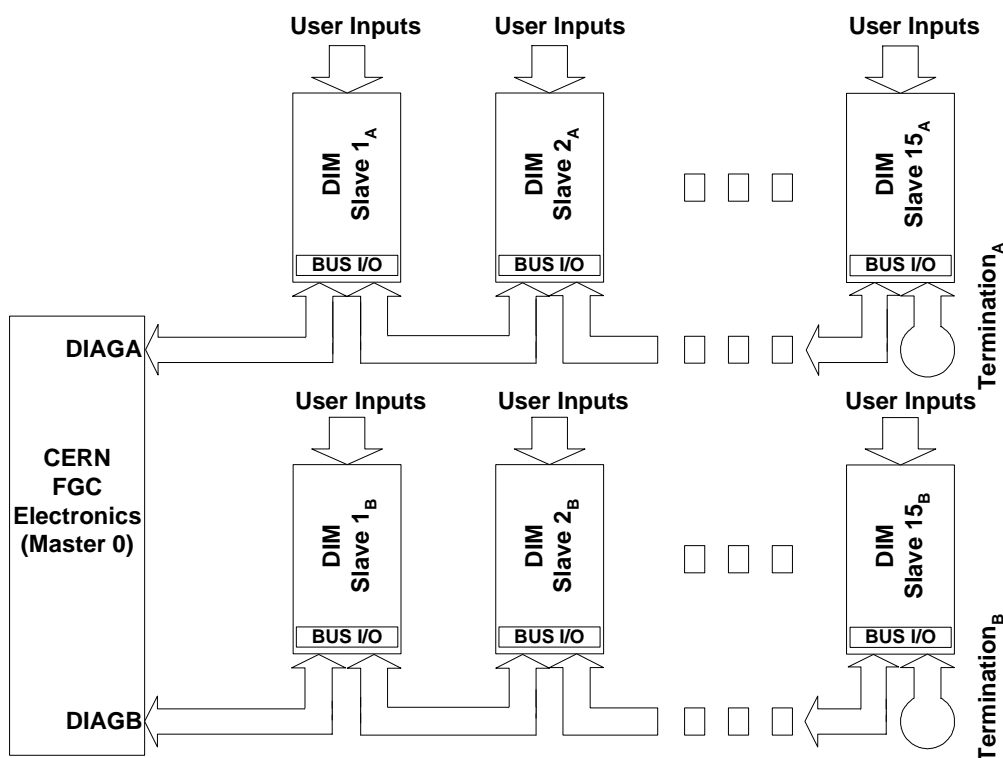


Figure 3-1 Diagnostic Interface Module Installation (General)

All data buses used, shall be correctly terminated (see installation instructions). An unused bus does not require termination.

The Master Module is interfaced internally in the CERN FGC Electronics with the Queued Serial Module (QSM) peripheral infrastructure of the Motorola MC68HC16Z1 microcontroller (HC16).

Three LED's on the back of the module indicate POWER, CLK and TRIG (memorised).

The module may acquire user data using the following acquisition channels:

- Analog (4 inputs)
- Digital (24 inputs)
- Trigger (1 input)
- DALLAS 1-Wire® ID-bus local network (1 Input, 1 Output)

Acquisition

All analog and digital data from all diagnostic modules are acquired by the CERN Function Generator Controller (FGC) Electronics every 20ms. Sampling at this frequency implies a maximum signal bandwidth of 25Hz, thus all analog inputs should be filtered below this frequency to prevent aliasing effects.

Analog Inputs

The 4 analog inputs interface to a 12-bit Analog Digital Converter (ADC) that connects to the controller for subsequent data serialisation. Total accuracy with temperature and linearity effects is specified as 10 bits.

A 2.5V reference voltage used by the ADC is also available to the host device. As a series resistor protects this output, the 2.5V reference should be buffered before use.

Digital Inputs

Each of the 24 digital input bits are pulled up to +5V at the input, filtered with an R-C network and then buffered before serialisation by the controller CPLD.

Triggered Acquisition

A Trigger input is provided for latching the status of the digital inputs DIN00 to DIN23 for fault diagnosis. This allows for determination of which signal initially causes a Fault/Alarm condition. Activation of the trigger stops an internal clock that is subsequently processed by the CERN FGC Electronics, to provide a 1st Fault analysis to a resolution of 8µs.

Analog data acquisition by the DIM is unaffected by the Trigger input.

The latching of the digital inputs, occurs 1µs after the receipt of the '+ve edge transition on the Trigger signal input, allowing for any circuit delays present and de-bouncing of the DIN inputs. The maximum delay between the assertion of the Trigger signal and the assertion of the relevant DIN bits shall be <500ns. The latched inputs will be reset by the DIM controller CPLD once the values have been correctly read out to the FGC.

Following a trigger event, all digital inputs will only return to the normal free-running mode after the reset command has been sent by the FGC – this will normally occur within 100ms. This allows for an immediate return to valid diagnostic data acquisition of the DIN inputs by the DIM, even if the Trigger input has not been reset to "0" by the user, which must occur before any further 1st Fault data can be acquired.

DALLAS 1-Wire® ID Bus Local Network Acquisition

The ID Bus is a network of parallel-connected devices self-powered from the data line and hence may function when the user equipment is not powered. Each device is pre-programmed with a unique identity number

The ID Local bus is an extension of the ID Bus and is used to identify functional units within the user equipment, generally those that may be easily removed. Once in operation, a list of connected units will be automatically generated at regular intervals. With the aid of database systems this information will be a powerful tool for subsequent inventory management.

The following Dallas (now Maxim) semiconductor devices may be connected to a Diagnostic Interface Module ID Local Bus:

- DS2401 TO92 64bit identity tag

- DS2401Z SOT223 64bit identity tag

While the ID Local Bus operates without power, certain guidelines and constraints apply to the installation (see the following installation chapter of this document).

4. INSTALLATION

4.1 SINGLE DIAGNOSTIC MODULE

The information below is valid for systems using only a single Diagnostic Interface Module regardless of ID Local Bus parameters.

Connector J1 (see Section 5 Electrical interface)

- Section 5.1.1 describes the connector analog and digital inputs.
- The equipment 'Sum of faults' generated by the host will normally generate the Trigger.
- Analog inputs should be buffered with a low impedance, current limited voltage source.
- The user may choose to use the Vref output (buffered) when performing a level shift of bipolar analog signals (alternatively an external Vref may be used).
- The user should connect all unused analog and digital inputs to 0V.
- The user should provide the +5V module supply via this connector (see **Table 5-4**).

Connector J2 (see Section 5 Electrical interface)

- The DATA_OUT, CLK_IN, SPARE_IN and ID_OUT pins should be connected to the CERN FGC Electronics DIAGA or DIAGB diagnostic connector. The CERN FGC Electronics connector is defined in the document 'LHC Function Generator Controller Electronics Installation - Interface Specification', EDMS Nr. 339391.
- The DATA_IN, CLK_OUT, SPARE_OUT and ID_IN pins should be terminated according to the data given in Section 4.3 of this chapter. The termination will normally be made on the circuit board where the Diagnostic Interface Module is installed.
- The 'ID Local In' pins should be connected to the user ID Local Bus components following the recommendations in the 'ID Local Bus' section of this chapter. Note that as no further diagnostic modules will be connected in this installation, closing the 'ID Local Bus' loop is not required.
- The 'ID Local Out' pins should be left unconnected.

Single Module Installation Example

An example of a single diagnostic module installation is shown below. **Figure 4-1** shows the connectivity to the CERN FGC Electronics. **Figure 4-2** shows a small ID-bus connection with two components attached, 4 bipolar $\pm 10\text{V}$ analog inputs using the on board reference and some examples of actuation devices attached to the Digital Inputs.

The total number of ID components that can be connected shall be < 100 .

Note that should a high precision analog measurement be required, this example requires the use of low offset op-amps ($< 5\text{mV}$) and high precision resistors (0.1%).

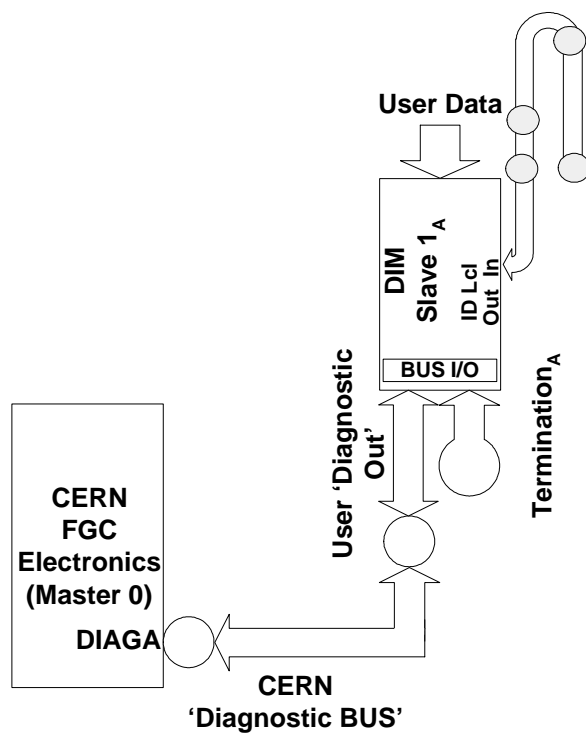
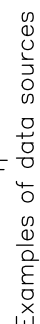


Figure 4-1 Single DIM Module Installation Example (Layout)

1. OpAmp current limit resistor
(digital inputs have internal diode protection)
2. To use full diagnostic resolution,
requires 0.1% matching resistors
3. For full diagnostic resolution,
requires low offset opamp (<5mV)



Note: - The DIAGNOSTIC_SPARE+/- shall be connected to the DIAGNOSTIC_DATA+/- respectively in the host equipment, either on the PCB, or in a termination connector.

4.2 MULTIPLE DIAGNOSTIC INTERFACE MODULES

The information below is valid for all systems using more than one Diagnostic Interface Module (DIM).

For clarification the term “DIM_{PREVIOUS}” refers either to the “Master DIM0” in the FGC or to the next DIM module in the direction **towards** the FGC. The term “DIM_{NEXT}” refers to the first or subsequent DIM modules in the direction **away** from the FGC, as shown in **Figure 4-3**.

General

- No more than 15 modules may be connected on a single bus.
- Modules may be connected together via a cable or by circuit board layout.
- Cable length:
 - Total length from the CERN FGC Electronics to the furthestmost module, not including the ID_local_bus, shall not exceed 100m (measured along the signal path).
 - Total length from the CERN FGC Electronics to the furthestmost module, including the ID_local_bus, shall not exceed 100m (measured along the signal path).
 - The total number of ID components that can be connected shall be <100.

Connector J1 (see Section 5)

- See **Section 4.1: Single Module** for J1 installation guidelines.

Connector J2 (see Section 5)

- The DIM module DATA_OUT, CLK_IN, SPARE_IN and ID_OUT pins should be connected to the DIM_{PREVIOUS} module DATA_IN, CLK_OUT, SPARE_OUT and ID_IN, OR to the CERN FGC Electronics DIAGA or DIAGB diagnostic connector.
 - The CERN FGC Electronics DIAGA/B connector is defined in the document ‘LHC Function Generator Controller Electronics Installation - Interface Specification’, EDMS Nr. 339391.
 - If the DIM is to connect to a DIM_{NEXT} module located in the same equipment, this connection will normally be made on the circuit board where the module is installed.
 - If the DIM is to connect to a DIM_{NEXT} module located outside of the equipment, the relevant equipment Technical Specification will specify the connector to be used.
- The DIM module DATA_IN, CLK_OUT, SPARE_OUT and ID_IN pins should be connected to the DIM_{NEXT} module DATA_OUT, CLK_IN, SPARE_IN and ID_OUT pins, or terminated according to the data given in Section 4.3 of this chapter.
 - If the DIM is to connect to a DIM_{PREVIOUS} module located in the same equipment, this connection will normally be made on the circuit board where the module is installed.
 - If the DIM is to connect to a DIM_{PREVIOUS} module located outside of the equipment, the relevant equipment Technical Specification will specify the connector to be used.

- The 'ID Local In' pins should be connected to the user ID Local Bus following the recommendations in the 'ID Local Bus' section of this chapter. Should the user not require an 'ID Local Bus', the 'ID Local In' pins shall be connected directly to the 'ID Local Out' pins, thus assuring the ID Bus continuity.
- The 'ID Local Out' pins should be connected to the user ID Local Bus following the recommendations in the 'ID Local Bus' section of this chapter.

Multiple Diagnostic Interface Module Installation Example

An example of a multiple DIM module installation is shown below. **Figure 4-3** shows one possible way of connecting 7 modules to the CERN FGC Electronics. **Figure 4-4** shows two modules as they could be connected on a circuit board as part of a multiple DIM module installation.

The first DIM module possesses a Local ID-bus connection, 4 bipolar $\pm 10\text{V}$ analog inputs using the on board reference and some examples of actuation devices. Note that should a high precision analog measurement be required, this example requires use of low offset op-amps ($< 5\text{mV}$) and high precision resistors (0.1%).

The second DIM module has no analog input and only 1 digital input and uses the same trigger as the first module. If this is the last module then a terminating connector should be fitted.

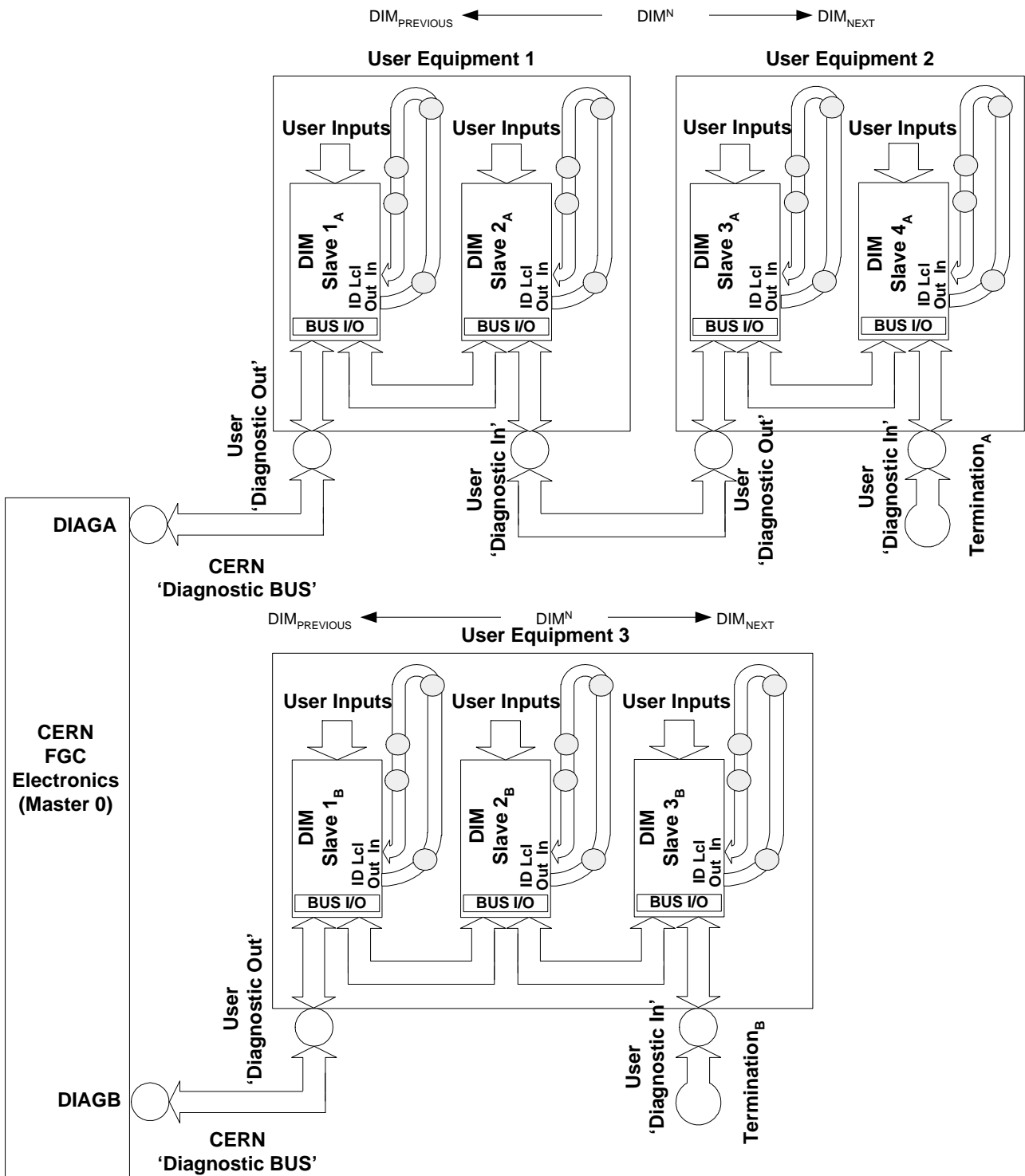


Figure 4-3 Multiple DIM Module Installation Example (Layout)

1. OpAmp current limit resistor
(digital inputs have internal diode protection)
2. To use full diagnostic resolution,
requires 0.1% matching resistors
3. For full diagnostic resolution,
requires low offset opamp (<5mV)

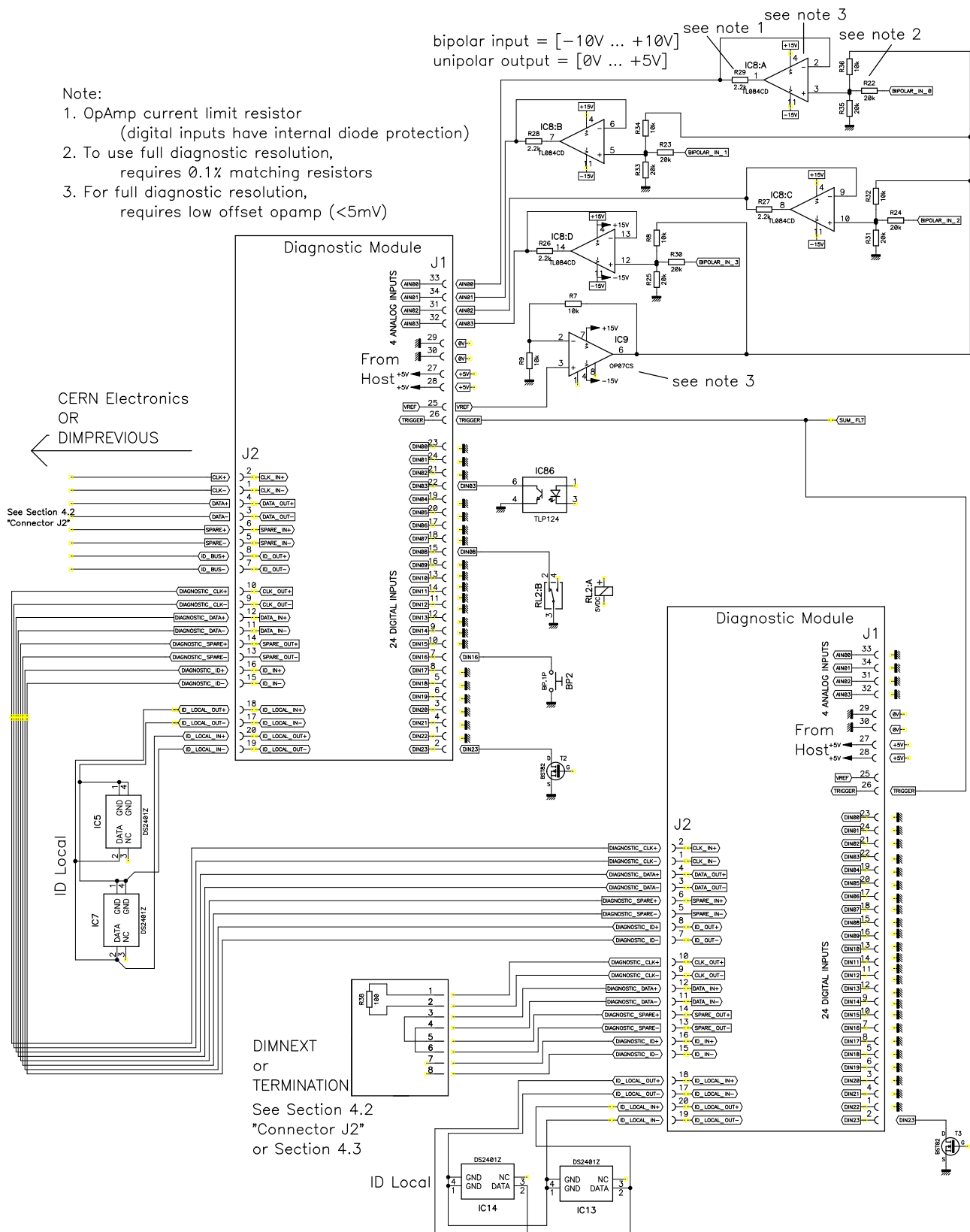


Figure 4-4 Multiple DIM Module Installation Example (Electrical)

Note:- The DIAGNOSTIC_SPARE+/- shall be connected to the DIAGNOSTIC_DATA+/- respectively in the host equipment, either on the PCB, or in the termination connector.

4.3 TERMINATION

The last module on any DIM bus should be terminated as follows:

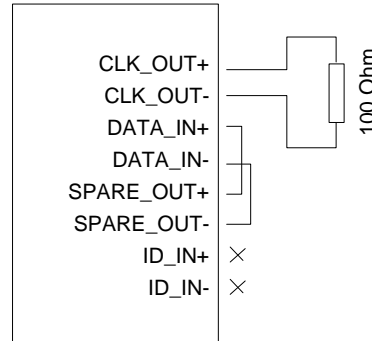


Figure 4-5 Termination Diagram

Termination may be made either:

- on the circuit board where the DIM module is mounted, particularly in the case of a single module installation.
- with a terminating connector, particularly in the case of modular installations where several identical equipments may be connected within the user system

Note:- The DIAGNOSTIC_SPARE+/- shall be connected to the DIAGNOSTIC_DATA+/- respectively in the host equipment, either on the PCB, or in the termination connector.

4.4 DALLAS 1-WIRE ID-BUS LOCAL NETWORK

The 1-Wire ID bus is a part-digital part-analog identification system that exploits variations in system (cable) capacitance, in conjunction with a 9600baud communication protocol, to read all devices found on the bus. Due to the method of operation, the 1-Wire ID Bus is particularly sensitive to network layout and cable capacitance. These are addressed in the notes below.

The 1-Wire ID Bus will generally not be operating when the user equipment is functioning, thus minimising the risk of interference between systems. Operation will be activated by the CERN FGC Electronics only when conditions are acceptable to do so. However, when the user equipment is in standby, there may be signals within the user equipment that could affect the 1-Wire ID Bus signal integrity. For this reason, care should be taken not to route high frequency signals (e.g. system clocks or inverter gate drives) alongside the 1-Wire ID Data Bus, except where these signals are inactive during equipment standby.

Before considering the system further, the 'network weight' must first be understood. Network weight is the given by:

$$W = L + \left(\frac{x}{2} \right)$$

where

L = total network cable length (in metres)

x = total number of ID components on the network

User equipment is considered 'light weight' where $W < 30$. All other users are considered 'heavy weight'.

As with most data lines, impedance mismatching and poor network layout will cause reflections, with a high probability of data corruption. In addition, the 1-Wire ID Bus operation is sensitive to bus capacitance, more so as the bus weight increases. To minimise problems due to these effects the following guidelines are given:

- All 1-Wire ID Data Buses shall be wired in a serial chain (see **Figure 4-6** below). Star connections are forbidden.
- Branches from the 1-Wire ID Data Bus shall be limited to 10cm maximum (see **Figure 4-6** below).
- Light weight users ($W < 30$): internal to the user equipment cable capacitance is considered to be insignificant and is thus not specified. However, cable impedance shall be $100\Omega \pm 20\%$. External to the user equipment a standardised data cable type shall be used (see **Section 5.2**).
- Heavy weight users ($W > 30$): a standardised data cable type shall be used throughout (see **Section 5.2**).
- Where a circuit board is used to route the 1-Wire ID Local Bus, care should be taken to not create a star configuration network but to route as shown in the figure below.

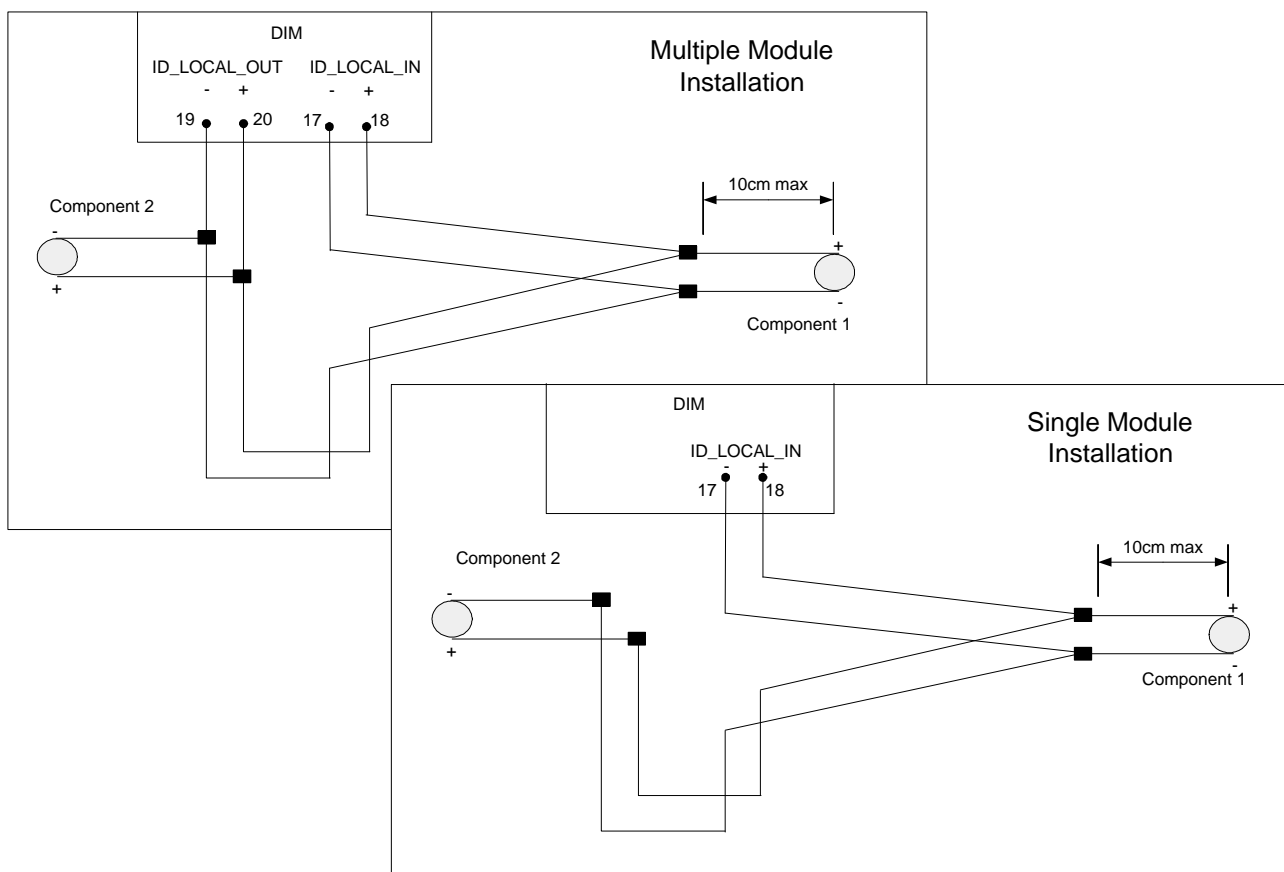


Figure 4-6 1-Wire ID Local Bus – Permitted Network Wiring Diagram

4.5 MECHANICAL

The top (connector) side of the module (Version 2.3) is shown in the **Figure 4-7** below.

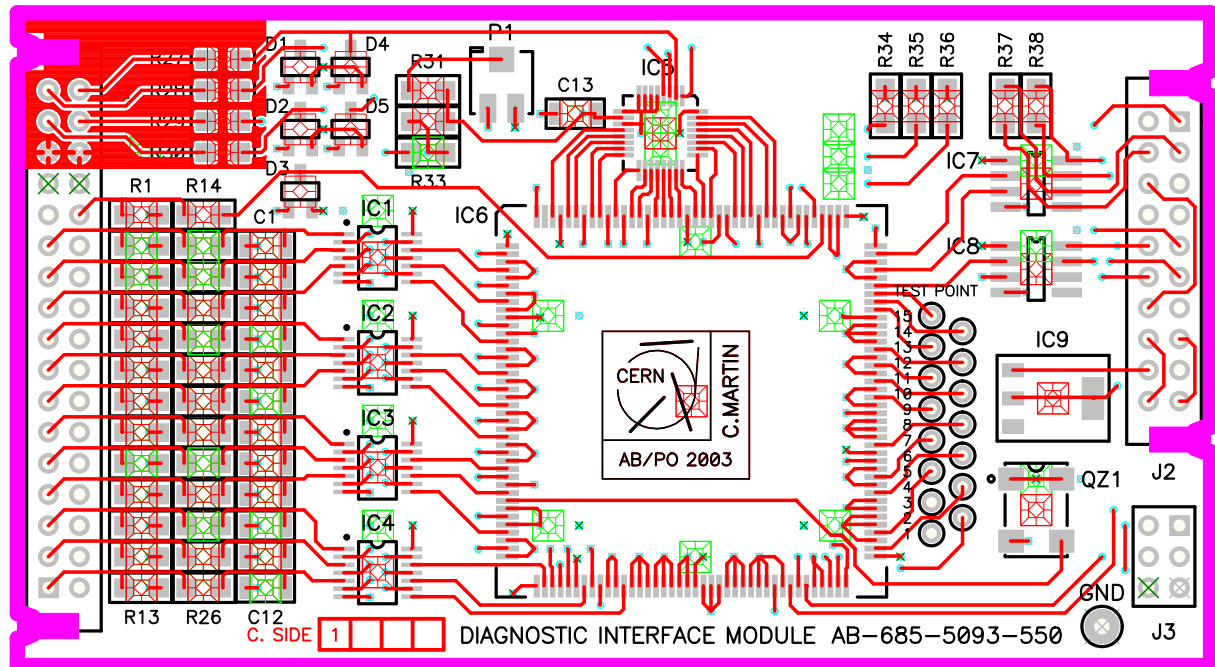


Figure 4-7 Diagnostic Interface Module: Top side layout

The module is constructed as a multi-layer printed circuit board with components mainly mounted on the top side. There are a small number of surface mount decoupling resistors, capacitors and LEDs mounted on the bottom side. The overall module dimensions are 97.79mm x 53.34mm (see **Figure 4-8**).

Located at each end, on the main components side, are the user input/output, CERN input/output and JTAG connectors (J1, J2 and J3 respectively). The JTAG connector J3 is intended solely for use by CERN authorised persons once the module has been removed from the user equipment.

The module is installed as a daughter-board, attached in a piggyback fashion to a larger motherboard. Use of the motherboard area directly below the diagnostic module is permitted, however maximum component height limitations apply (refer to **Figure 4-8** below for physical installation description). Note that the CPLD IC6 (located approximately in the centre of the module), generates some heat and thus the placement of sensitive components facing this location should be avoided.

Due regard should be taken on the host equipment in the areas where the DIM module retaining catches rotate down when extracting the module (see **Figure 4-8**).

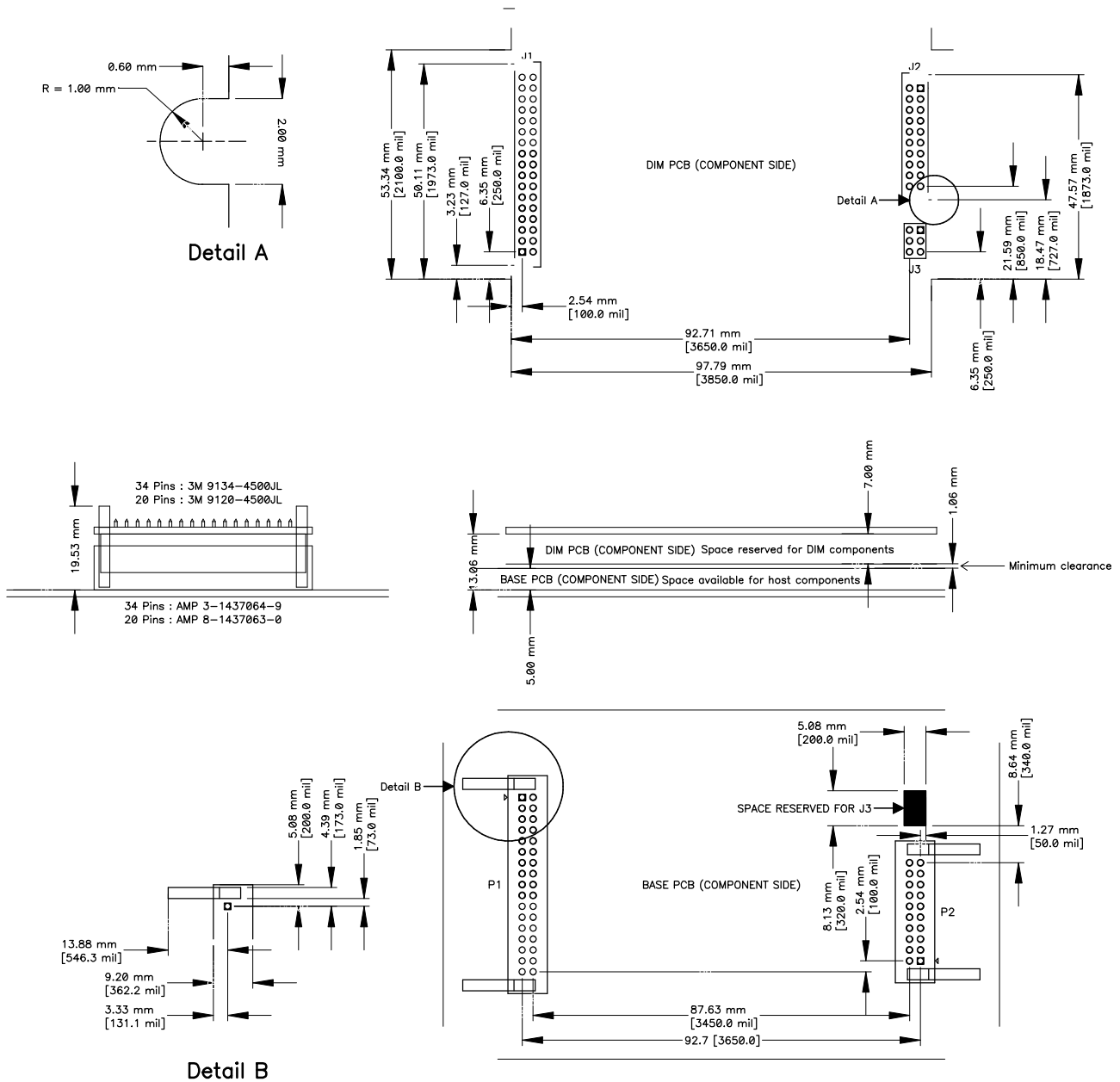


Figure 4-8 DIM Mechanical Dimensions and Installation Diagram

5. ELECTRICAL INTERFACE

5.1 DIAGNOSTIC INTERFACE MODULE CONNECTORS

The connector types specified in the **Table 5-1** and **Table 5-7** provide a simple but effective means for both the mechanical locking in-place and for easy extraction of the DIM modules from their host equipment. The following image shows the 34 pin host side type.

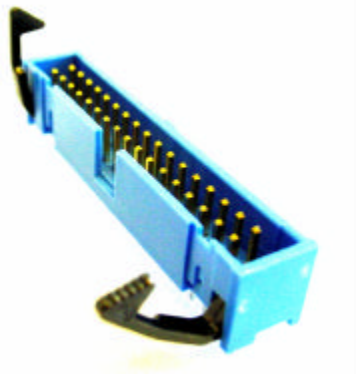


Figure 5-1 Type AMP 3-1437064-9 Host Connector

The data sheet for the required mating connector type in the host equipment can be seen on Page 32 of this document. The WWW site url is:

<http://ecommas.tycoelectronics.com/commerce/DocumentDelivery/DDEController?Action=ecatdrawselcritsIt&Part=1437063-4>

The electrical characteristics of the signal interfaces to the module at J1, and J2 are given in the following section

5.1.1 CONNECTOR J1

5.1.1.1 CONNECTOR TYPE

Connector No.	Module Connector Supplier/Type	Matching Connector Supplier/Type
J1	3M 9134-4500JL	AMP 3-1437064-9 - (See Page 32)

Table 5-1 Connector J1 - Connector type

The connector J1 located on the DIM module provides all of the interconnection with the host equipment for the digital, analog and power signals as listed below.

5.1.1.2 PIN ALLOCATION

J1 Pin number	Signal name
33, 34, 31, 32	AIN00 to AIN03 respectively
29, 30	0V Ground from host
27, 28,	+5V Power from host
25	VREF (External Reference Voltage Output)
26	TRIGGER (1 ST FAULT)
23, 24, 21, 22, 19, 20, 17, 18, 15, 16, 13, 14	DIN00 to DIN11 respectively
11, 12, 9, 10, 7, 8, 5, 6, 3, 4, 1, 2	DIN12 to DIN23 respectively

Table 5-2 Connector J1 – Pin allocation

5.1.1.3 SIGNAL DESCRIPTION

Name	Source/ Destin.	Source Type OC=Open Collector	Parameter	Function
DIN00 to DIN23	User / DIM	OC Output	Hi = [2.0V...Vcc] Lo = [0V ... 0.8V]	DIM module Digital Inputs.
TRIGGER	User / DIM	OC Output	Hi = [2.0V...Vcc] Lo = [0V ... 0.8V]	Latching of DIN00-DIN23 in the DIM module occurs on the positive going edge of this signal
AIN00 to AIN03	User / DIM	Analog Output	0 to +5V	DIM module Analog Inputs 0-3 (non-latched).
VREF	DIM / User	Analog Output	+2.50 VDC Z _{OUT} = 1k Ohm.	Reference Voltage (2.5V) used by the DIM module ADC and made available to the user equipment. If used, it shall be adequately buffered in the host equipment
POWER (Vcc)	User / DIM	+5V ±0.25V Input	<200 mA	Power to the DIM module from the host equipment.
POWER GND	User / DIM	0V		Power return/Ground reference to DIM module from the host

Table 5-3 Connector J1 - Signal Description

Parameter	Min.	Typical	Max.	Unit
Power				
Supply +Vcc	4.75	5	5.25	Volt
Current Consumption	-	<200	-	mA

Table 5-4 Connector J1 – Power Supply Specification

The schematic diagram of the Diagnostic Interface Module Digital, Trigger and Analog Input circuits are shown below:

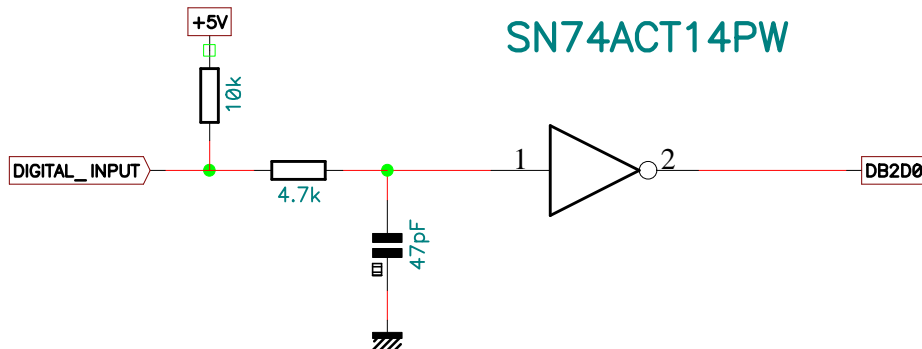


Figure 5-2 Connector J1 - Input Circuit (Digital)

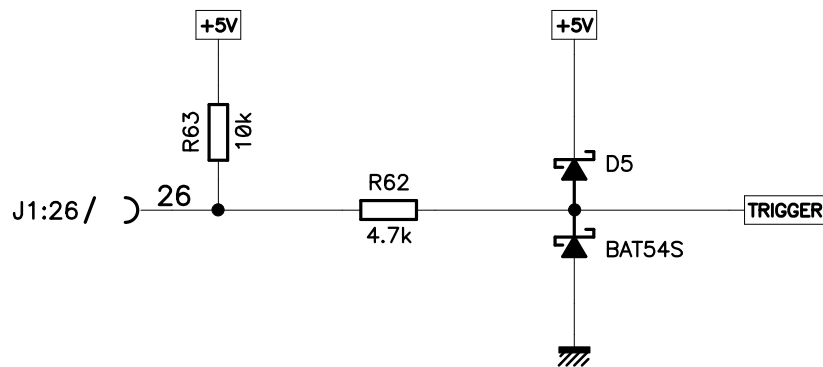


Figure 5-3 Connector J1 - Input Circuit (Trigger)

Parameter	Min.	Typical	Max.	Unit
Digital/Trigger Inputs				
Absolute maximum input	-0.3		Vcc + 0.3	Volt
High Level Threshold	2.0	-	-	Volt
Low Level Threshold	-	-	0.8	Volt
Sink Current Requirement	1	-	-	mA
Trigger Input				
Rise Time (0.8 to 2.0V)	-	-	40	nS

Table 5-5 Connector J1 – Digital Input Specification

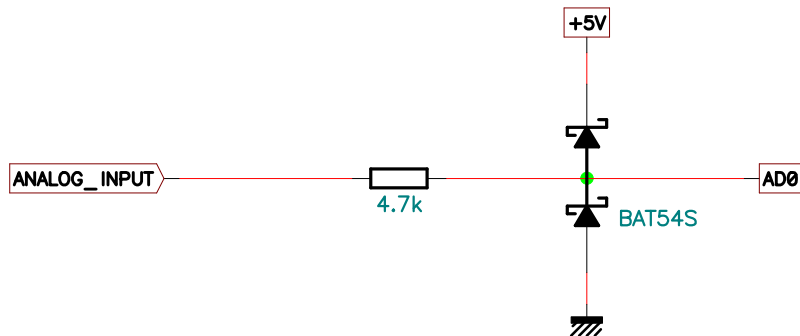


Figure 5-4 Connector J1 - Input Circuit (Analog)

Parameter	Min.	Typical	Max.	Unit
Analog Inputs				
Absolute maximum input	-0.3		Vcc + 0.3V	Volt
Input Voltage Range	0		+5	Volt
Input Impedance	-	5M Ω // 15pF	-	Ohm

Table 5-6 Connector J1 – Analog Input Specification

5.1.2 CONNECTOR J2

5.1.2.1 CONNECTOR TYPE

Connector No.	Module Connector Supplier/Type	Matching Connector Supplier/Type
J2	3M 9120-4500JL	AMP 8-1437063-0 - (See Page 32)

Table 5-7 Connector J2 - Connector type

5.1.2.2 PIN ALLOCATION

J2 Pin number	Signal name	Connection Direction (see Section 4.2)
1	CLK_IN-	DIM _{PREVIOUS}
2	CLK_IN+	
3	DATA_OUT-	
4	DATA_OUT+	
5	SPARE_IN-	
6	SPARE_IN+	
7	ID_OUT-	
8	ID_OUT+	
9	CLK_OUT-	DIM _{NEXT}
10	CLK_OUT+	
11	DATA_IN-	
12	DATA_IN+	
13	SPARE_OUT-	
14	SPARE_OUT+	
15	ID_IN-	
16	ID_IN+	
17	ID_LOCAL_IN-	TO/FROM Local DALLAS ID Devices
18	ID_LOCAL_IN+	
19	ID_LOCAL_OUT-	
20	ID_LOCAL_OUT+	

Table 5-8 Connector J2 – Pin Allocation

5.1.2.3 SIGNAL DESCRIPTION

All signals are differential pairs.

Name	Source/ Destin.	Source Type	Function
CLK_OUT \pm CLK_IN \pm	CERN FGC Electronics / DIM _n	RS485	Parallel 500kHz clock for serialising data
DATA_IN \pm	DIM _{n-1} / DIM _n	RS485	Serial data from preceding DIM module
DATA_OUT \pm	DIM _n / DIM _{n+1}	RS485	Serial data for following DIM module
SPARE_OUT \pm	DIM _n / DIM _{n+1}	RS485	Reserved for internal use by AB/PO/CC
SPARE_IN \pm	DIM _{n-1} / DIM _n	RS485	Reserved for internal use by AB/PO/CC
ID_IN \pm	DIM _{n-1} / DIM _n	1-Wire ID	CERN equipment identifier
ID_OUT \pm	DIM _n / DIM _{n+1}	1-Wire ID	CERN equipment identifier
ID_LOCAL_IN \pm	User ID Local Bus / DIM	1-Wire ID	User equipment identifier
ID_LOCAL_OUT \pm	DIM / User ID Local Bus	1-Wire ID	User equipment identifier

Table 5-9 Connector J2 – Signal Description

5.1.3 CONNECTOR J3

This connector is reserved for programming of the DIM module CPLD integrated circuit. This will be carried out by the responsible CERN staff, during the production phase of the module, or at a later date if a firmware change is required. There shall be no interconnection to the host system with this connector.

5.1.3.1 CONNECTOR TYPE

Connector No.	Module Connector Supplier/Type	Matching Connector Supplier/Type
J3	SAMTEC SSW-103-01-T-D	-

Table 5-10 Connector J3 - Connector type

5.1.3.2 PIN ALLOCATION

J3 Pin number	Signal name
1	TMS
2	TDI
3	TDO
4	TCK
5	0V Ground
6	+5V

Table 5-11 Connector J3 – Pin allocation

5.1.3.3 SIGNAL DESCRIPTION

Name	Source/ Destin.	Source Type OC=Open Collector	Function
TMS	JTAG / DIM	TTL	DIM FPGA device programming
TDI	JTAG / DIM	TTL	DIM FPGA device programming
TDO	JTAG / DIM	TTL	DIM FPGA device programming
TCK	JTAG / DIM	TTL	DIM FPGA device programming
0V Ground	DIM / JTAG	0V	DIM FPGA device programming
+5V	DIM / JTAG	+5V	DIM FPGA device programming

Table 5-12 Connector J3 – Signal Description

5.2 MODULE INTERCONNECTING CABLE

Performance of all the Diagnostic Interface Module functions is only guaranteed where the interconnecting cable meets the following parameters:

Name	Value
EN 50173	Category 5 or better
Wire Construction	Multi-strand
Cable Construction	Twisted pair, Screened
Capacitance / km	<50nF
Nominal Impedence	100 Ω

Table 5-13 Interconnecting Cable Specification

The cable shall correspond to CERN safety instruction 23 for tunnel installation.

A suitable cable, available in the CERN stores, with individually screened pairs and an overall screen is the following:

SCEM Nr. 04.21.70.104.6
 DESCRIPTION CABLE LAN STP 4x2 AWG27/7CAT 6

← [04.21.60](#)

[Group: 04](#)

04.21.70.B - LAN CABLE

General information : [e-mail to Cern Stores](#)


Technical information : [product manager](#)

```

CONSTRUCTION : 4 twisted pair
CONDUCTOR    : Cu Sn AWG 27/7
INSULATION   : PE cellular Ø 1.00 mm
SCREENING     : Polyester aluminium
               Tinned copper braid
SHEATH       : Polyolefine
SPECIFICATIONS
Impedance     : 100 Ohm ± 15 Ohm (f <= 300 MHz)
Mutual capacitance : 48 pF/km
Conductor resistance : 170 Ohm/km
Insulation resistance : 5 GOhm/km
Propagation speed : 0.75
FREQUENCY (MHz)  1    20   100  200  300  600
ATTENUATION (dB/10 m) 0,3  1,3  2,9  4,2  5,2  7,8
  
```

Remarks

[JS 23 SAFETY INSTRUCTION](#)

	SCEM	CONDUCT. Number	DIAMETER mm	SHEATH COLOUR	TYPE
 NEW	04.21.70.104.6	4 x 2	5,8	grey	CAT 6 - STP

The manufactures data sheet is included for reference on the following pages.

**MegaLine 727 flex**

**better than
new Category 6**

Communication Cable 600 MHz

**S/STP 100 ohm
Work-/ Patch Area**

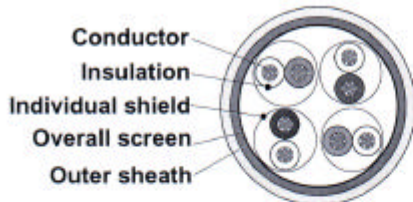
Type: KS-02YSCH 4 x 2 x AWG 27/7 pimf- 100 ohm

Structure:

Conductor: bare copper strands, AWG 27/7
 Insulation: cellular-PE, core-Ø: nom. 1,0 mm
 Pair cabling: 2 cores form a pair,
 Colour code: wt/bl, wt/or, wt/gn, wt/br
 Individual shield: aluminum bonded polyester tape,
 metal side outwards
 Cabling: n pairs twisted together
 Overall screen: tinned copper wire braid
 Outer sheath: halogenfree-compound
 Colour: light-grey - RAL 7035
 flame red - RAL 3000
 rape yellow - RAL 1021
 yellow green - RAL 6018
 sky blue - RAL 5015

Printing:

KERPEN special MegaLine 727 flex, 4P, *H*

**Fields of Application:**

Work area/end user connection, patch panels
 Category 5
 acc. to EN50173, EN50173 2nd. ed., ISO/IEC 11801,
 ISO/IEC 11801 2nd. ed., EN50168
 Category 6
 acc. to ISO/IEC 11801 2nd. ed.
 and prEN 50288-5-2, September 2001
 IEEE 802.3 10 BASE T Ethernet,
 IEEE 802.3u 100 BASE T Fast Ethernet,
 IEEE 802.3ab 1000 BASE T Gigabit Ethernet,
 IEEE 802.5 Token Ring,
 IEEE 802.12 100VG-AnyLAN,
 FDDI on copper, ISDN, B-ISDN,
 ATM, DQDB, Video

Temperature Range:

for fixed installation: - 20 °C to + 60 °C
 for mobile operations: 0 °C to + 50 °C

Bending Radius:

min. 5 x overall diameter

Flame Retardance:

acc. to IEC 60332-3 Cat.C

Absence of Halogens: Smoke Density:

acc. to IEC 60754-2 acc. to IEC 61034

Other characteristics:

Size	Outer-Ø (approx.) Mm	Weight (approx.) kg/km	Calorific value (approx.)		Colour	Part No.
			MJ/m	kWh/m		
4 x 2 x AWG 27/7	5.8	34	0.35	0.1	light-grey	7KS01189
4 x 2 x AWG 27/7	5.8	34	0.35	0.1	flame red	7KS01338
4 x 2 x AWG 27/7	5.8	34	0.35	0.1	rape yellow	7KS01034
4 x 2 x AWG 27/7	5.8	34	0.35	0.1	yellow green	7KS01479
4 x 2 x AWG 27/7	5.8	34	0.35	0.1	sky blue	7KS01480



Communication Cable 600 MHz

S/STP 100 ohm
Work-/ Patch Area

Type: KS-02YSCH 4 x 2 x AWG 27/7 pimf- 100 ohm

MegaLine 727 flex

better than
new Category 6

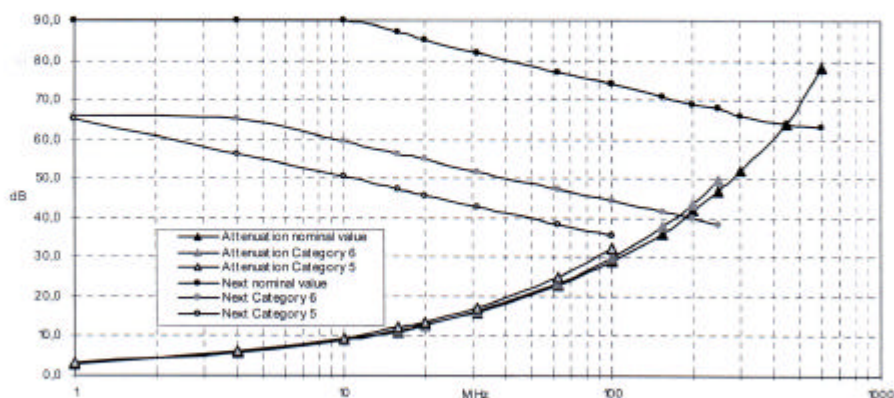
Electrical characteristics at 20 °C:

DC resistance:	max.	170	ohm/km
Insulation resistance:	min.	5	Gohmxkm
Mutual capacitance:	nominal value	48	pF/m
Transfer capacitance (e):	approx.	0.75	c
Signal velocity:	approx.	440	ns/100 m
Skew:	approx.	12	ns/100 m at 100 MHz
Characteristic impedance:		100 Ohm \pm 5 Ω	at 100 MHz
Transfer impedance	max.	10 mohm/m	at 10 MHz acc. to IEC 96-1; A 5.2
Screening attenuation	nominal value	60 dB	up to 1000 MHz
Coupling attenuation:	nominal value	90 dB	up to 1000 MHz
Test voltage U_{eff} :		1000	V
Operating voltage U_{eff} :	max.	125	V

Frequency (MHz)	Attenuation (dB/100m)		Next (dB)		ACR (dB/100m)		PS-NEXT (dB)		PS-ACR (dB/100m)		EL-FEXT (dB/100m)		PS-EL-FEXT (dB/100m)		RL** (dB)	
	nom.	Cat.6* (max.)	nom.	Cat.6* (min.)	nom.	Cat.6* (min.)	nom.	Cat.6* (min.)	nom.	Cat.6* (min.)	nom.	Cat.6* (min.)	nom.	Cat.6* (min.)	nom.	Cat.6* (min.)
1	3,1	3,1	90,0	66,0	86,9	62,9	87,0	64,0	83,9	60,9	90,0	n.def	87,0	n.def	n.def	n.def
4	5,1	5,7	90,0	65,3	84,9	59,5	87,0	63,3	81,9	57,6	90,0	58,0	87,0	55,0	24,0	23,0
10	8,7	9,0	90,0	59,3	81,3	50,3	87,0	57,3	78,3	48,3	90,0	50,0	87,0	47,0	30,0	25,0
16	11,2	11,4	87,0	56,2	75,8	44,8	84,0	54,2	72,8	42,8	85,0	45,9	82,0	43,0	30,0	25,0
20	12,5	12,8	85,0	54,8	72,5	42,0	82,0	52,8	69,5	40,0	80,0	44,0	77,0	41,0	28,0	25,0
31,25	15,7	16,1	82,0	51,9	66,3	35,8	79,0	49,9	63,3	33,8	70,0	40,1	67,0	37,1	26,0	23,6
62,5	22,8	23,2	77,0	47,4	54,2	24,1	74,0	45,4	51,2	22,2	60,0	34,1	57,0	31,1	25,0	21,5
100	29,4	29,9	74,0	44,3	44,6	14,4	71,0	42,3	41,6	12,4	50,0	30,0	47,0	27,0	24,0	20,1
155	36,8	37,9	71,0	41,4	34,2	3,5	68,0	39,4	31,2	1,5	45,0	26,2	42,0	23,2	22,0	18,8
200	42,0	43,7	69,0	39,8	27,0	-3,9	66,0	37,8	24,0	-5,9	40,0	24,0	37,0	21,0	20,0	18,0
250	46,5	49,5	68,0	38,3	21,5	-11,2	65,0	36,3	18,5	-13,2	35,0	22,0	32,0	19,0	20,0	17,3
300	51,2	n.def	66,0	n.def	14,8	n.def	63,0	n.def	11,8	n.def	30,0	n.def	27,0	n.def	18,0	n.def
450	64,0	n.def	64,0	n.def	0,0	n.def	61,0	n.def	-3,0	n.def	25,0	n.def	22,0	n.def	n.def	n.def
600	77,0	n.def	63,0	n.def	-14,0	n.def	60,0	n.def	-17,0	n.def	20,0	n.def	17,0	n.def	n.def	n.def

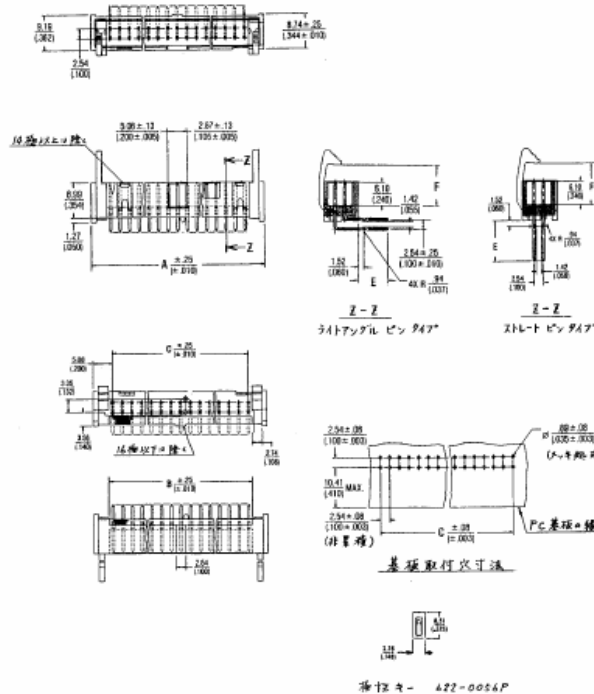
* prEN 50288-5-2, September 2001

** f.f.s



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REVISED			
REV	DATE	DESCRIPTION	BY
0		Released (FJ00-1640-00)	



材料	
基板材料	ガラスエポキシ樹脂 (54V-0) 色調: 青
コンタクト	リン青銅
コンタクトメッキ	ニッケル下地に金メッキ
電気的規格	
定格電圧	1A
絶縁電圧	>1kVDC
絶縁耐圧	>300VDC (SEA LEVEL)
温度特性	標準的規格
定格温度	-55°C ~ 105°C

注 1. 旧型番記載の説明

製品コード	501-△△□□
極数	7
タイプ	0: ライトアングル 11.5E 極数 1: ライトアングル 13.1E 極数 2: ストレート 11.5E 極数 3: ストレート 13.1E 極数

E: ストレインリリーフ無し、フィメラルソケット用ラッチ付
ES: ストレインリリーフ付、フィメラルソケット用ラッチ付
シリーズコード

型番				寸法 MM(INCHES)				ストレーンリリーフ無し (TYPE E)		ストレーンリリーフ付 (TYPE ES)	
1.58(.062) プリント基板厚	3.18(.125) プリント基板厚	1.58(.062) プリント基板厚	3.18(.125) プリント基板厚	極数	A	B	C	F	F	F	F
2.59±.25 (.102±.010)	4.11±.25 (.162±.010)	2.59±.25 (.102±.010)	4.11±.25 (.162±.010)								
1437063-4	1437063-8	501-0607ES 501-0607XX	501-0617XX	501-0627ES 501-0627XX	6	15.24(.600)	7.11(.280)	5.08(.200)			
2-1437063-3	2-1437063-8 3-1437063-0	501-1007ES 501-1007XX	501-1017XX	501-1027ES 501-1027XX	10	20.32(.800)	12.19(.480)	10.16(.400)			
4-1437063-6	5-1437063-3	501-1207ES 501-1207XX	501-1217XX	501-1227ES 501-1227XX	12	22.86(.900)	14.73(.580)	12.70(.500)			
5-1437063-8	6-1437063-4 6-1437063-7	501-1407ES 501-1407XX	501-1417XX	501-1427ES 501-1427XX	14	25.40(1.000)	17.27(.680)	15.24(.600)			
7-1437063-1 7-1437063-3 8-1437063-7	8-1437063-0 8-1437063-1 9-1437063-1	501-1607ES 501-1607XX	501-1617XX	501-1627ES 501-1627XX	16	27.94(1.100)	19.81(.780)	17.78(.700)			
9-1437063-7	1437064-3 1437064-5	501-2007ES 501-2007XX	501-2017XX	501-2027ES 501-2027XX	20	33.02(1.300)	24.89(.980)	22.86(.900)			
1-1437064-5	2-1437064-3	501-2407ES 501-2407XX	501-2417XX	501-2427ES 501-2427XX	24	38.10(1.500)	29.97(1.180)	27.94(1.100)	10.54 (.415)	14.61 (.575)	
3-1437064-5	3-1437064-9 4-1437064-1	501-2607ES 501-2607XX	501-2617XX	501-2627ES 501-2627XX	26	40.64(1.600)	32.51(1.280)	30.48(1.200)			
4-1437064-9	5-1437064-3	501-3007ES 501-3007XX	501-3017XX	501-3027ES 501-3027XX	30	45.72(1.800)	37.59(1.480)	35.56(1.400)			
5-1437064-6 5-1437064-8	6-1437064-8 7-1437064-0	501-3407ES 501-3407XX	501-3417XX	501-3427ES 501-3427XX	34	50.80(2.000)	42.67(1.680)	40.64(1.600)			
9-1437064-1	9-1437064-5 9-1437064-8 1437065-1	501-3607ES 501-3607XX	501-3617XX	501-3627ES 501-3627XX	36	53.34(2.100)	45.21(1.780)	43.18(1.700)			
2-1437065-0		501-4007ES 501-4007XX	501-4017XX	501-4027ES 501-4027XX	40	58.42(2.300)	50.29(1.980)	48.26(1.900)			
3-1437065-5	4-1437065-0	501-4407ES 501-4407XX	501-4417XX	501-4427ES 501-4427XX	44	63.50(2.500)	55.37(2.180)	53.34(2.100)			
		501-5007ES 501-5007XX	501-5017XX	501-5027ES 501-5027XX	50	71.12(2.800)	62.99(2.480)	60.96(2.400)			
		501-6007ES 501-6007XX	501-6017XX	501-6027ES 501-6027XX	60	83.82(3.300)	75.69(2.980)	73.66(2.900)			
		501-6407ES 501-6407XX	501-6417XX	501-6427ES 501-6427XX	64	88.90(3.500)	80.77(3.180)	78.74(3.100)			

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DESIGNED: *[Signature]* CHECKED: *[Signature]*

REVISIONS: 1. 1.58(.062) プリント基板厚 2. 3.18(.125) プリント基板厚 3. 1.58(.062) プリント基板厚 4. 3.18(.125) プリント基板厚

APPLICATION SPEC: 1. 1.58(.062) プリント基板厚 2. 3.18(.125) プリント基板厚 3. 1.58(.062) プリント基板厚 4. 3.18(.125) プリント基板厚

MATERIAL: 1. 1.58(.062) プリント基板厚 2. 3.18(.125) プリント基板厚 3. 1.58(.062) プリント基板厚 4. 3.18(.125) プリント基板厚

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CUSTOMER DRAWING: 1. 1.58(.062) プリント基板厚 2. 3.18(.125) プリント基板厚 3. 1.58(.062) プリント基板厚 4. 3.18(.125) プリント基板厚

AMP Tyco Electronics AMP K.K. Kawasaki, Japan

バーティカル イジェクタ ヘッダー
VERTICAL EJECTOR HEADER

SIZE: A2 CASE CODE: 00779 DRAWING NO: 1437063-4

REVISION: 1. 1.58(.062) プリント基板厚 2. 3.18(.125) プリント基板厚 3. 1.58(.062) プリント基板厚 4. 3.18(.125) プリント基板厚

DATE: 1/22/00

SHEET: 1 OF 1