

N-Channel MOSFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. A proprietary planar stripe design yields excellent reliability and manufacturability. Low switching loss is achieved with low input capacitance and ultra low C_{rss} "Miller" capacitance. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control slew rates during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency. Reliability in flyback, boost, forward, and other circuits is enhanced by the high avalanche energy capability.



IS OTO P*
APT100M50J
 "UL Recognized" file # E145592

Single die MOSFET



FEATURES

- Fast switching with low EMI/RFI
- Low $R_{DS(on)}$
- Ultra low C_{rss} for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant 

TYPICAL APPLICATIONS

- PFC and other boost converter
- Buck converter
- Two switch forward (asymmetrical bridge)
- Single switch forward
- Flyback
- Inverters

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	103	A
	Continuous Drain Current @ $T_C = 100^\circ\text{C}$	65	
I_{DM}	Pulsed Drain Current ^①	490	
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy ^②	3350	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	75	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$			960	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.13	$^\circ\text{C/W}$
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.15		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55		150	$^\circ\text{C}$
$V_{Isolation}$	RMS Voltage (50-60Hz Sinusoidal Waveform from Terminals to Mounting Base for 1 Min.)	2500			V
W_T	Package Weight		1.03		oz
			29.2		g
Torque	Terminals and Mounting Screws.			10	in·lbf
				1.1	N·m

Static Characteristics

$T_J = 25^{\circ}\text{C}$ unless otherwise specified

APT100M50J

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	500			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to $25^{\circ}\text{C}, I_D = 250\mu A$		0.60		V/ $^{\circ}\text{C}$
$R_{DS(on)}$	Drain-Source On Resistance ^③	$V_{GS} = 10V, I_D = 75A$		0.028	0.036	Ω
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 5mA$	3	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient			-10		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500V$ $V_{GS} = 0V$			100	μA
		$T_J = 25^{\circ}\text{C}$ $T_J = 125^{\circ}\text{C}$			500	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 30V$			± 100	nA

Dynamic Characteristics

$T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}	Forward Transconductance	$V_{DS} = 50V, I_D = 75A$		115		S
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1MHz$		24600		pF
C_{rss}	Reverse Transfer Capacitance			330		
C_{oss}	Output Capacitance			2645		
$C_{o(cr)}^{④}$	Effective Output Capacitance, Charge Related	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 333V$		1535		
$C_{o(er)}^{⑤}$	Effective Output Capacitance, Energy Related			775		
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10V, I_D = 75A,$ $V_{DS} = 250V$		620		nC
Q_{gs}	Gate-Source Charge			140		
Q_{gd}	Gate-Drain Charge			280		
$t_{d(on)}$	Turn-On Delay Time	Resistive Switching $V_{DD} = 333V, I_D = 75A$ $R_G = 2.2\Omega^{⑥}, V_{GG} = 15V$		105		ns
t_r	Current Rise Time			125		
$t_{d(off)}$	Turn-Off Delay Time			280		
t_f	Current Fall Time			90		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)			103	A
I_{SM}	Pulsed Source Current (Body Diode) ^①				490	
V_{SD}	Diode Forward Voltage	$I_{SD} = 75A, T_J = 25^{\circ}\text{C}, V_{GS} = 0V$			1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 75A^{②}$ $di_{SD}/dt = 100A/\mu s, T_J = 25^{\circ}\text{C}$		855		ns
Q_{rr}	Reverse Recovery Charge			35		μC
dv/dt	Peak Recovery dv/dt	$I_{SD} \leq 75A, di/dt \leq 1000A/\mu s, V_{DD} = 100V,$ $T_J = 125^{\circ}\text{C}$			8	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at $T_J = 25^{\circ}\text{C}, L = 1.19mH, R_G = 2.2\Omega, I_{AS} = 75A$.

③ Pulse test: Pulse Width < 380 μs , duty cycle < 2%.

④ $C_{o(cr)}$ is defined as a fixed capacitance with the same stored charge as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$.

⑤ $C_{o(er)}$ is defined as a fixed capacitance with the same stored energy as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$. To calculate $C_{o(er)}$ for any value of V_{DS} less than $V_{(BR)DSS}$, use this equation: $C_{o(er)} = -5.71E-7/V_{DS}^2 + 1.33E-7/V_{DS} + 3.80E-10$.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

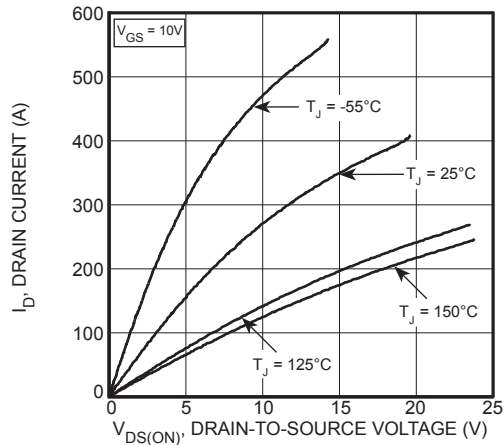


Figure 1, Output Characteristics

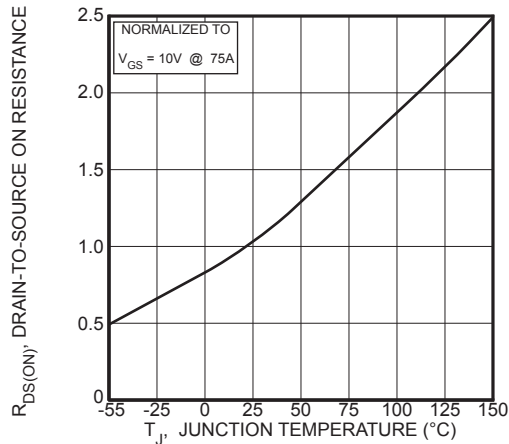
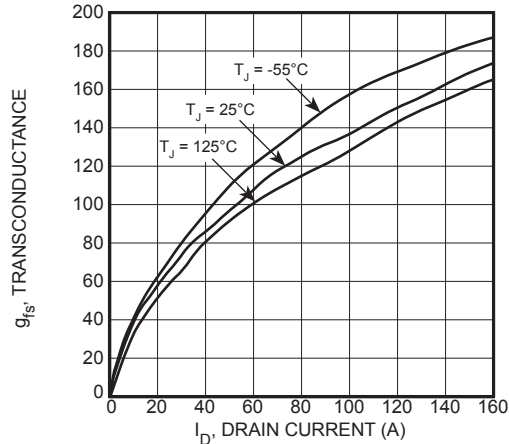
Figure 3, $R_{DS(ON)}$ vs Junction Temperature

Figure 5, Gain vs Drain Current

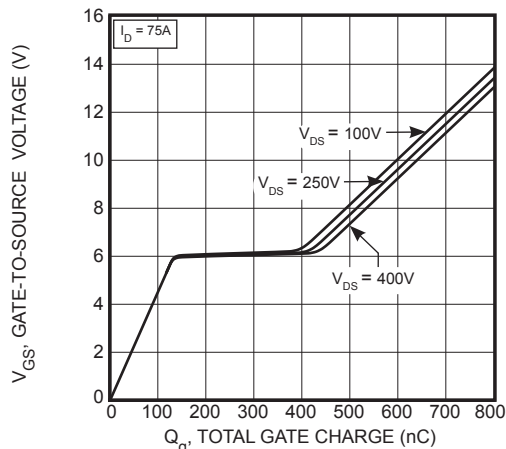


Figure 7, Gate Charge vs Gate-to-Source Voltage

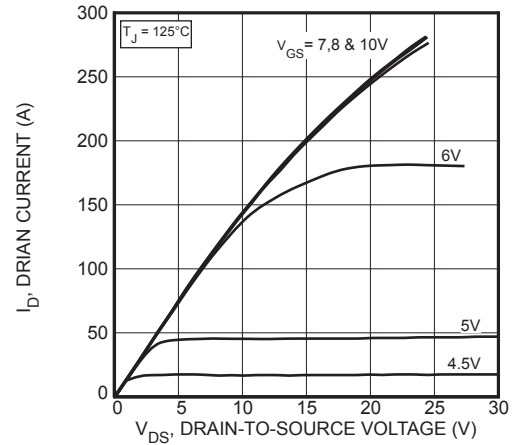


Figure 2, Output Characteristics

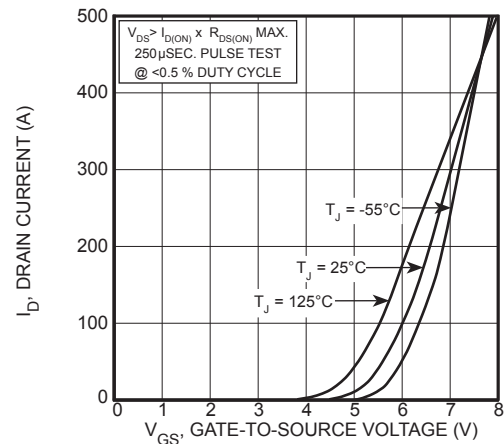


Figure 4, Transfer Characteristics

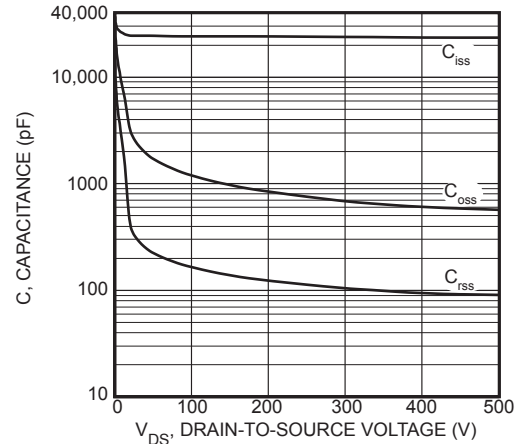


Figure 6, Capacitance vs Drain-to-Source Voltage

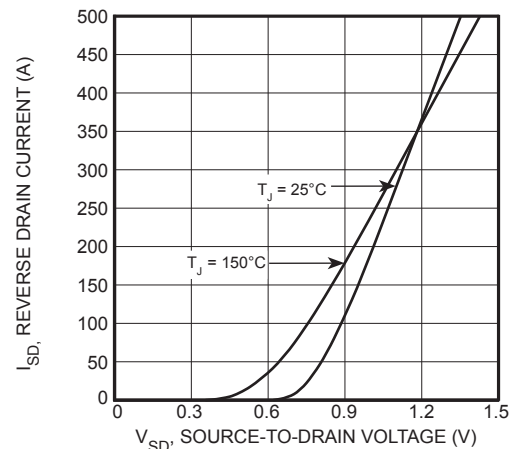
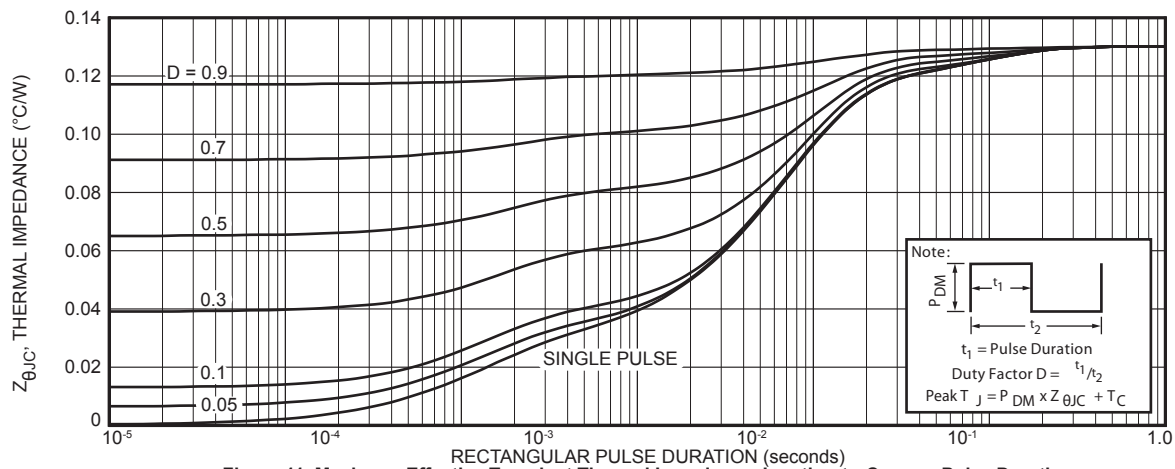
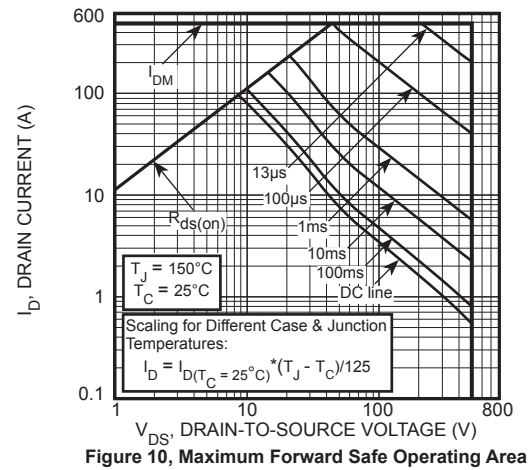
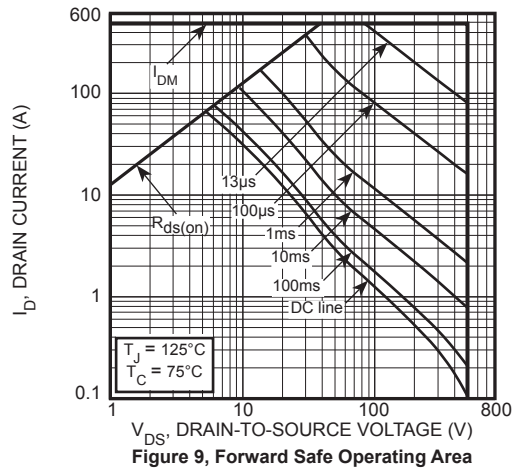
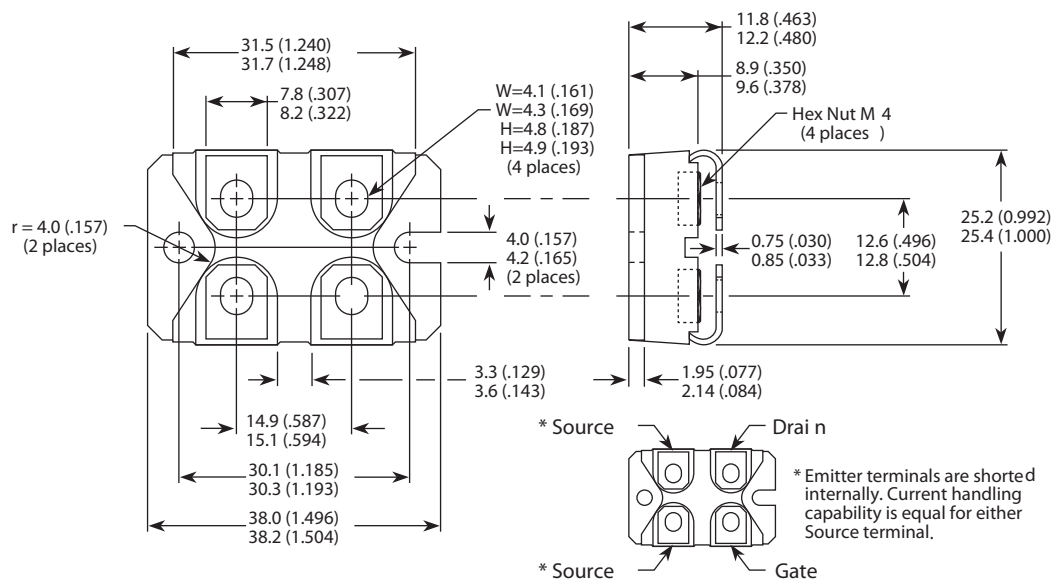


Figure 8, Reverse Drain Current vs Source-to-Drain Voltage



SOT-227 (ISOTOP®) Package Outline



Dimensions in Millimeters and (Inches)