

## *Memory FRAM*

# 4 M Bit (512 K × 8)

## MB85R4001A

### ■ DESCRIPTIONS

The MB85R4001A is an FRAM (Ferroelectric Random Access Memory) chip consisting of 524,288 words × 8 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85R4001A is able to retain data without using a back-up battery, as is needed for SRAM.

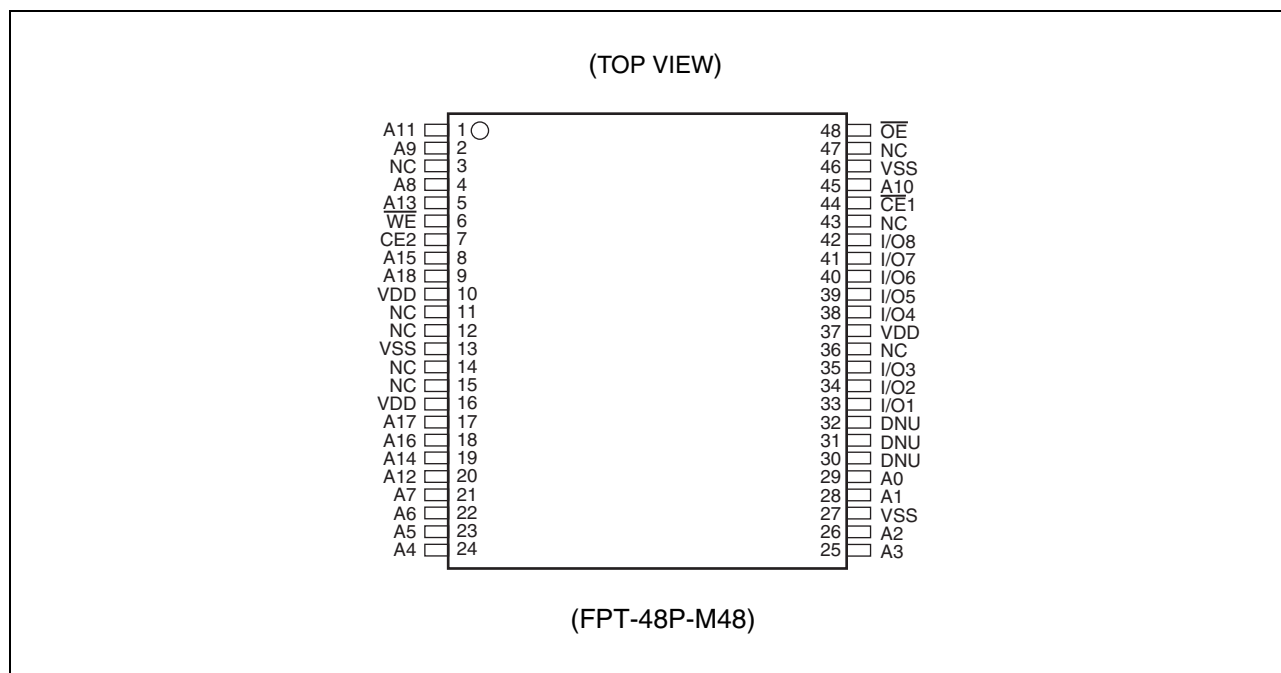
The memory cells used in the MB85R4001A can be used for  $10^{10}$  read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E<sup>2</sup>PROM.

The MB85R4001A uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

### ■ FEATURES

- Bit configuration : 524,288 words × 8 bits
- Read/write endurance :  $10^{10}$  times
- Operating power supply voltage : 3.0 V to 3.6 V
- Operating temperature range : - 40 °C to + 85 °C
- Data retention : 10 years ( + 55 °C)
- Package : 48-pin plastic TSOP (1)

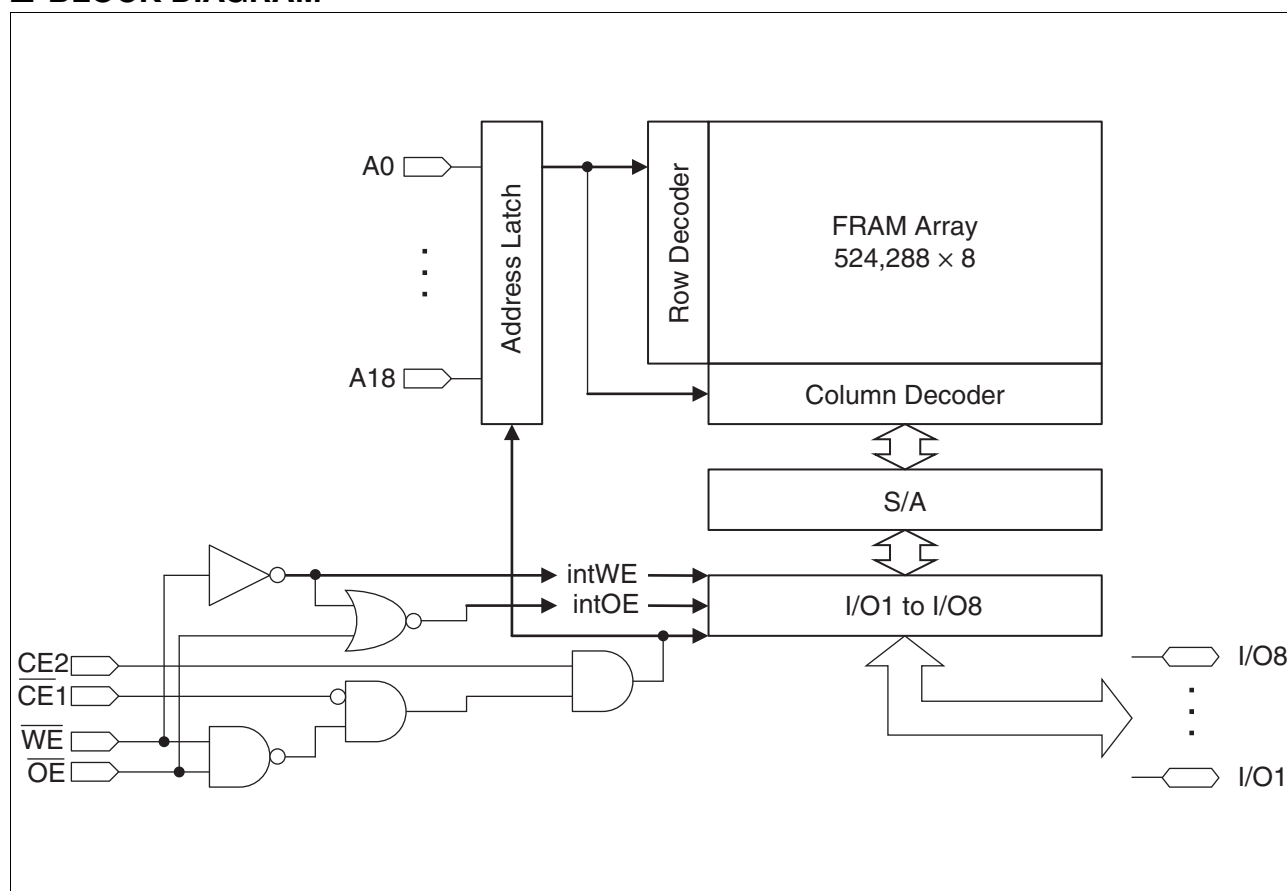
## PIN ASSIGNMENTS



## PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1, 2, 4, 5, 8, 9, 17 to 26, 28, 29, 45	A0 to A18	Address Input pins
33 to 35, 38 to 42	I/O1 to I/O8	Data Input/Output pins
44	$\overline{CE}1$	Chip Enable 1 Input pin
7	CE2	Chip Enable 2 Input pin
6	$\overline{WE}$	Write Enable Input pin
48	$\overline{OE}$	Output Enable Input pin
10, 16, 37	VDD	Supply Voltage pins Connect all three pins to the power supply.
13, 27, 46	VSS	Ground pins Connect all three pins to ground.
3, 11, 12, 14, 15, 36, 43, 47	NC	No Connect pins
30 to 32	DNU	Do Not Use pins Make sure to connect these pins to ground.

## ■ BLOCK DIAGRAM



## ■ FUNCTIONAL TRUTH TABLE

Operation Mode	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	I/O <sub>1</sub> to I/O <sub>8</sub>	Supply Current
Standby Precharge	H	X	X	X	Hi-Z	Standby (I <sub>SB</sub> )
	X	L	X	X		
	X	X	H	H		
Read	$\overline{\downarrow}$	H	H	L	Data Output	Operation (I <sub>CC</sub> )
	L	$\uparrow$				
Read (Pseudo-SRAM, $\overline{OE}$ control*1)	L	H	H	$\overline{\downarrow}$		
Write	$\overline{\downarrow}$	H	L	H	Data Input	
	L	$\uparrow$				
Write (Pseudo-SRAM, $\overline{WE}$ control*2)	L	H	$\overline{\downarrow}$	H		

Note: L = V<sub>IL</sub>, H = V<sub>IH</sub>, X can be either V<sub>IL</sub> or V<sub>IH</sub>, Hi-Z = High Impedance

$\downarrow$  : Latch address and latch data at falling edge,  $\uparrow$  : Latch address and latch data at rising edge

\*1 :  $\overline{OE}$  control of the Pseudo-SRAM means the valid address at the falling edge of  $\overline{OE}$  to read.

\*2 :  $\overline{WE}$  control of the Pseudo-SRAM means the valid address and data at the falling edge of  $\overline{WE}$  to write.

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	$V_{CC}$	- 0.5	+ 4.0	V
Input Pin Voltage*	$V_{IN}$	- 0.5	$V_{CC} + 0.5 ( \leq 4.0 )$	V
Output Pin Voltage*	$V_{OUT}$	- 0.5	$V_{CC} + 0.5 ( \leq 4.0 )$	V
Operating Ambient Temperature	$T_A$	- 40	+ 85	°C
Storage Temperature	$T_{STG}$	- 40	+ 125	°C

\* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage*	$V_{CC}$	3.0	3.3	3.6	V
High Level Input Voltage*	$V_{IH}$	$V_{CC} \times 0.8$	—	$V_{CC} + 0.5 ( \leq 4.0 )$	V
Low Level Input Voltage*	$V_{IL}$	- 0.5	—	+ 0.6	V
Operating Ambient Temperature	$T_A$	- 40	—	+ 85	°C

\* : All voltages are referenced to VSS (ground 0 V).

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current*3	$ I_{LI} $	$V_{IN} = 0 \text{ V to } V_{CC}$	—	—	10	$\mu\text{A}$
Output Leakage Current	$ I_{LO} $	$V_{OUT} = 0 \text{ V to } V_{CC},$ $\overline{CE1} = V_{IH} \text{ or } \overline{OE} = V_{IH}$	—	—	10	$\mu\text{A}$
Operating Power Supply Current	$I_{CC}$	$\overline{CE1} = 0.2 \text{ V}, \overline{CE2} = V_{CC}-0.2 \text{ V},$ $I_{out} = 0 \text{ mA}^{*1}$	—	15	20	$\text{mA}$
Standby Current	$I_{SB}$	$\overline{CE1} \geq V_{CC}-0.2 \text{ V}$	—	50	150	$\mu\text{A}$
		$\overline{CE2} \leq 0.2 \text{ V}^{*2}$				
		$\overline{OE} \geq V_{CC}-0.2 \text{ V}, \overline{WE} \geq V_{CC}-0.2 \text{ V}^{*2}$				
High Level Output Voltage	$V_{OH}$	$I_{OH} = -1.0 \text{ mA}$	$V_{CC} \times 0.8$	—	—	$\text{V}$
Low Level Output Voltage	$V_{OL}$	$I_{OL} = 2.0 \text{ mA}$	—	—	0.4	$\text{V}$

\*1 : During the measurement of  $I_{CC}$ , the Address, Data In were taken to only change once per active cycle.  
 $I_{out}$ : output current

\*2 : All pins other than setting pins should be input at the CMOS level voltages such as  $H \geq V_{CC} - 0.2 \text{ V}$ ,  $L \leq 0.2 \text{ V}$ .

\*3 : This also applies to DNU pins.

## 2. AC Characteristics

### • AC Test Conditions

Supply Voltage	: 3.0 V to 3.6 V
Operating Ambient Temperature	: -40 °C to +85 °C
Input Voltage Amplitude	: 0.3 V to 2.7 V
Input Rising Time	: 5 ns
Input Falling Time	: 5 ns
Input Evaluation Level	: 2.0 V / 0.8 V
Output Evaluation Level	: 2.0 V / 0.8 V
Output Impedance	: 50 pF

#### (1) Read Cycle

(within recommended operating conditions)

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle Time	$t_{RC}$	150	—	ns
$\overline{CE}1$ Active Time	$t_{CA1}$	120	—	ns
$\overline{CE}2$ Active Time	$t_{CA2}$	120	—	ns
$\overline{OE}$ Active Time	$t_{RP}$	120	—	ns
Precharge Time	$t_{PC}$	20	—	ns
Address Setup Time	$t_{AS}$	0	—	ns
Address Hold Time	$t_{AH}$	50	—	ns
$\overline{OE}$ Setup Time	$t_{ES}$	0	—	ns
Output Hold Time	$t_{OH}$	0	—	ns
Output Set Time	$t_{LZ}$	30	—	ns
$\overline{CE}1$ Access Time	$t_{CE1}$	—	120	ns
$\overline{CE}2$ Access Time	$t_{CE2}$	—	120	ns
$\overline{OE}$ Access Time	$t_{OE}$	—	120	ns
Output Floating Time	$t_{OHZ}$	—	20	ns

#### (2) Write Cycle

(within recommended operating conditions)

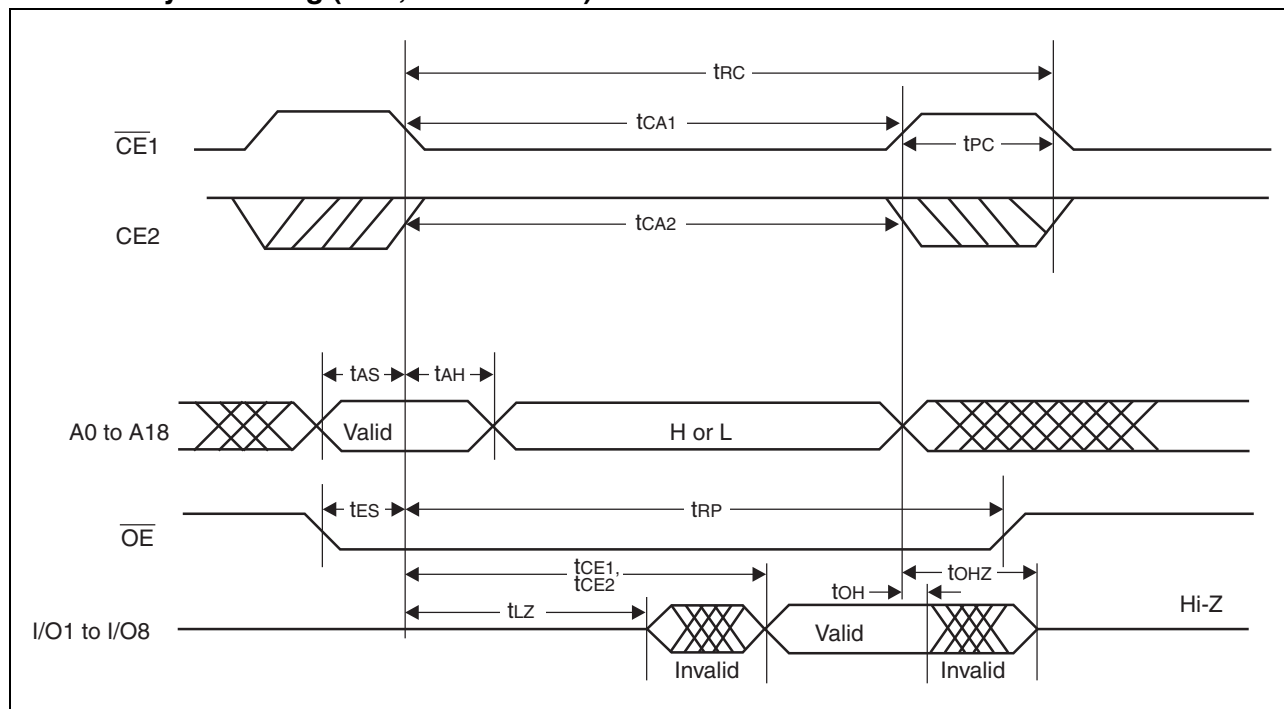
Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	$t_{WC}$	150	—	ns
$\overline{CE}1$ Active Time	$t_{CA1}$	120	—	ns
$\overline{CE}2$ Active Time	$t_{CA2}$	120	—	ns
Precharge Time	$t_{PC}$	20	—	ns
Address Setup Time	$t_{AS}$	0	—	ns
Address Hold Time	$t_{AH}$	50	—	ns
Write Pulse Width	$t_{WP}$	120	—	ns
Data Setup Time	$t_{DS}$	0	—	ns
Data Hold Time	$t_{DH}$	50	—	ns
Write Setup Time	$t_{WS}$	0	—	ns

### 3. Pin Capacitance

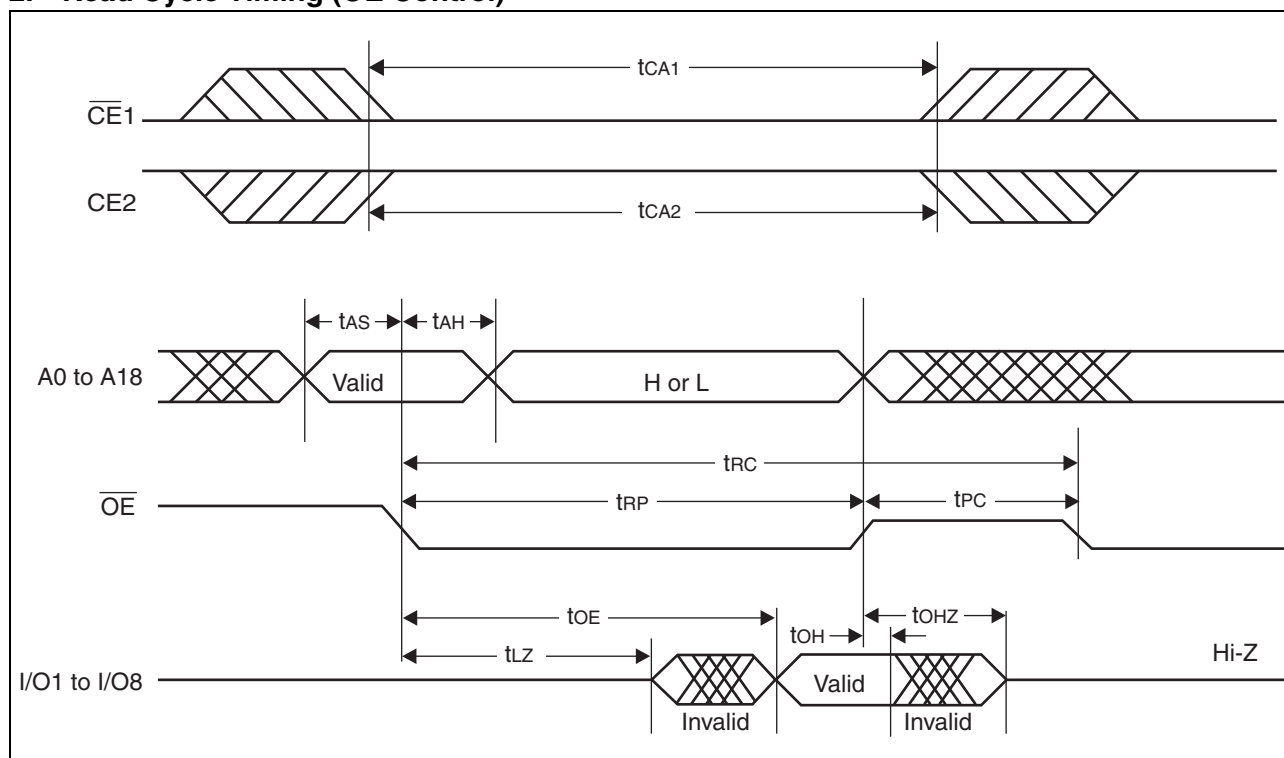
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	$C_{IN}$	$V_{IN} = V_{OUT} = 0\text{ V}$ , $f = 1\text{ MHz}$ , $T_A = +25\text{ °C}$	—	—	10	pF
Output Capacitance	$C_{OUT}$		—	—	10	pF
DNU Pin Input Capacitance	$C_{DNU}$		—	—	10	pF

## ■ TIMING DIAGRAMS

### 1. Read Cycle Timing ( $\overline{CE1}$ , CE2 Control)

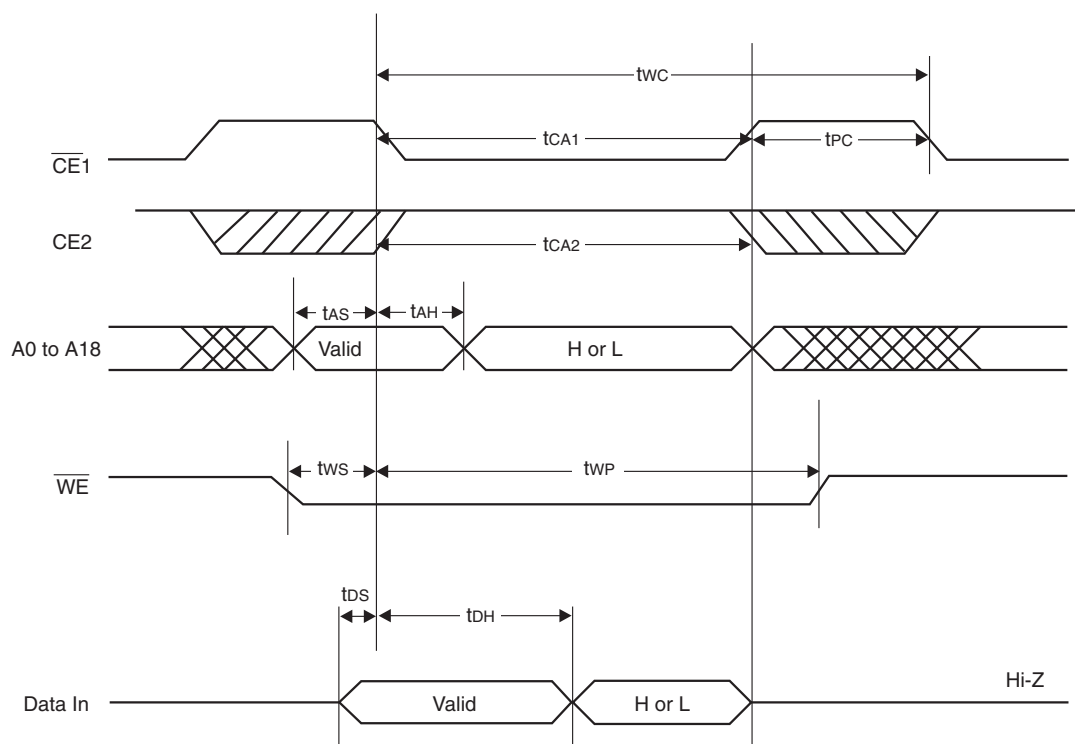


### 2. Read Cycle Timing ( $\overline{OE}$ Control)

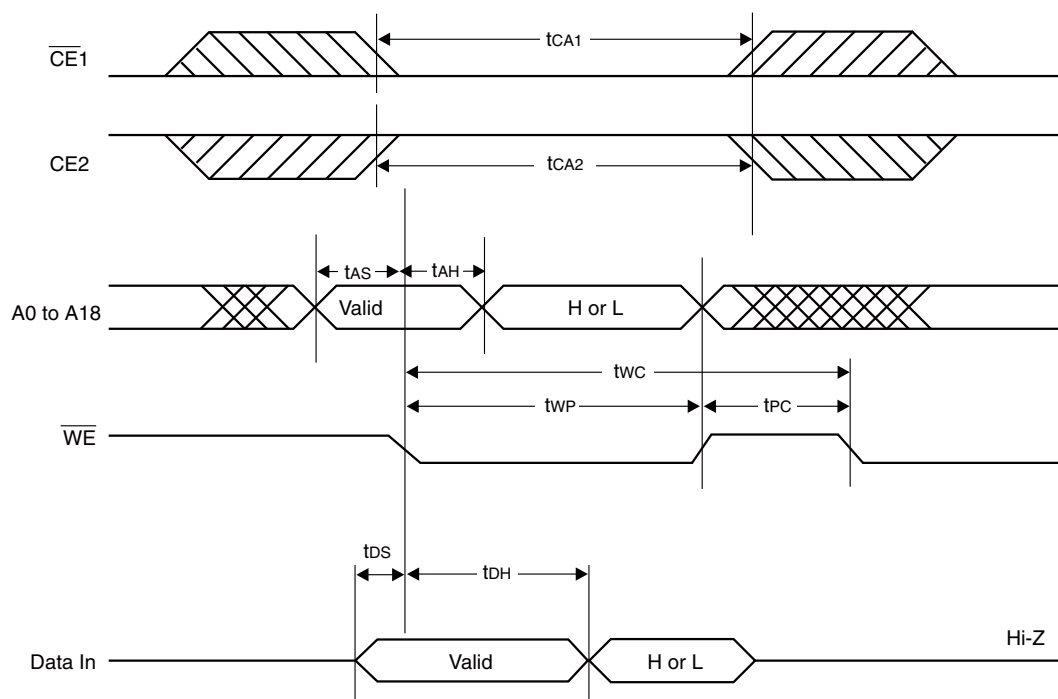




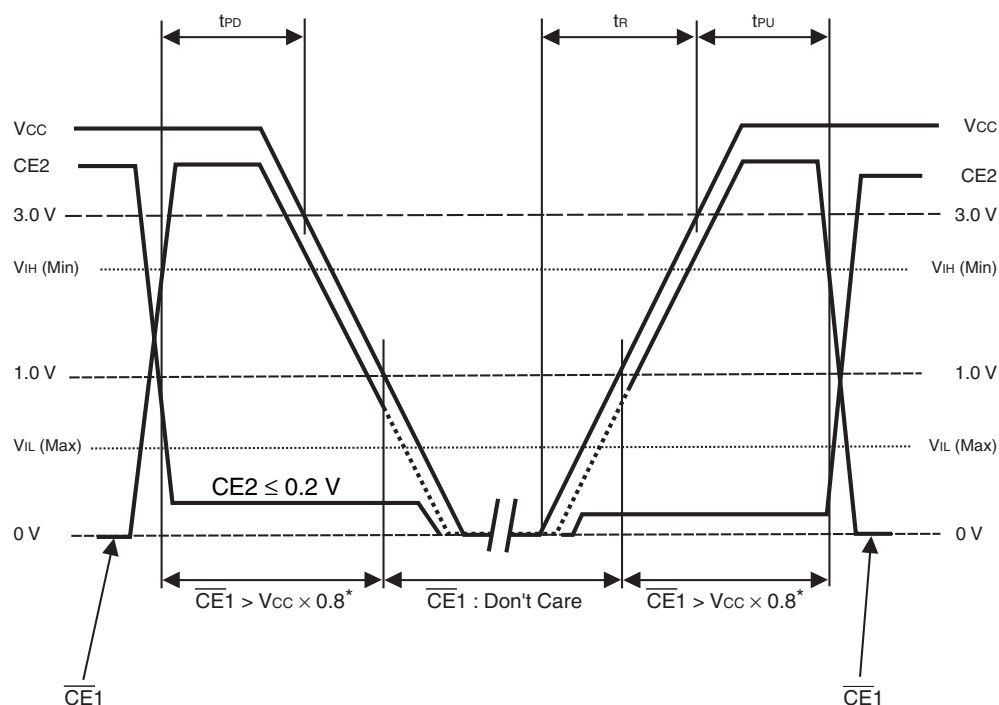
### 3. Write Cycle Timing ( $\overline{\text{CE1}}$ , CE2 Control)



### 4. Write Cycle Timing ( $\overline{\text{WE}}$ Control)



## ■ POWER ON/OFF SEQUENCE



\* :  $\overline{CE1}(\text{Max}) < V_{CC} + 0.5 \text{ V}$

Notes: • Use either of  $\overline{CE1}$  or  $CE2$ , or both for disable control of the device.

- Because turning the power-on from an intermediate level cause malfunction, when the power is turned on,  $V_{CC}$  is required to be started from 0 V.
- If the device does not operate within the specified conditions of read cycle, write cycle, power on/off sequence, memory data can not be guaranteed.
- When turning the power on or off, it is recommended that  $CE2$  is connected to ground to prevent unexpected writing.

(within recommended operating conditions)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CE1}$ level hold time for Power OFF	$t_{PD}$	85	—	—	ns
$\overline{CE1}$ level hold time for Power ON	$t_{PU}$	85	—	—	ns
Power supply rising time	$t_R$	0.05	—	200	ms

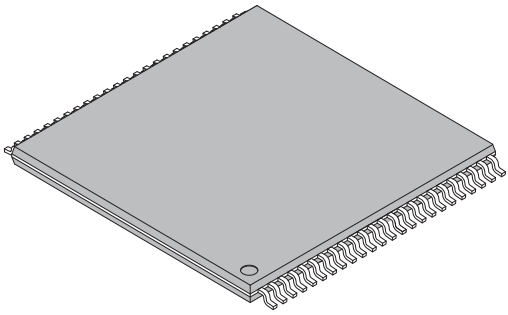
## ■ NOTES ON USE

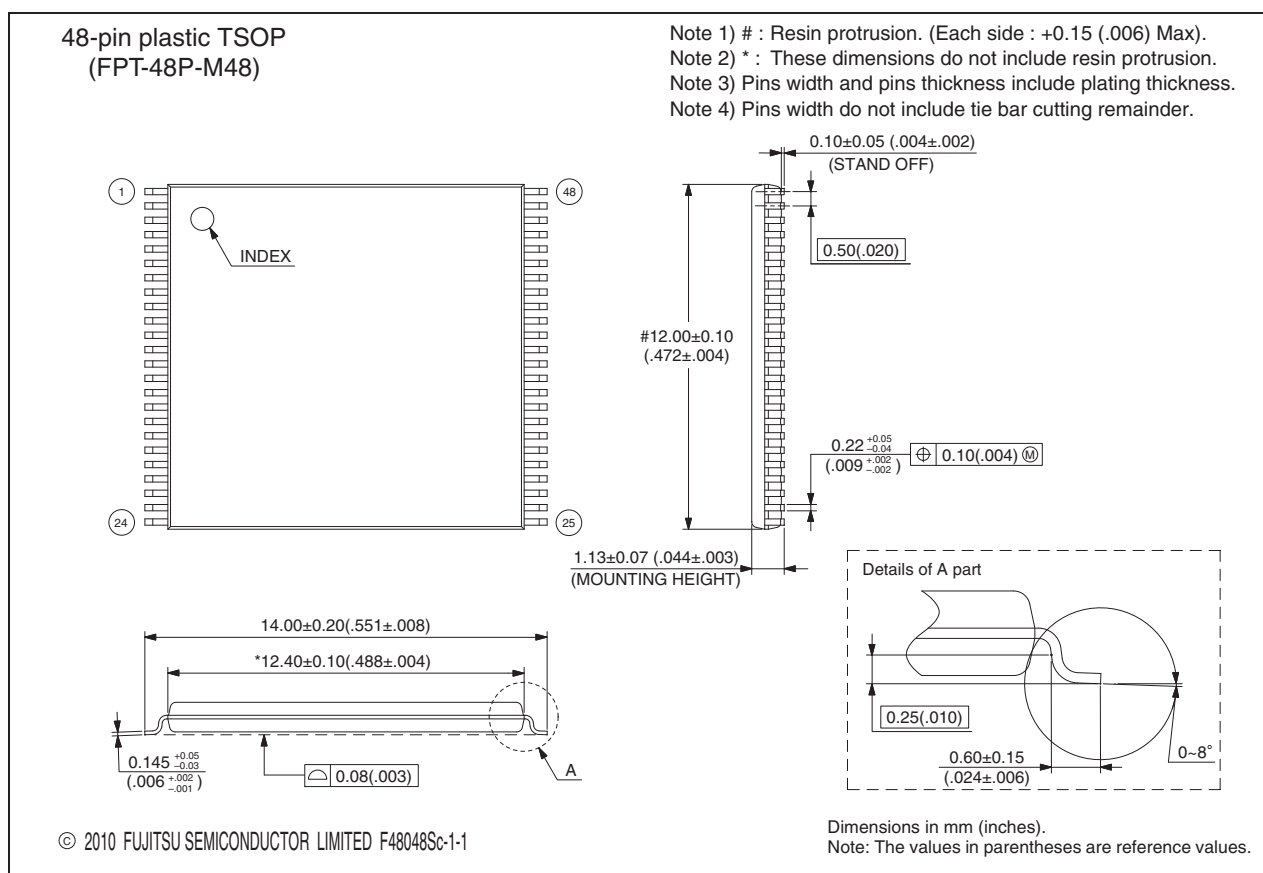
After the IR reflow completed, it is not guaranteed to hold the data written prior to the IR reflow.

## ■ ORDERING INFORMATION

Part Number	Package
MB85R4001ANC-GE1	48-pin plastic TSOP(1) (FPT-48P-M48)

## ■ PACKAGE DIMENSIONS

 <p>48-pin plastic TSOP</p> <p>(FPT-48P-M48)</p>	Lead pitch	0.50 mm
	Package width × package length	12.00 mm × 12.40 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.36 g



Please check the latest package dimension at the following URL.  
<http://edevic.fujitsu.com/package/en-search/>

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