320C3x, 320C4x, and 320MCM42x Power-Up Sensitivity at Cold Temperatures

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ABSTRACT

System board-level design and end-equipment environments can impact the operation of specific commercial and military 320C3x (320C30, 320C31, 320LC31, 320C32, and 320VC33), 320C4x (320C40 and 320C44) digital signal processors (DSPs), and the military 320MCM42x (320MCM42C and 320MCM42D) multichip modules (MCMs) during power up. The 320MCM42x MCM incorporates two 320C40 DSP die.

Specifically, the subject DSPs and MCMs may randomly exhibit application sensitivity during power up when exposed to temperatures near the lower end of the device recommended operating conditions (ROCs), as specified in the applicable device data sheets and DSCC standard microcircuit drawings (SMDs). Also, information covering the 320C4x design change and the 320VC33 circuit design, which addresses the application sensitivity, is included in this application report.

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1 320C3x/320C4x Architecture Overview

The 320C3x family of digital signal processors (DSPs) (320C30, 320C31, 320LC31, 320C32, and 320VC33) can perform parallel multiply and arithmetic logic unit (ALU) operations on integer or floating-point data in a single cycle. Each processor contains a general-purpose register file, a program cache, dedicated auxiliary register arithmetic units (ARLU), internal dual-access memories, one direct memory access (DMA) channel supporting concurrent input/output (I/O), and a short machine-cycle time. The 320C3x architecture supports a nonmaskable external reset signal that can be either synchronous or asynchronous with 320C3x internal clocks. The 320C3x architecture also supports four external maskable interrupt signals that are useful in a variety of applications.

The 320C4x family of DSPs (320C40 and 320C44) can perform single-cycle multiplications on 32-bit integer and 40-bit floating-point values. Use of parallel instructions allow multiply and ALU operations to occur in the same cycle. The ALU performs single-cycle operations on 32-bit integer, 32-bit logical, and 40-bit floating-point data, including single-cycle integer and floating-point conversions. Four internal buses carry two operands from memory and two operands from the register file, thus, allowing parallel multiplies and adds/subtracts on four integer or floating-point operands in a single cycle. The DMA coprocessor is a programmable, on-chip device that supports simultaneous memory transfer and CPU operation with minimal CPU overhead. Six DMA channels for memory-to-memory transfers are available in a unified mode, and a special split mode supports 12 DMA channels for communication-port to/from memory transfers. The 320C4x offers six (C40) or four (C44) on-chip communications ports for interfacing with other 320C4x DSPs and peripherals. Each communication port features a 160-Mbit/s, bidirectional peak data-transfer rate (at 40-ns cycle time). The military 320MCM42x contains two 320C40 known-good die.

2 Application Sensitivity and Background Information

All commercial and military 320C3x date-code and die revisions are subject to the application sensitivity. The circuit design of the 320VC33 and the design changes to the commercial 320C4x devices, with die revision 3.x or newer (C44) and die revision 7.x or newer (C40), address the application sensitivity. All military 320C40 devices and multichip modules (MCMs) are subject to the application sensitivity because, as of the publication date of this application report, TI Military Products Division has not released die revision 7.x, or newer, in the ceramic package. The 320C44 DSP is available only with commercial specifications.

The following example is based on customer communications. It addresses the type of sensitivity that might be experienced during power up and predominantly at cold-temperature ambient conditions.

> Random entry into IDLE2 mode of the 320Cxx (C3x or C4x) typically occurs during system-level operation and/or test when used with other on-board components and test-equipment fixtures specific to the board. The following paragraph describes the application sensitivity.
>
> When powered up at cold temperature, instead of going into the normal operating toggle mode, the output system clocks from the DSP (H1/H3) become frozen. The DSP output clocks exhibit a fixed H1 = high state and a fixed H3 = low state, verifying the device is in IDLE2 mode (described in greater detail in the following paragraphs). Asserting a DSP RESET does not force the device to function properly, i.e., the DSP output clocks (H1/H3) do not start to toggle. Asserting the interrupts after the 320C3x enters IDLE2 mode restores the processor to its active state, initiates toggle of the system output clocks (H1/H3), and returns the DSP function to normal. As well as being exhibited predominantly during power up after a system cold soak, this behavior also has been observed to occur randomly during power up at room-temperature ambient conditions.

3 IDLE2 Power-Down Mode

IDLE2 mode is a power-management mode designed to save power when the device is not required to be in its normal functioning state. It serves the same function as IDLE (idle until interrupt), with the exception that IDLE2 mode removes the functional clock input from the internal device. IDLE2 mode can be invoked by executing the proper opcode instructions. Table 1 defines the die revisions incorporating the IDLE2 opcode and the design change whereby the external RESET is asynchronously made available to the internal circuitry.

Table 1. Die Revision vs IDLE2 Opcode†

DSP	DIE REVISION						
	1.x	2.x	3.x	4.x	5.x	6.x	7.x
C30	–	–	–	–	–	–	x
C31	–	–	–	–	x	x	x
LC31	–	–	–	–	x	x	x
C32	x	x	–	–	–	–	–
VC33	xC	–	–	–	–	–	–
C40	–	–	–	–	x	x	xC
C44	–	x	xC	–	–	–	–

† "x" denotes the IDLE2 opcode implementation in the design and "C" denotes implementation of the exit IDLE2 on RESET capability. This table should not be interpreted as a line comparison between devices as to when the design revision was implemented.

In IDLE2 mode, the DSPs supporting this mode behave as follows:

- No instructions are executed.
- The CPU, peripherals, and internal memory retain their previous state.
- The external bus output pins are idle.
- The device remains in IDLE2 mode until one of the four external interrupts (INT3–INT0) is asserted *for at least one H1 cycle*. When one of the four interrupts is asserted for at least one H1 cycle, the H1/H3 clocks start after a delay of one H1 cycle. To avoid generating multiple false interrupts in level-triggered mode, the interrupt must be asserted for no more than two H1 cycles.
- When the device is in nonemulation mode, the internal clocking stops and H1 remains high while H3 remains low (see Figure 1). When the emulator is connected, the DSP detects the emulator and disables the IDLE2 opcode decode.

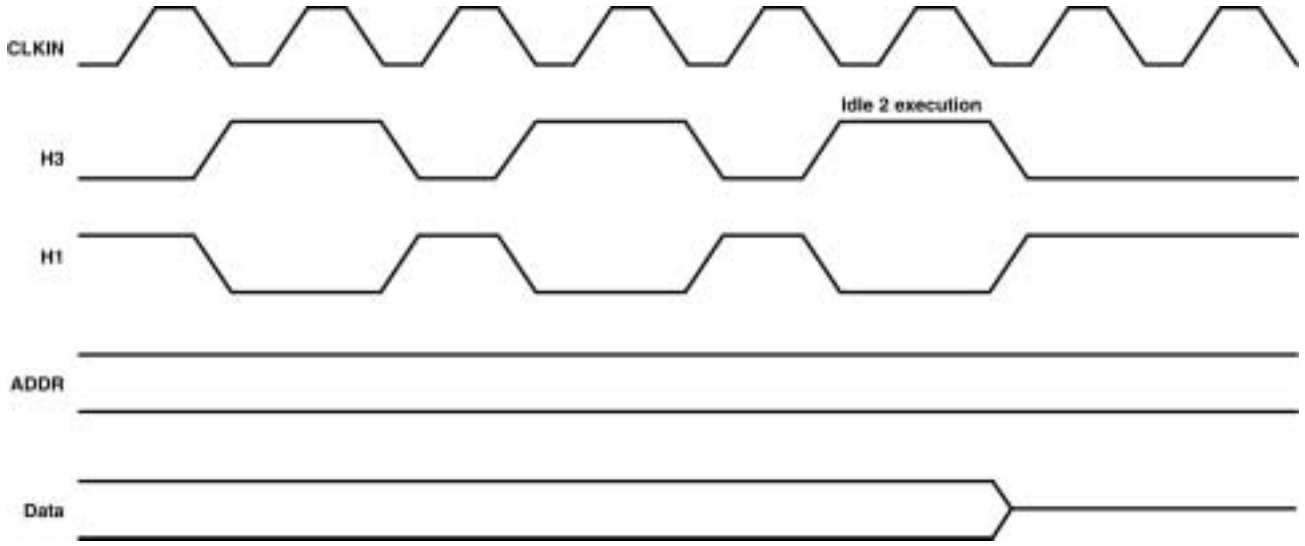

Figure 1. IDLE2 Timing

Figure 2 shows how the CPU randomly enters IDLE2 mode upon power up and the mechanism for waking up the CPU.

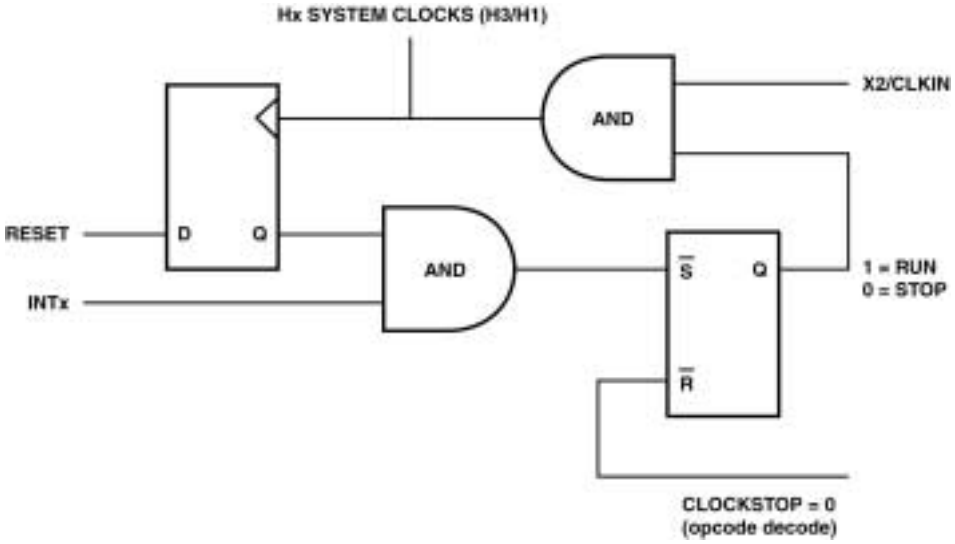

Figure 2. 320C3x IDLE2 Circuit Diagram

Normally, IDLE2 mode begins with the CPU asserting CLOCKSTOP = 0, causing the CPU clock to be halted because no clocks are applied to the core. The SET line of an S-R flip-flop has precedence, therefore, any INT0–INT3 pin in an active low state (asynchronous) causes the clock STOP line to go high, allowing the CPU clocks to pass. However, as shown in Figure 2, RESET does not affect operation of the circuit because the RESET signal must first pass through a clocked D-type flip-flop.

The input clock must be running throughout the process of placing the DSP in IDLE2 mode.

4 Random Entry Into IDLE2 Mode

Under certain board-level design and/or operating conditions, it is possible for a DSP device discussed in this application report to randomly or intermittently enter into an arbitrary (i.e., not invoked by opcode) IDLE2 mode upon power up. The internal DSP circuitry, along with external system-level operating conditions, can allow a random entry into IDLE2 mode. An analysis of the IDLE2 circuit diagram shows the S-R flip-flop is built as a feedback circuit using two NAND gates. The function table (see Table 2) shows that the circuit output can go either to a 0 state, a 1 state, or an indeterminate state, depending on the input signal conditions of the S-R flip-flop.

Table 2. S-R Flip-Flop Function Table

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	COMMENT
0	0	1	1	–
0	1	1	0	–
1	0	0	1	–
1	1	Q	$\overline{Q}$	(hold)

During power up, inputs to the S-R flip-flop are undefined because the external RESET comes through the D-type flip-flop, which is synchronized by the output clocks. Consequently, during power up, the exact state of the external RESET signal is not reflected at the inputs of the S-R flip-flop. Depending on the external operating conditions (e.g., temperature, power-supply ramp rate, etc.), the output of the D-type flip-flop during power up might be randomly indeterminate. These conditions can cause the subject DSP devices, i.e., those lacking the subsequent design implementation discussed in the following paragraphs, to randomly enter IDLE2 mode.

Cold temperatures influence functional behavior of internal circuitry during power up. However, the device can randomly enter IDLE2 mode after soaking at a warmer temperature (warmer than –55°C) if the ramp time of the power supply is slow (see the *Board-/System-Level Design Considerations* section).

The 320VC33 circuit design, along with specific die revisions of the 320C4x devices detailed previously, allow the external RESET pin to be asynchronously fed directly to the AND gate instead of through the D-type flip-flop as implemented in all the other 320C3x DSPs. This circuit design makes the state of the RESET signal directly available to the S-R flip-flop inputs during power up, thereby exiting the device's random entry into IDLE2 mode when RESET is applied during the documented power-up procedures (see Figure 3). The TMS320VC33 was the first device to implement this design feature, so it was never subject to the application sensitivity. The 320C30, 320C31, 320LC31, and 320C32 DSPs *do not incorporate* this design feature.

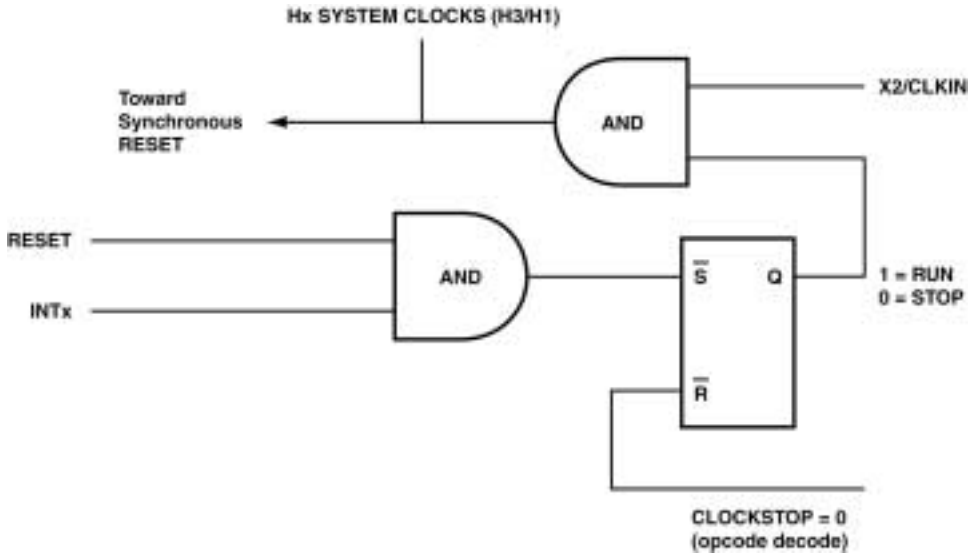

Figure 3. 320C4x IDLE2 Circuit Diagram (Design-Level Change)

For the C4x DSPs, only the commercial C4x DSPs with die revisions 7.x (320C40) and 3.x (320C44) have the design change that addresses the application sensitivity. Figure 4 shows an example of the commercial package symbolization that indicates the die revision. For the commercial 320C44 (not shown in Figure 4), the letters FB indicate die revision 3.x.

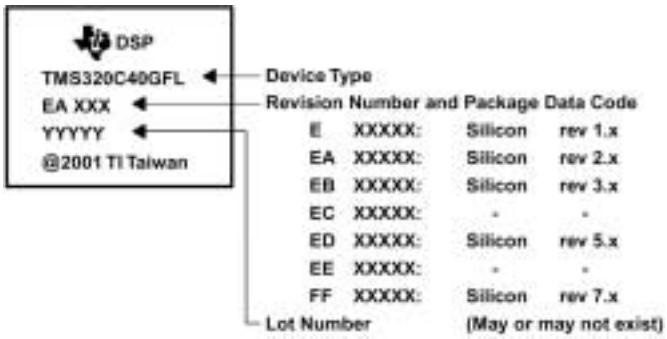

Figure 4. Commercial 320C4x DSPs Die-Revision Identification

5 Board-/System-Level Design Considerations

For customers wishing to avoid the potential for randomly entering IDLE2 mode during power up in cold-temperature operating conditions, several board-level design aspects can be considered. A combination of various operating conditions are involved. No single set of operating conditions can initiate random entry into IDLE2 mode. For example, a warmer soak temperature [warmer than the minimum specified in the recommended operating conditons (ROC)], combined with a more slowly rising power-supply ramp time, can cause a given device to enter IDLE2 mode. Conversely, a device cold soaked to a temperature near the low end of the ROC, but powered up with a fast-ramping power supply might rarely, if ever, enter IDLE2 mode.

There are indications that increasing the power-supply ramp rate, i.e., reducing the power-supply ramp time, can reduce the probability that the S-R flip-flop will enter an indeterminate/unknown state, especially at low temperature. It is important to note that power-supply ramp rate characteristics *should not* be used as a method to ensure that IDLE2 mode is not entered during power up. Also, power-supply noise can be a contributing factor. Thus, increasing the onboard power-supply bypass capacitance can reduce the power-supply noise and might reduce the likelihood of the subject device entering IDLE2 mode for a given board design. However, increasing bypass capacitance may increase the power-supply ramp time to the point of introducing a higher probability of the device entering IDLE2 mode. Engineering judgment is required to select the proper value of bypass capacitance.

Because pulling an interrupt low is the only way to bring a device out of IDLE2 mode, during power up an INTx flag can be forced low along with RESET and, thereafter, allowed to go high coincident with RESET without an interrupt flag being set. This serves two purposes:

- Accomplishes an internal device-level reset
- The device does not enter the unwanted IDLE2 mode during power up.

The following conditions define the timing constraints:

- Interrupt flags are cleared by RESET and are not to be set in the *first three cycles* of operation after RESET is deasserted. Unless otherwise specified, the term “cycle” refers to the output clock cycle (H1/H3).
- If an interrupt *is* to be used as a boot select, it should be held *low four or more cycles* after RESET is deasserted. If an interrupt *is not* to be used as a boot select, it may be deasserted immediately after the RESET signal is deasserted. There are no relative timing constraints.
- Level-triggered interrupts must be asserted for more than one H1 cycle to ensure exit from IDLE2 mode, and an interrupt should be asserted for *no more than two H1 cycles* to ensure the interrupt is recognized only one time and to avoid multiple false alarms in the level-triggered mode. This timing requirement is due primarily to the short interrupt response timing of the DMA, which can service and clear the INTx flag as soon as the third cycle. CPU interrupts are slower, plus the CPU can manually clear the flag within the interrupt service routine (ISR) thereby widening the maximum value to the width of the ISR (ISR clears the flag on the last instruction).

Figure 5 shows the interrupt-response timing after IDLE2 operations.

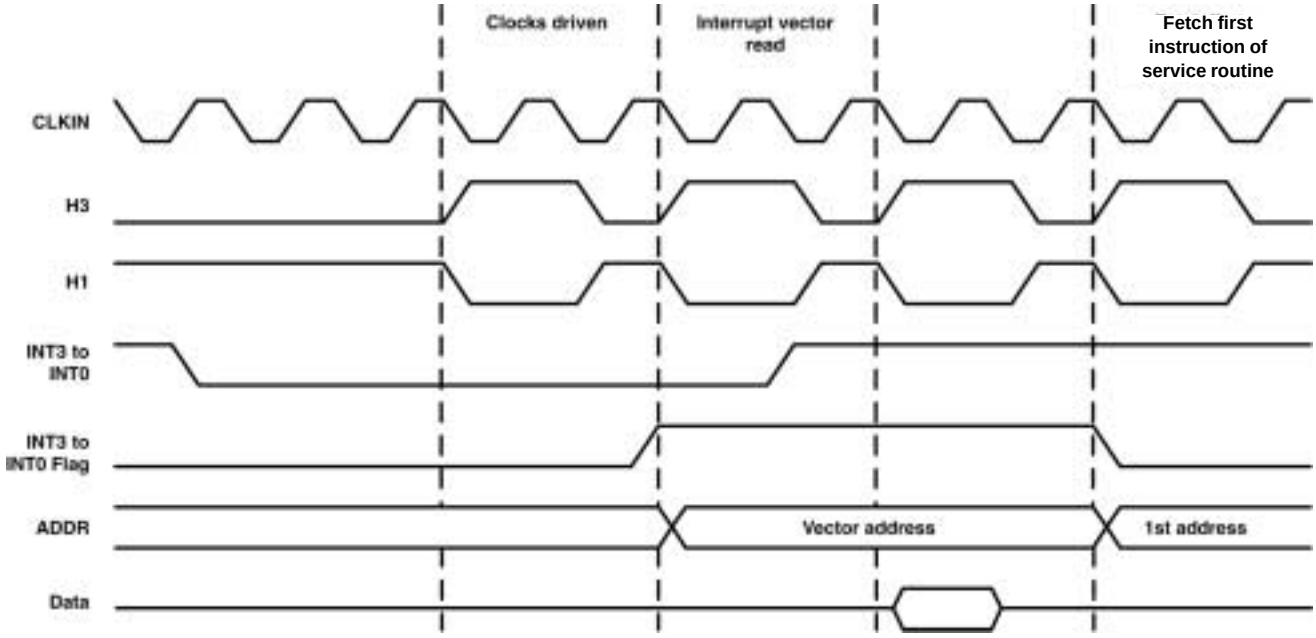

Figure 5. Interrupt-Response Timing After IDLE2 Operations

Figure 6 shows the timing response of INTx and RESET signals during power up to ensure device performance without entering IDLE2 mode.

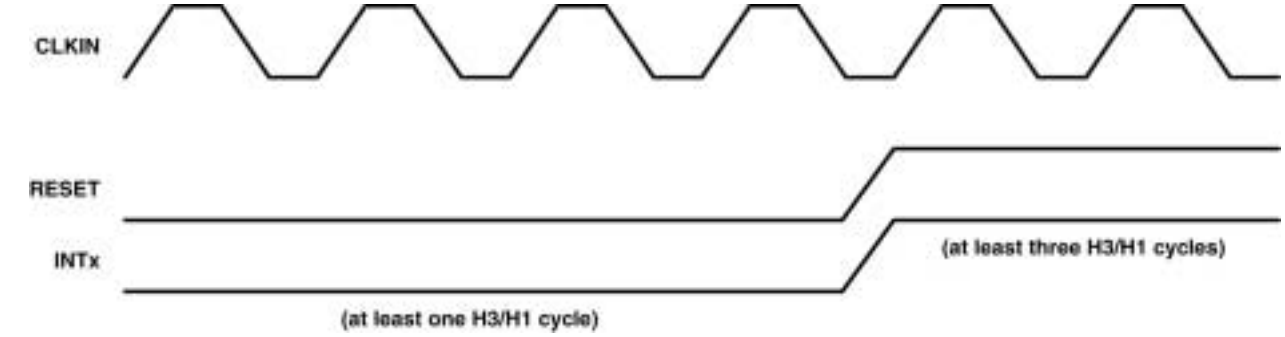

Figure 6. Timing for RESET and INTx During Power Up

6 Frequently Asked Questions (FAQs)

1. Is there any way to exit IDLE2 mode other than pulling an interrupt low?

A: In the present C30, C31, LC31, and C32 (not including the 320VC33) designs (also C40s with die revisions before 7.x and C44s with die revisions before 3.x) with IDLE2 circuitry, pulling an interrupt low is the only way to bring the subject DSP out of IDLE2 mode. This is because only the INTx inputs have the asynchronous access needed to start the H1/H3 system clock.

2. During power up, is it necessary for the RESET signal to be low (along with one of the interrupt signals) to ensure the device does not inadvertently enter IDLE2 mode?

A: It is sufficient for the devices with the design change to have RESET low during power up to avoid entering IDLE2 mode. However, devices with the design change do not include internal power-good detection circuitry, so it is still possible for these devices to power up in IDLE2 mode when no interrupt or reset pin is held logic low. Therefore, the board designer must apply one of these signals if the output clocks are to be used by some other logic in the system. For devices that do not have the design change, pulling one of the interrupts low (during power up) is sufficient to prevent the device from entering IDLE2 mode. If an interrupt is applied without RESET, the device can wake up and begin execution at whatever address and execution state the CPU is in (i.e., random).

3. Does TI have a design change scheduled for the C30, C31, LC31, and C32 IDLE2 circuitry?

A: Randomly entering IDLE2 mode during power up is an unlikely occurrence. Several factors of board design, operational environment, and power-supply characteristics must be present for the subject DSPs to randomly enter IDLE2 mode during power up. Once the DSPs successfully power up, entering IDLE2 mode is possible only under control of the program code. As discussed in this application report, a workaround exists for systems that randomly enter IDLE2 mode during power up. At this time, a schedule for a die design revision has not been set. The 320VC33 device incorporates the design change.

4. Is there a specific power-supply ramp rate that will keep the subject DSPs from entering IDLE2 mode during power up?

A: Statistically, entering IDLE2 mode during power up can occur for *any* power-supply ramp rate, especially under conditions pushing the ROC limits of temperature, supply voltage, and noise. TI has not accomplished the characterization of the power-supply ramp rate as to its effect on device function. Power-supply ramp rate characteristics should not be used as a method to ensure IDLE2 mode is not entered during power up.

5. How does the 320VC33 design compare with the other members of the 320C3x family?

A: The 320VC33 exits IDLE2 upon reset, otherwise it is logically equivalent to the 320C31.

6. Is the IDLE2 power-up susceptibility dependent on the die-manufacturing process used in the wafer fab?

A: Early die revisions of each subject device type where IDLE2 was implemented, but fabricated using an older CMOS process technique, are not as susceptible to randomly entering IDLE2 mode during power up.

7. Are there any other conditions that might cause the subject DSPs to enter IDLE2 mode?

A: Because the CPU is effectively executing random code in any memory space *until reset occurs*, a random opcode value equivalent to an IDLE2 also can cause the CPU to enter IDLE2 mode.

8. Does a cold temperature environment increase the probability of entering IDLE2 mode?

A: Randomly entering IDLE2 mode is observed predominantly after a cold soak (near minimum ROC), but the probability of entering IDLE2 mode is affected by a variety of system design parameters, e.g., power-supply ramp rates, noise, device-initialization sequence, etc. Randomly entering IDLE2 mode has occurred during power up at room-temperature conditions.

9. I execute an IDLE2 and the clocks do not stop as expected. What is causing this to occur?

A: When the emulator is connected, the DSP detects the emulator and disables the IDLE2 opcode decode. For the clocks to stop, the emulator must be disconnected. Inserting an IDLE2 in a system's acceptance code is one method of determining if the system is performing as expected. The *emulator must be disconnected* for this verification to work properly.

7 References

Commercial device information:

1. *TMS320C3x User's Guide* (SPRU031)
2. *TMS320C30 Digital Signal Processor* data sheet (SPRA032)
3. *TMS320C31, TMS320LC31 Digital Signal Processors* data sheet (SPRS035)
4. *TMS320C32 Digital Signal Processor* data sheet (SPRS027)
5. *TMS320VC33 Digital Signal Processor* data sheet (SPRS087)
6. *TMS320C4x User's Guide* (SPRU063)
7. *TMS320C40 Digital Signal Processor* data sheet (SPRS038)
8. *TMS320C44 Digital Signal Processor* data sheet (SPRS031)

Military device information:

9. *TMS320C3x User's Guide* (SPRU031)
10. *SMJ320C30 Digital Signal Processor* data sheet (SGUS014)
11. *SMJ320C31, SMJ320LC31, SMQ320LC31 Digital Signal Processors* data sheet (SGUS026)
12. *SMQ320C32 Digital Signal Processor* data sheet (SGUS027)
13. *SM320VC33, SMJ320VC33 Digital Signal Processors* data sheet (SGUS034)
14. *TMS320C4x User's Guide* (SPRU063)
15. *SMJ320C40, TMP320C40 Digital Signal Processors* data sheet (SGUS017)
16. *TMP320C40KGD, SMJ320C40KGD, TMP320C40KGDCT, SMJ320C40KGDCT Floating-Point Digital Signal Processors Known Good Dies* data sheet (SGUS024)

8 World Wide Web Resources

Texas Instruments: www.ti.com

TI DSP Knowledgebase: www-k.ext.ti.com/sc/technical-support/knowledgebase.htm

TI Military Semiconductors: www.ti.com/sc/docs/products/military/overview.htm

Military Semiconductors Errata Baseline: www.ti.com/sc/docs/products/military/errata/index.htm

TI Military Digital Signal Processors: www.ti.com/sc/docs/products/military/processr/index.htm

9 Revision History

January 11, 2002
Page 4, Table 1. Added ‘‘x” to C31/5.x cell.
Page 7, last sentence of paragraph. Clarified meaning of package data code.

May 2, 2002
Page 4, Table 1. Added ‘x” to LC31/5.x cell. Added dashes in blank cells.

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