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16/32

M32C/83 Group

Hardware Manual

RENESAS 16/32-BIT SINGLE-CHIP MICROCOMPUTER

M16C FAMILY / M32C/80 SERIES

Hardware Manual

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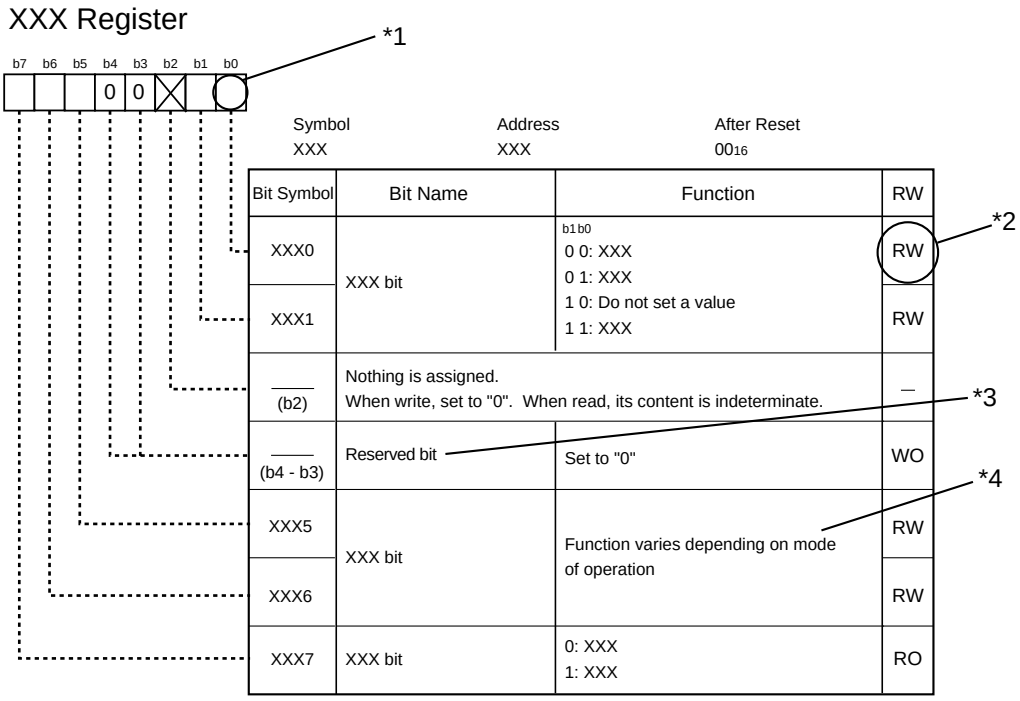
How to Use This Manual

1. Introduction

This hardware manual provides detailed information on the M32C/83 Group of microcomputers.
Users are expected to have basic knowledge of electric circuits, logical circuits and microcomputers.

2. Register Diagram

The symbols, and descriptions, used for bit function in each register are shown below.



*1

Blank: Set to "0" or "1" according to the application

0: Set to "0"

1: Set to "1"

X: Nothing is assigned

*2

RW: Read and write

RO: Read only

WO: Write only

–: Nothing is assigned

*3

• Reserved bit

Reserved bit. Set to specified value.

*4

• Nothing is assigned

Nothing is assigned to the bit concerned. As the bit may be use for future functions, set to "0" when writing to this bit.

• Do not set a value

The operation is not guaranteed when a value is set.

• Function varies depending on mode of operation

Bit function varies depending on peripheral function mode.
Refer to respective register for each mode.

3. M16C Family Documents

The following documents were prepared for the M16C family. (1)

Document	Contents
Short Sheet	Hardware overview
Data Sheet	Hardware overview and electrical characteristics
Hardware Manual	Hardware specifications (pin assignments, memory maps, peripheral specifications, electrical characteristics, timing charts)
Software Manual	Detailed description of assembly instructions and microcomputer performance of each instruction
Application Note	• Application examples of peripheral functions • Sample programs • Introduction to the basic functions in the M16C family • Programming method with Assembly and C languages
RENESAS TECHNICAL UPDATE	Preliminary report about the specification of a product, a document, etc.

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02F0₁₆		
02F1₁₆		
02F2₁₆		
02F3₁₆		
02F4₁₆	UART4 Special Mode Register 4 (U4SMR4)	181
02F5₁₆	UART4 Special Mode Register 3 (U4SMR3)	180
02F6₁₆	UART4 Special Mode Register 2 (U4SMR2)	179
02F7₁₆	UART4 Special Mode Register (U4SMR)	178
02F8₁₆	UART4 Transmit/Receive Mode Register (U4MR)	176
02F9₁₆	UART4 Baud Rate Register (U4BRG)	
02FA₁₆ 02FB₁₆	UART4 Transmit Buffer Register (U4TB)	175
02FC₁₆	UART4 Transmit/Receive Control Register 0 (U4C0)	177
02FD₁₆	UART4 Transmit/Receive Control Register 1 (U4C1)	178
02FE₁₆ 02FF₁₆	UART4 Receive Buffer Register (U4RB)	175
0300₁₆	Timer B3,B4,B5 Count Start Flag (TBSR)	155
0301₁₆		
0302₁₆ 0303₁₆	Timer A1-1 Register (TA11)	168
0304₁₆ 0305₁₆	Timer A2-1 Register (TA21)	
0306₁₆ 0307₁₆	Timer A4-1 Register (TA41)	
0308₁₆	Three-Phase PWM Control Register 0 (INVC0)	165
0309₁₆	Three-Phase PWM Control Register 1 (INVC1)	166
030A₁₆	Three-Phase Output Buffer Register 0 (IDB0)	167
030B₁₆	Three-Phase Output Buffer Register 1 (IDB1)	
030C₁₆	Dead Time Timer (DTT)	
030D₁₆	Timer B2 Interrupt Generation Frequency Set Counter (ICTB2)	168
030E₁₆		
030F₁₆		
0310₁₆ 0311₁₆	Timer B3 Register (TB3)	153
0312₁₆ 0313₁₆	Timer B4 Register (TB4)	
0314₁₆ 0315₁₆	Timer B5 Register (TB5)	
0316₁₆		
0317₁₆		
0318₁₆		
0319₁₆		
031A₁₆		
031B₁₆	Timer B3 Mode Register (TB3MR)	154
031C₁₆	Timer B4 Mode Register (TB4MR)	
031D₁₆	Timer B5 Mode Register (TB5MR)	
031E₁₆		
031F₁₆	External Interrupt Cause Select Register (IFSR)	106

Address	Register	Page
0320₁₆		
0321₁₆		
0322₁₆		
0323₁₆		
0324₁₆	UART3 Special Mode Register 4 (U3SMR4)	181
0325₁₆	UART3 Special Mode Register 3 (U3SMR3)	180
0326₁₆	UART3 Special Mode Register 2 (U3SMR2)	179
0327₁₆	UART3 Special Mode Register (U3SMR)	178
0328₁₆	UART3 Transmit/Receive Mode Register (U3MR)	176
0329₁₆	UART3 Baud Rate Register (U3BRG)	
032A₁₆ 032B₁₆	UART3 Transmit Buffer Register (U3TB)	175
032C₁₆	UART3 Transmit/Receive Control Register 0 (U3C0)	177
032D₁₆	UART3 Transmit/Receive Control Register 1 (U3C1)	178
032E₁₆ 032F₁₆	UART3 Receive Buffer Register (U3RB)	175
0330₁₆		
0331₁₆		
0332₁₆		
0333₁₆		
0334₁₆	UART2 Special Mode Register 4 (U2SMR4)	181
0335₁₆	UART2 Special Mode Register 3 (U2SMR3)	180
0336₁₆	UART2 Special Mode Register 2 (U2SMR2)	179
0337₁₆	UART2 Special Mode Register (U2SMR)	178
0338₁₆	UART2 Transmit/Receive Mode Register (U2MR)	176
0339₁₆	UART2 Baud Rate Register (U2BRG)	
033A₁₆ 033B₁₆	UART2 Transmit Buffer Register (U2TB)	175
033C₁₆	UART2 Transmit/Receive Control Register 0 (U2C0)	177
033D₁₆	UART2 Transmit/Receive Control Register 1 (U2C1)	178
033E₁₆ 033F₁₆	UART2 Receive Buffer Register (U2RB)	175
0340₁₆	Count Start Flag (TABSR)	138
0341₁₆	Clock Prescaler Reset Flag (CPSRF)	73
0342₁₆	One-Shot Start Flag (ONSF)	139
0343₁₆	Trigger Select Register (TRGSR)	140
0344₁₆	Up-Down Flag (UDF)	139
0345₁₆		
0346₁₆ 0347₁₆	Timer A0 Register (TA0)	137
0348₁₆ 0349₁₆	Timer A1 Register (TA1)	
034A₁₆ 034B₁₆	Timer A2 Register (TA2)	
034C₁₆ 034D₁₆	Timer A3 Register (TA3)	
034E₁₆ 034F₁₆	Timer A4 Register (TA4)	

Blank spaces are reserved. No access is allowed.

Quick Reference by Address

Address	Register	Page
0350$_{16}$ 0351$_{16}$	Timer B0 Register (TB0)	153
0352$_{16}$ 0353$_{16}$	Timer B1 Register (TB1)	
0354$_{16}$ 0355$_{16}$	Timer B2 Register (TB2)	
0356$_{16}$	Timer A0 Mode Register (TA0MR)	138
0357$_{16}$	Timer A1 Mode Register (TA1MR)	
0358$_{16}$	Timer A2 Mode Register (TA2MR)	
0359$_{16}$	Timer A3 Mode Register (TA3MR)	
035A$_{16}$	Timer A4 Mode Register (TA4MR)	
035B$_{16}$	Timer B0 Mode Register (TB0MR)	154
035C$_{16}$	Timer B1 Mode Register (TB1MR)	
035D$_{16}$	Timer B2 Mode Register (TB2MR)	
035E$_{16}$	Timer B2 Special Mode Register (TB2SC)	168
035F$_{16}$	Count Source Prescaler Register (TCSPR)	73
0360$_{16}$		
0361$_{16}$		
0362$_{16}$		
0363$_{16}$		
0364$_{16}$	UART0 Special Mode Register 4 (U0SMR4)	181
0365$_{16}$	UART0 Special Mode Register 3 (U0SMR3)	180
0366$_{16}$	UART0 Special Mode Register 2 (U0SMR2)	179
0367$_{16}$	UART0 Special Mode Register (U0SMR)	178
0368$_{16}$	UART0 Transmit/Receive Mode Register (U0MR)	176
0369$_{16}$	UART0 Baud Rate Register (U0BRG)	
036A$_{16}$ 036B$_{16}$	UART0 Transmit Buffer Register (U0TB)	175
036C$_{16}$	UART0 Transmit/Receive Control Register 0 (U0C0)	177
036D$_{16}$	UART0 Transmit/Receive Control Register 1 (U0C1)	178
036E$_{16}$ 036F$_{16}$	UART0 Receive Buffer Register (U0RB)	175
0370$_{16}$		
0371$_{16}$		
0372$_{16}$		
0373$_{16}$		
0374$_{16}$		
0375$_{16}$		
0376$_{16}$	PLL Control Register 0 (PLC0)	74
0377$_{16}$	PLL Control Register 1 (PLC1)	75
0378$_{16}$	DMA0 Cause Select Register (DM0SL)	117
0379$_{16}$	DMA1 Cause Select Register (DM1SL)	
037A$_{16}$	DMA2 Cause Select Register (DM2SL)	
037B$_{16}$	DMA3 Cause Select Register (DM3SL)	
037C$_{16}$ 037D$_{16}$	CRC Data Register (CRCD)	243
037E$_{16}$	CRC Input Register (CRCIN)	
037F$_{16}$		

Address	Register	Page
0380$_{16}$ 0381$_{16}$	A/D0 Register0 (AD00)	230
0382$_{16}$ 0383$_{16}$	A/D0 Register1 (AD01)	
0384$_{16}$ 0385$_{16}$	A/D0 Register2 (AD02)	
0386$_{16}$ 0387$_{16}$	A/D0 Register3 (AD03)	
0388$_{16}$ 0389$_{16}$	A/D0 Register4 (AD04)	
038A$_{16}$ 038B$_{16}$	A/D0 Register5 (AD05)	
038C$_{16}$ 038D$_{16}$	A/D0 Register6 (AD06)	
038E$_{16}$ 038F$_{16}$	A/D0 Register7 (AD07)	
0390$_{16}$		
0391$_{16}$		
0392$_{16}$		
0393$_{16}$		
0394$_{16}$	A/D0 Control Register 2 (AD0CON2)	230
0395$_{16}$		
0396$_{16}$	A/D0 Control Register 0 (AD0CON0)	228
0397$_{16}$	A/D0 Control Register 1 (AD0CON1)	229
0398$_{16}$	D/A Register 0 (DA0)	242
0399$_{16}$		
039A$_{16}$	D/A Register 1 (DA1)	242
039B$_{16}$		
039C$_{16}$	D/A Control Register (DACON)	242
039D$_{16}$		
039E$_{16}$		
039F$_{16}$		

Blank spaces are reserved. No access is allowed.

Quick Reference by Address

Address	Register	Page
03A0$_{16}$	Function Select Register A8 (PS8)	376
03A1$_{16}$	Function Select Register A9 (PS9)	377
03A2$_{16}$		
03A3$_{16}$		
03A4$_{16}$		
03A5$_{16}$		
03A6$_{16}$		
03A7$_{16}$		
03A8$_{16}$		
03A9$_{16}$		
03AA$_{16}$		
03AB$_{16}$		
03AC$_{16}$		
03AD$_{16}$		
03AE$_{16}$		
03AF$_{16}$	Function Select Register C (PSC)	380
03B0$_{16}$	Function Select Register A0 (PS0)	373
03B1$_{16}$	Function Select Register A1 (PS1)	
03B2$_{16}$	Function Select Register B0 (PSL0)	378
03B3$_{16}$	Function Select Register B1 (PSL1)	
03B4$_{16}$	Function Select Register A2 (PS2)	374
03B5$_{16}$	Function Select Register A3 (PS3)	
03B6$_{16}$	Function Select Register B2 (PSL2)	379
03B7$_{16}$	Function Select Register B3 (PSL3)	
03B8$_{16}$		
03B9$_{16}$	Function Select Register A5 (PS5)	375
03BA$_{16}$		
03BB$_{16}$		
03BC$_{16}$	Function Select Register A6 (PS6)	375
03BD$_{16}$	Function Select Register A7 (PS7)	376
03BE$_{16}$		
03BF$_{16}$		
03C0$_{16}$	Port P6 Register (P6)	372
03C1$_{16}$	Port P7 Register (P7)	
03C2$_{16}$	Port P6 Direction Register (PD6)	371
03C3$_{16}$	Port P7 Direction Register (PD7)	
03C4$_{16}$	Port P8 Register (P8)	372
03C5$_{16}$	Port P9 Register (P9)	
03C6$_{16}$	Port P8 Direction Register (PD8)	371
03C7$_{16}$	Port P9 Direction Register (PD9)	
03C8$_{16}$	Port P10 Register (P10)	372
03C9$_{16}$	Port P11 Register (P11)	
03CA$_{16}$	Port P10 Direction Register (PD10)	371
03CB$_{16}$	Port P11 Direction Register(PD11)	
03CC$_{16}$	Port P12 Register (P12)	372
03CD$_{16}$	Port P13 rRegister (P13)	
03CE$_{16}$	Port P12 Direction Register (PD12)	371
03CF$_{16}$	Port P13 Direction Register (PD13)	

Address	Register	Page
03D0$_{16}$	Port P14 Register (P14)	372
03D1$_{16}$	Port P15 Register (P15)	
03D2$_{16}$	Port P14 Direction Register (PD14)	371
03D3$_{16}$	Port P15 Direction Register (PD15)	
03D4$_{16}$		
03D5$_{16}$		
03D6$_{16}$		
03D7$_{16}$		
03D8$_{16}$		
03D9$_{16}$		
03DA$_{16}$	Pull-Up Control Register 2 (PUR2)	381
03DB$_{16}$	Pull-Up Control Register 3 (PUR3)	382
03DC$_{16}$	Pull-Up Control Register 4 (PUR4)	
03DD$_{16}$		
03DE$_{16}$		
03DF$_{16}$		
03E0$_{16}$	Port P14 Register (P0)	372
03E1$_{16}$	Port P14 Register (P1)	
03E2$_{16}$	Port P14 Direction Register (PD0)	371
03E3$_{16}$	Port P14 Direction Register (PD1)	
03E4$_{16}$	Port P14 Register (P2)	372
03E5$_{16}$	Port P14 Register (P3)	
03E6$_{16}$	Port P14 Direction Register (PD2)	371
03E7$_{16}$	Port P14 Direction Register (PD3)	
03E8$_{16}$	Port P14 Register (P4)	372
03E9$_{16}$	Port P14 Register (P5)	
03EA$_{16}$	Port P14 Direction Register (PD4)	371
03EB$_{16}$	Port P14 Direction Register (PD5)	
03EC$_{16}$		
03ED$_{16}$		
03EE$_{16}$		
03EF$_{16}$		
03F0$_{16}$	Pull-Up Control Register 0 (PUR0)	381
03F1$_{16}$	Pull-Up Control Register 1 (PUR1)	
03F2$_{16}$		
03F3$_{16}$		
03F4$_{16}$		
03F5$_{16}$		
03F6$_{16}$		
03F7$_{16}$		
03F8$_{16}$		
03F9$_{16}$		
03FA$_{16}$		
03FB$_{16}$		
03FC$_{16}$		
03FD$_{16}$		
03FE$_{16}$		
03FF$_{16}$	Port Control Register (PCR)	383

Blank spaces are reserved. No access is allowed.

1. Overview

The M32C/83 group microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/83 group is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It incorporates a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Outline

Tables 1.1 and 1.2 list performance outlines of the M32C/83 group.

Table 1.1 M32C/83 Group Performance (144-Pin Package)

Item		Performance
CPU	Basic Instructions	108 instructions
	Shortest Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, VCC=4.2 V to 5.5 V)(3) 50 ns (f(BCLK)=20 MHz, VCC=3.0 V to 5.5 V)
	Operation Mode	Single-chip mode, Memory expansion mode and Microprocessor mode
	Address Space	16 Mbytes
	Memory Capacity	See Table 1.3.
Peripheral Function	I/O Port	123 I/O pins and 1 input pin
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function: 16 bits x 12 channels Waveform generating function: 16 bits x 28 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus(1), 8-bit or 16-bit clock synchronous serial I/O)
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2)
	CAN Module	1 channel Supporting CAN 2.0B specification
	A/D Converter	10-bit A/D converter: 2 circuits, 34 channels
	D/A Converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions
	DRAMC	$\overline{CAS}$-before-$\overline{RAS}$ refresh, Self-refresh, EDO, FP
	CRC Calculation Circuit	CRC-CCITT
	XY Converter	16 bits x 16 bits
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock Generating Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally
	Oscillation Stop Detect Function	Main clock oscillation stop detect function
Electric Characteristics	Supply Voltage	4.2 V to 5.5 V (f(BCLK)=32 MHz) 3.0 V to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 V to 3.6 V (f(BCLK)=20 MHz, not through VDC)
	Power Consumption	41 mA (VCC=5 V, f(BCLK)=32 MHz) 38 mA (VCC=5 V, f(BCLK)=30 MHz) 26 mA (VCC=3.3 V, f(BCLK)=20 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 340 µA (VCC=3.3 V, f(XCIN)=32 kHz, through VDC in wait mode) 5.0 µA (VCC=3.3 V, f(XCIN)=32 kHz, not through VDC in wait mode) 0.4 µA (VCC=5 V, in stop mode) 0.4 µA (VCC=3.3 V, in stop mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V
	Program and Erase Endurance	100 cycles
Operating Ambient Temperature		–20 to 85°C, –40 to 85°C (optional)
Package		144-pin plastic molded LQFP

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. Contact Renesas Technology Sales Co., Ltd. when operating frequency exceeding 30MHz is required.

All options are on a request basis.

Table 1.2 M32C/83 Group Performance (100-Pin Package)

Item		Performance
CPU	Basic Instructions	108 instructions
	Shortest Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, VCC=4.2 V to 5.5 V)(3) 50 ns (f(BCLK)=20 MHz, VCC=3.0 V to 5.5 V)
	Operation Mode	Single-chip mode, Memory expansion mode and Microprocessor mode
	Address Space	16 Mbytes
	Memory Capacity	See Table 1.3
Peripheral Function	I/O Port	87 I/O pins and 1 input pin
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function: 16 bits x 5 channels Waveform generating function: 16 bits x 10 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus(1))
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2)
	CAN Module	1 channel Supporting CAN 2.0B specification
	A/D Converter	10-bit A/D converter: 2 circuits, 26 channels
	D/A Converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt factors Immediate transfer, Calculation transfer and Chain transfer functions
	DRAMC	$\overline{CAS}$-before-$\overline{RAS}$ refresh, Self-refresh, EDO, FP
	CRC Calculation Circuit	CRC-CCITT
	XY Converter	16 bits x 16 bits
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock Generating Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally
	Oscillation Stop Detect Function	Main clock oscillation stop detect function
Electric Characteristics	Supply Voltage	4.2 V to 5.5 V (f(BCLK)=32 MHz) 3.0 V to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 V to 3.6 V (f(BCLK)=20 MHz, not through VDC)
	Power Consumption	41 mA (VCC=5 V, f(BCLK)=32 MHz) 38 mA (VCC=5 V, f(BCLK)=30 MHz) 26 mA (VCC=3.3 V, f(BCLK)=20 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 340 µA (VCC=3.3 V, f(XCIN)=32 kHz, through VDC in wait mode) 5.0 µA (VCC=3.3 V, f(XCIN)=32 kHz, not through VDC in wait mode) 0.4 µA (VCC=5 V, f(XCIN)=32 kHz, in stop mode) 0.4 µA (VCC=3.3 V, f(XCIN)=32 kHz, in stop mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V
	Program and Erase Endurance	100 cycles
Operating Ambient Temperature		–20 to 85°C, –40 to 85°C (optional)
Package		100-pin plastic molded LQFP/QFP

NOTES:

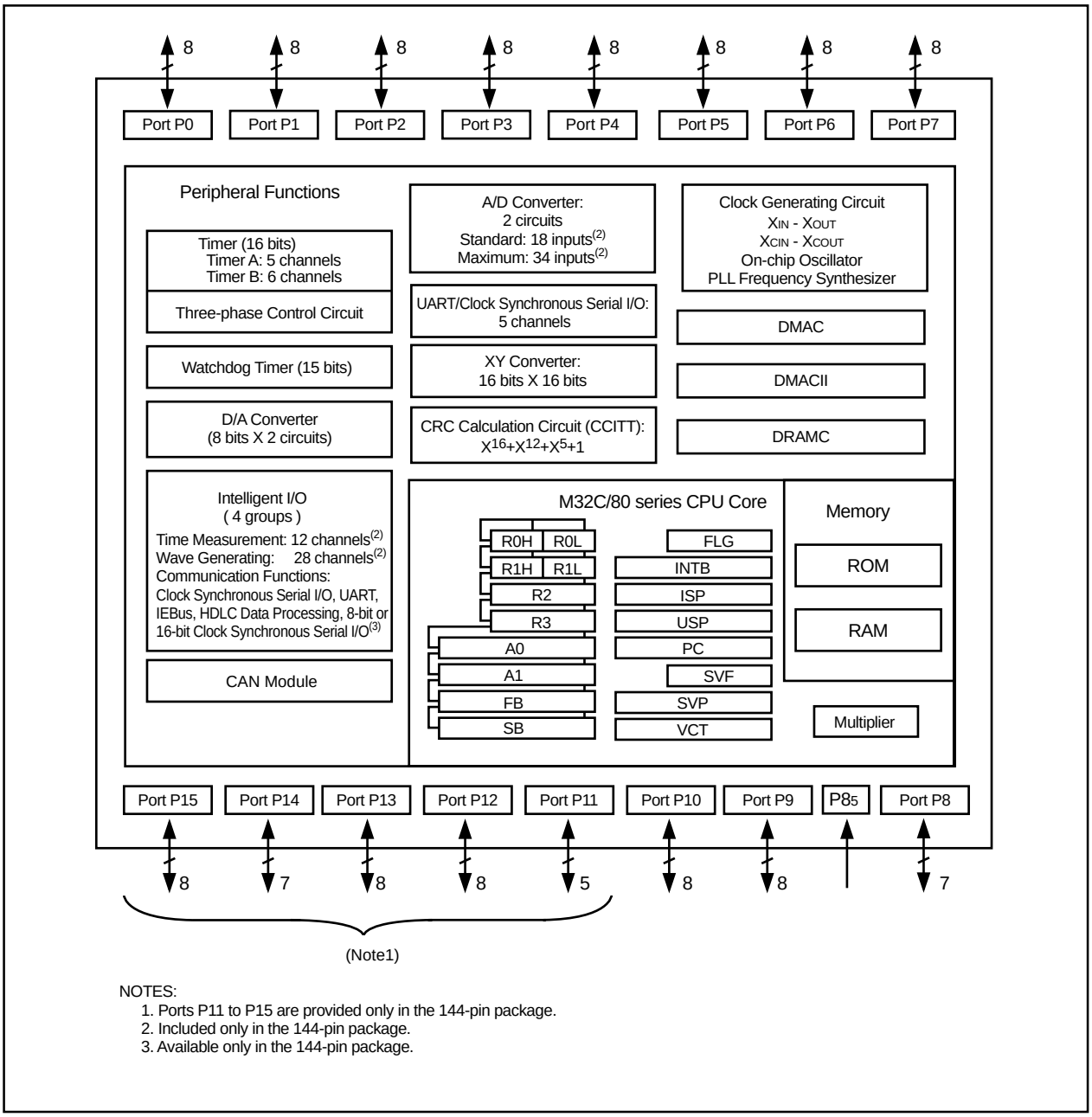
1. IEBus is a trademark of NEC Electronics Corporation.
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. Contact Renesas Technology Sales Co., Ltd. when operating frequency exceeding 30MHz is required.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/83 group microcomputer.

The M32C/83 group microcomputer contains ROM and RAM as memory to store instructions and data, CPU to execute calculations and peripheral functions such as interrupt, timer, serial I/O, DMAC, CRC calculation circuit, A/D converter, D/A converter, DRAMC, intelligent I/O and I/O ports.



NOTES:
1. Ports P11 to P15 are provided only in the 144-pin package.
2. Included only in the 144-pin package.
3. Available only in the 144-pin package.

Figure 1.1 M32C/83 Group Block Diagram

1.4 Product Information

Table 1.3 lists product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/83 Group

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks
M30835FJGP	512K	31K	144P6Q-A	Flash Memory
M30833FJGP			100P6Q-A	
M30833FJFP			100P6S-A	

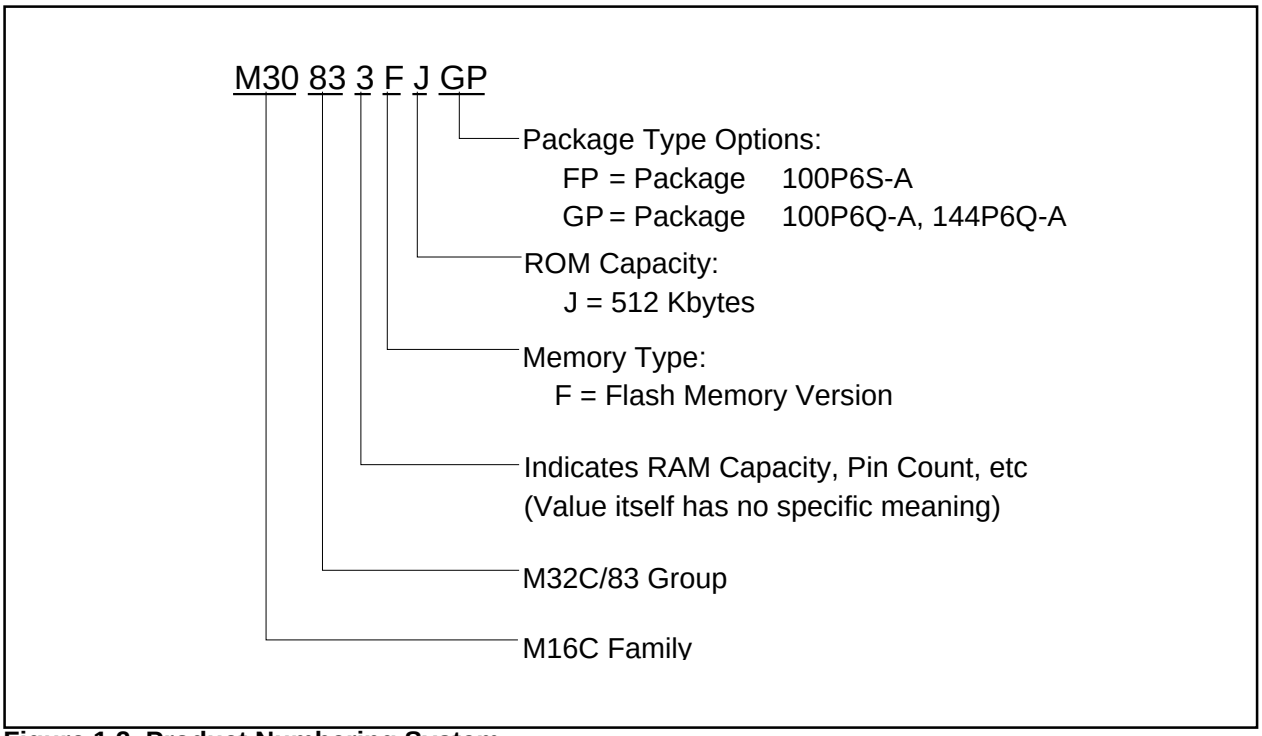


Figure 1.2 Product Numbering System

1.5 Pin Assignments

Figures 1.3 to 1.5 show pin assignments (top view).

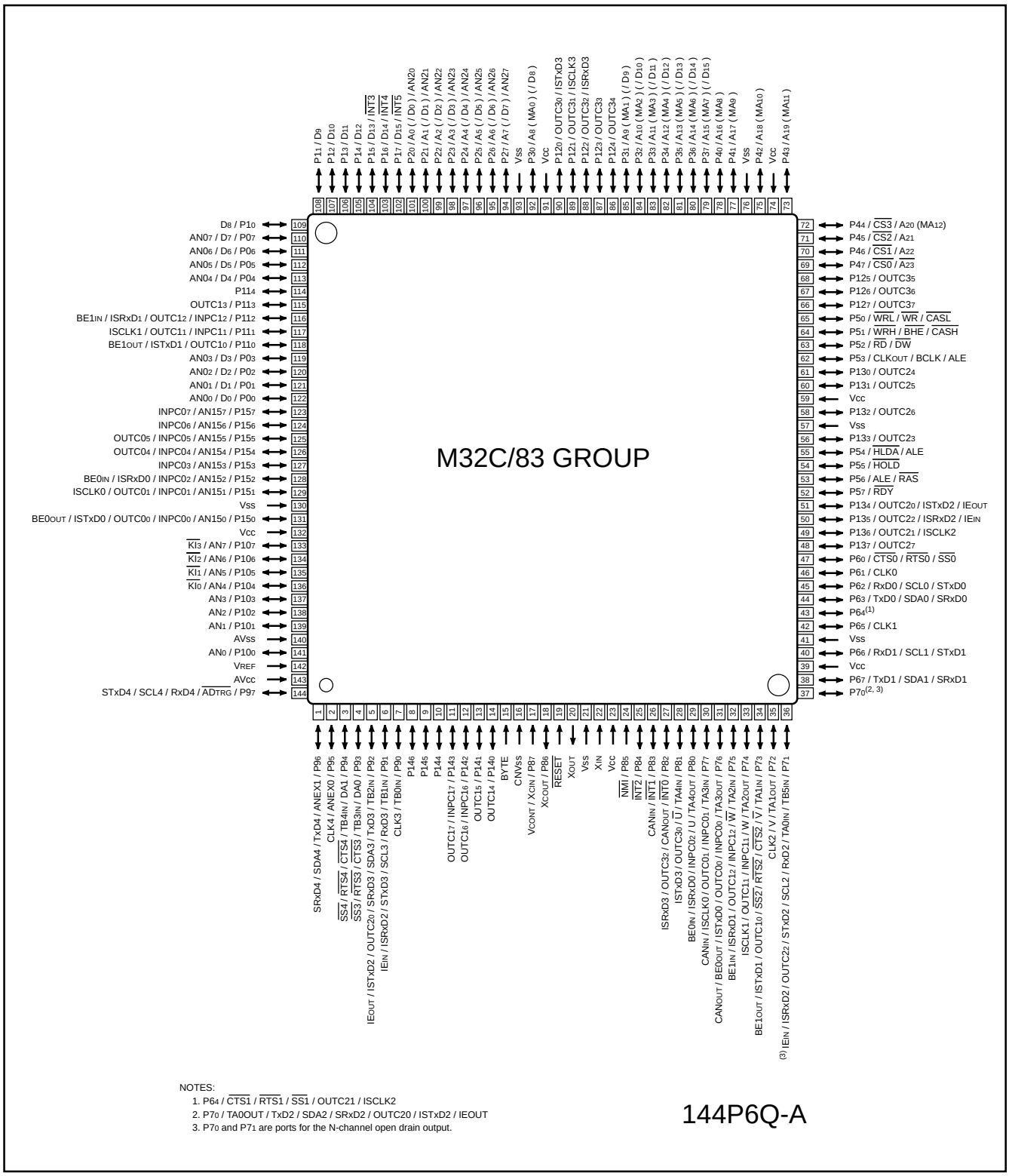


Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9$_6$			TxD4/SDA4/SRxD4		ANEX1	
2		P9$_5$			CLK4		ANEX0	
3		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3	OUTC2$_0$/IE$_{OUT}$/ISTxD2		
6		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3	IE$_{IN}$/ISRxD2		
7		P9$_0$		TB0$_{IN}$	CLK3			
8		P14$_6$						
9		P14$_5$						
10		P14$_4$						
11		P14$_3$				INPC1$_7$/OUTC1$_7$		
12		P14$_2$				INPC1$_6$/OUTC1$_6$		
13		P14$_1$				OUTC1$_5$		
14		P14$_0$				OUTC1$_4$		
15	BYTE							
16	CNV$_{SS}$							
17	X$_{CIN}$/V$_{CONT}$	P8$_7$						
18	X$_{COUT}$	P8$_6$						
19	$\overline{RESET}$							
20	X$_{OUT}$							
21	V$_{SS}$							
22	X$_{IN}$							
23	V$_{CC}$							
24		P8$_5$	$\overline{NMI}$					
25		P8$_4$	$\overline{INT2}$					
26		P8$_3$	$\overline{INT1}$		CAN$_{IN}$			
27		P8$_2$	$\overline{INT0}$		CAN$_{OUT}$	OUTC3$_2$/ISRxD3		
28		P8$_1$		TA4$_{IN}$/$\overline{U}$		OUTC3$_0$/ISTxD3		
29		P8$_0$		TA4$_{OUT}$/U		INPC0$_2$/ISRxD0/BE0$_{IN}$		
30		P7$_7$		TA3$_{IN}$	CAN$_{IN}$	INPC0$_1$/OUTC0$_1$/ISCLK0		
31		P7$_6$		TA3$_{OUT}$	CAN$_{OUT}$	INPC0$_0$/OUTC0$_0$/ISTxD0/BE0$_{OUT}$		
32		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
33		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1		
34		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
35		P7$_2$		TA1$_{OUT}$/V	CLK2			
36		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	OUTC2$_2$/ISRxD2/IE$_{IN}$		
37		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	OUTC2$_0$/ISTxD2/IE$_{OUT}$		
38		P6$_7$			TxD1/SDA1/SRxD1			
39	V$_{CC}$							
40		P6$_6$			RxD1/SCL1/STxD1			
41	V$_{SS}$							
42		P6$_5$			CLK1			
43		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$	OUTC2$_1$/ISCLK2		
44		P6$_3$			TxD0/SDA0/SRxD0			
45		P6$_2$			RxD0/SCL0/STxD0			
46		P6$_1$			CLK0			
47		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
48		P13$_7$				OUTC2$_7$		

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
49		P13$_6$				OUTC2$_1$/ISCLK2		
50		P13$_5$				OUTC2$_2$/ISRxD2/IE$_{IN}$		
51		P13$_4$				OUTC2$_0$/ISTxD2/IE$_{OUT}$		
52		P5$_7$						$\overline{RDY}$
53		P5$_6$						ALE/$\overline{RAS}$
54		P5$_5$						$\overline{HOLD}$
55		P5$_4$						$\overline{HLDA}$/ALE
56		P13$_3$				OUTC2$_3$		
57	V$_{SS}$							
58		P13$_2$				OUTC2$_6$		
59	V$_{CC}$							
60		P13$_1$				OUTC2$_5$		
61		P13$_0$				OUTC2$_4$		
62		P5$_3$						CLK$_{OUT}$/BCLK/ALE
63		P5$_2$						$\overline{RD}$/$\overline{DW}$
64		P5$_1$						$\overline{WRH}$/BHE/$\overline{CASH}$
65		P5$_0$						$\overline{WRL}$/$\overline{WR}$/$\overline{CASL}$
66		P12$_7$				OUTC3$_7$		
67		P12$_6$				OUTC3$_6$		
68		P12$_5$				OUTC3$_5$		
69		P4$_7$						$\overline{CS0}$/$\overline{A_{23}}$
70		P4$_6$						$\overline{CS1}$/A$_{22}$
71		P4$_5$						$\overline{CS2}$/A$_{21}$
72		P4$_4$						$\overline{CS3}$/A$_{20}$(MA$_{12}$)
73		P4$_3$						A$_{19}$(MA$_{11}$)
74	V$_{CC}$							
75		P4$_2$						A$_{18}$(MA$_{10}$)
76	V$_{SS}$							
77		P4$_1$						A$_{17}$(MA$_9$)
78		P4$_0$						A$_{16}$(MA$_8$)
79		P3$_7$						A$_{15}$(MA$_7$)(/D$_{15}$)
80		P3$_6$						A$_{14}$(MA$_6$)(/D$_{14}$)
81		P3$_5$						A$_{13}$(MA$_5$)(/D$_{13}$)
82		P3$_4$						A$_{12}$(MA$_4$)(/D$_{12}$)
83		P3$_3$						A$_{11}$(MA$_3$)(/D$_{11}$)
84		P3$_2$						A$_{10}$(MA$_2$)(/D$_{10}$)
85		P3$_1$						A$_9$(MA$_1$)(/D$_9$)
86		P12$_4$				OUTC3$_4$		
87		P12$_3$				OUTC3$_3$		
88		P12$_2$				OUTC3$_2$/ISRxD3		
89		P12$_1$				OUTC3$_1$/ISCLK3		
90		P12$_0$				OUTC3$_0$/ISTxD3		
91	V$_{CC}$							
92		P3$_0$						A$_8$(MA$_0$)(/D$_8$)
93	V$_{SS}$							
94		P2$_7$					AN2$_7$	A$_7$(/D$_7$)
95		P2$_6$					AN2$_6$	A$_6$(/D$_6$)
96		P2$_5$					AN2$_5$	A$_5$(/D$_5$)

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
97		$P2_4$					$AN2_4$	A_4(/D_4)
98		$P2_3$					$AN2_3$	A_3(/D_3)
99		$P2_2$					$AN2_2$	A_2(/D_2)
100		$P2_1$					$AN2_1$	A_1(/D_1)
101		$P2_0$					$AN2_0$	A_0(/D_0)
102		$P1_7$	$\overline{INT5}$					D_{15}
103		$P1_6$	$\overline{INT4}$					D_{14}
104		$P1_5$	$\overline{INT3}$					D_{13}
105		$P1_4$						D_{12}
106		$P1_3$						D_{11}
107		$P1_2$						D_{10}
108		$P1_1$						D_9
109		$P1_0$						D_8
110		$P0_7$					$AN0_7$	D_7
111		$P0_6$					$AN0_6$	D_6
112		$P0_5$					$AN0_5$	D_5
113		$P0_4$					$AN0_4$	D_4
114		$P11_4$						
115		$P11_3$				$OUTC1_3$		
116		$P11_2$				$INPC1_2$/$OUTC1_2$/ISRxD1/$BE1_{IN}$		
117		$P11_1$				$INPC1_1$/$OUTC1_1$/ISCLK1		
118		$P11_0$				$OUTC1_0$/ISTxD1/$BE1_{OUT}$		
119		$P0_3$					$AN0_3$	D_3
120		$P0_2$					$AN0_2$	D_2
121		$P0_1$					$AN0_1$	D_1
122		$P0_0$					$AN0_0$	D_0
123		$P15_7$				$INPC0_7$	$AN15_7$	
124		$P15_6$				$INPC0_6$	$AN15_6$	
125		$P15_5$				$INPC0_5$/$OUTC0_5$	$AN15_5$	
126		$P15_4$				$INPC0_4$/$OUTC0_4$	$AN15_4$	
127		$P15_3$				$INPC0_3$	$AN15_3$	
128		$P15_2$				$INPC0_2$/ISRxD0/$BE0_{IN}$	$AN15_2$	
129		$P15_1$				$INPC0_1$/$OUTC0_1$/ISCLK0	$AN15_1$	
130	V_{SS}							
131		$P15_0$				$INPC0_0$/$OUTC0_0$/ISTxD0/$BE0_{OUT}$	$AN15_0$	
132	V_{CC}							
133		$P10_7$	$\overline{KI_3}$				AN_7	
134		$P10_6$	$\overline{KI_2}$				AN_6	
135		$P10_5$	$\overline{KI_1}$				AN_5	
136		$P10_4$	$\overline{KI_0}$				AN_4	
137		$P10_3$					AN_3	
138		$P10_2$					AN_2	
139		$P10_1$					AN_1	
140	AV_{SS}							
141		$P10_0$					AN_0	
142	V_{REF}							
143	AV_{CC}							
144		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

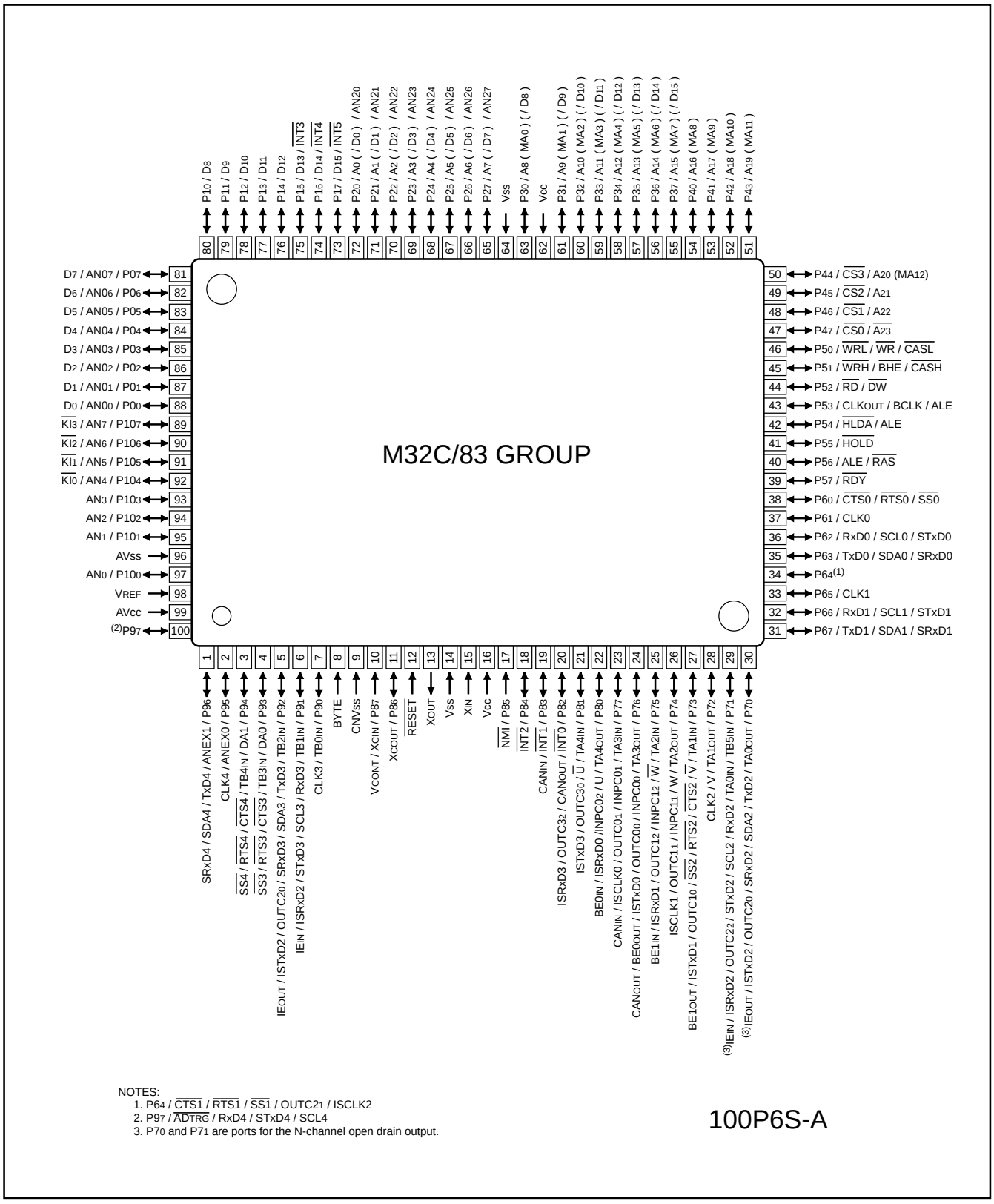


Figure 1.4 Pin Assignment for 100-Pin Package

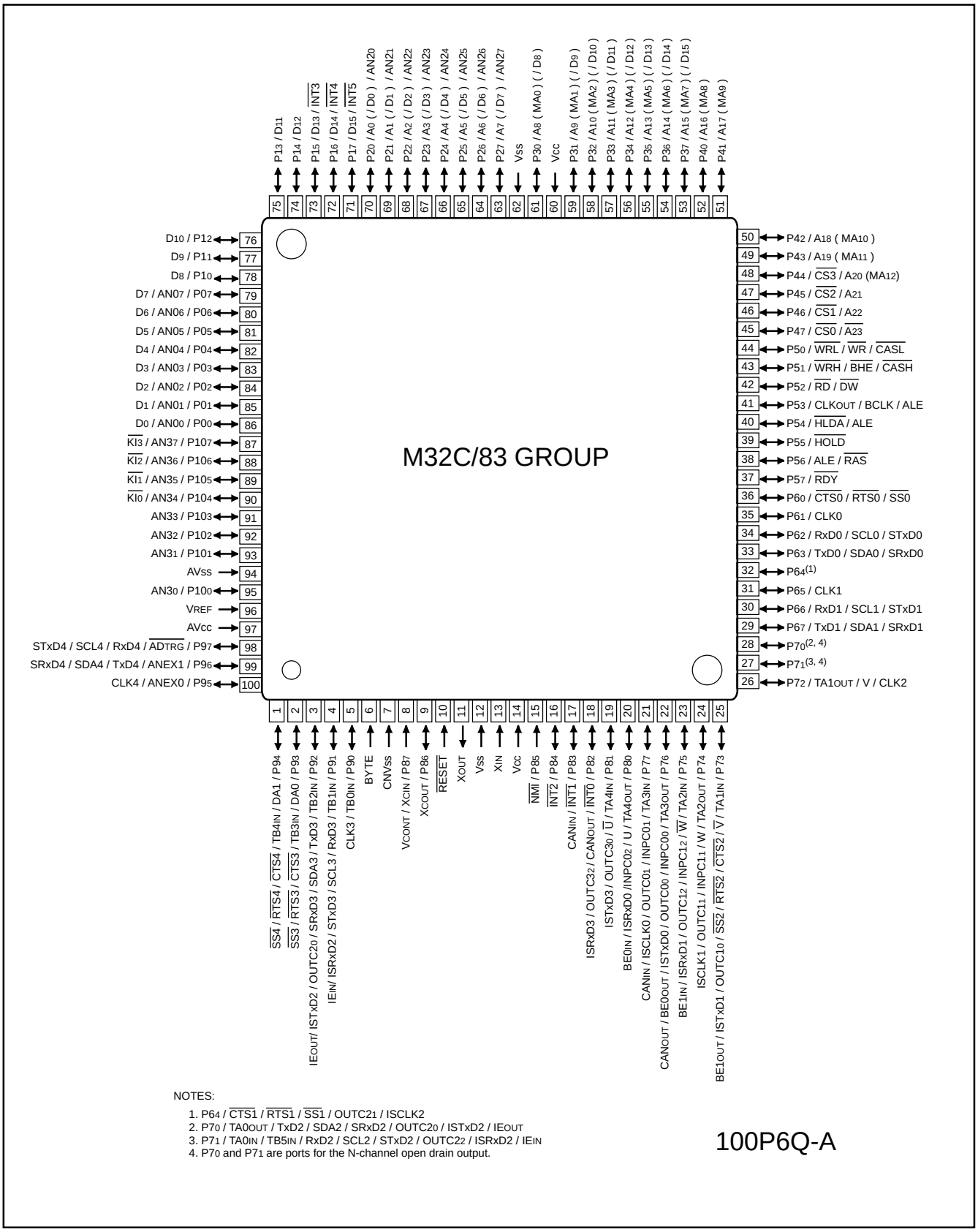


Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
1	99		P9$_6$			TxD4/SDA4/SRxD4		ANEX1	
2	100		P9$_5$			CLK4		ANEX0	
3	1		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4	2		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5	3		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3	OUTC2$_0$/IE$_{OUT}$/ISTxD2		
6	4		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3	IE$_{IN}$/ISRxD2		
7	5		P9$_0$		TB0$_{IN}$	CLK3			
8	6	BYTE							
9	7	CNV$_{SS}$							
10	8	X$_{CIN}$/V$_{CONT}$	P8$_7$						
11	9	X$_{COUT}$	P8$_6$						
12	10	$\overline{RESET}$							
13	11	X$_{OUT}$							
14	12	V$_{SS}$							
15	13	X$_{IN}$							
16	14	V$_{CC}$							
17	15		P8$_5$	$\overline{NMI}$					
18	16		P8$_4$	$\overline{INT2}$					
19	17		P8$_3$	$\overline{INT1}$		CAN$_{IN}$			
20	18		P8$_2$	$\overline{INT0}$		CAN$_{OUT}$	OUTC3$_2$/ISRxD3		
21	19		P8$_1$		TA4$_{IN}$/$\overline{U}$		OUTC3$_0$/ISTxD3		
22	20		P8$_0$		TA4$_{OUT}$/U		INPC0$_2$/ISRxD0/BE0$_{IN}$		
23	21		P7$_7$		TA3$_{IN}$	CAN$_{IN}$	INPC0$_1$/OUTC0$_1$/ISCLK0		
24	22		P7$_6$		TA3$_{OUT}$	CAN$_{OUT}$	INPC0$_0$/OUTC0$_0$/ISTxD0/BE0$_{OUT}$		
25	23		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
26	24		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1		
27	25		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
28	26		P7$_2$		TA1$_{OUT}$/V	CLK2			
29	27		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	OUTC2$_2$/ISRxD2/IE$_{IN}$		
30	28		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	OUTC2$_0$/ISTxD2/IE$_{OUT}$		
31	29		P6$_7$			TxD1/SDA1/SRxD1			
32	30		P6$_6$			RxD1/SCL1/STxD1			
33	31		P6$_5$			CLK1			
34	32		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$	OUTC2$_1$/ISCLK2		
35	33		P6$_3$			TxD0/SDA0/SRxD0			
36	34		P6$_2$			RxD0/SCL0/STxD0			
37	35		P6$_1$			CLK0			
38	36		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
39	37		P5$_7$						$\overline{RDY}$
40	38		P5$_6$						ALE/$\overline{RAS}$
41	39		P5$_5$						$\overline{HOLD}$
42	40		P5$_4$						$\overline{HLDA}$/ALE
43	41		P5$_3$						CLK$_{OUT}$/BCLK/ALE
44	42		P5$_2$						$\overline{RD}$/$\overline{DW}$
45	43		P5$_1$						$\overline{WRH}$/$\overline{BHE}$/$\overline{CASH}$
46	44		P5$_0$						$\overline{WRL}$/$\overline{WR}$/$\overline{CASL}$
47	45		P4$_7$						$\overline{CS0}$/A$_{23}$
48	46		P4$_6$						$\overline{CS1}$/A$_{22}$
49	47		P4$_5$						$\overline{CS2}$/A$_{21}$
50	48		P4$_4$						$\overline{CS3}$/A$_{20}$(MA$_{12}$)

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
51	49		$P4_3$						$A_{19}(MA_{11})$
52	50		$P4_2$						$A_{18}(MA_{10})$
53	51		$P4_1$						$A_{17}(MA_9)$
54	52		$P4_0$						$A_{16}(MA_8)$
55	53		$P3_7$						$A_{15}(MA_7)(/D_{15})$
56	54		$P3_6$						$A_{14}(MA_6)(/D_{14})$
57	55		$P3_5$						$A_{13}(MA_5)(/D_{13})$
58	56		$P3_4$						$A_{12}(MA_4)(/D_{12})$
59	57		$P3_3$						$A_{11}(MA_3)(/D_{11})$
60	58		$P3_2$						$A_{10}(MA_2)(/D_{10})$
61	59		$P3_1$						$A_9(MA_1)(/D_9)$
62	60	V_{CC}							
63	61		$P3_0$						$A_8(MA_0)(/D_8)$
64	62	V_{SS}							
65	63		$P2_7$					$AN2_7$	$A_7(/D_7)$
66	64		$P2_6$					$AN2_6$	$A_6(/D_6)$
67	65		$P2_5$					$AN2_5$	$A_5(/D_5)$
68	66		$P2_4$					$AN2_4$	$A_4(/D_4)$
69	67		$P2_3$					$AN2_3$	$A_3(/D_3)$
70	68		$P2_2$					$AN2_2$	$A_2(/D_2)$
71	69		$P2_1$					$AN2_1$	$A_1(/D_1)$
72	70		$P2_0$					$AN2_0$	$A_0(/D_0)$
73	71		$P1_7$	$\overline{INT5}$					D_{15}
74	72		$P1_6$	$\overline{INT4}$					D_{14}
75	73		$P1_5$	$\overline{INT3}$					D_{13}
76	74		$P1_4$						D_{12}
77	75		$P1_3$						D_{11}
78	76		$P1_2$						D_{10}
79	77		$P1_1$						D_9
80	78		$P1_0$						D_8
81	79		$P0_7$					$AN0_7$	D_7
82	80		$P0_6$					$AN0_6$	D_6
83	81		$P0_5$					$AN0_5$	D_5
84	82		$P0_4$					$AN0_4$	D_4
85	83		$P0_3$					$AN0_3$	D_3
86	84		$P0_2$					$AN0_2$	D_2
87	85		$P0_1$					$AN0_1$	D_1
88	86		$P0_0$					$AN0_0$	D_0
89	87		$P10_7$	$\overline{KI_3}$				AN_7	
90	88		$P10_6$	$\overline{KI_2}$				AN_6	
91	89		$P10_5$	$\overline{KI_1}$				AN_5	
92	90		$P10_4$	$\overline{KI_0}$				AN_4	
93	91		$P10_3$					AN_3	
94	92		$P10_2$					AN_2	
95	93		$P10_1$					AN_1	
96	94	AV_{SS}							
97	95		$P10_0$					AN_0	
98	96	V_{REF}							
99	97	AV_{CC}							
100	98		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Symbol	Function	I/O Type	Description
V_{CC} V_{SS}	Power Supply Input	I I	Apply 3.0 to 5.5 V to the V_{CC} pins. Apply 0 V to the V_{SS} pin.
CNV_{SS}	CNV_{SS}	I	Switches processor mode. Connect this pin to V_{SS} to start up in single-chip mode (memory expansion mode). Connect this pin to V_{CC} to start up in microprocessor mode.
$\overline{RESET}$	Reset Input	I	The microcomputer is in a reset state when "L" is applied to the $\overline{RESET}$ pin.
X_{IN} X_{OUT}	Clock Input Clock Output	I O	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between X_{IN} and X_{OUT}. To use an external clock, apply the clock to X_{IN} and leave X_{OUT} open.
BYTE	Input to Switch External Data Bus Width	I	Switches the data bus in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when the BYTE pin is held "H". Set to either. Connect this pin to V_{SS} when an external bus is not being used.
AV_{CC}	Analog Power Supply Input	I	Supplies power to the A/D converter and D/A converter. Connect this pin to V_{CC}.
AV_{SS}	Analog Power Supply Input	I	Supplies power to the A/D converter and D/A converter. Connect this pin to V_{SS}.
V_{REF}	Reference Voltage Input	I	Supplies reference voltage to the A/D converter.
$P0_0$ to $P0_7$	I/O Port P0	I/O	8-bit I/O ports in CMOS individually programmed to input or output under the control of the direction register. An input port in single-chip mode can be set, by program, for a pull-up or for no pull-up in 4-bit units. When these pins are used as bus control pins in memory expansion mode and microprocessor mode, internal pull-up resistor cannot be selected. Ports used as input ports can be set for a pull-up or for no pull-up in the modes above.
D_0 to D_7	Data Bus	I/O	Inputs and outputs data (D_0 to D_7) when these pins are set as the separate bus.
$AN0_0$ to $AN0_7$	Analog Input Pin	I	Analog input pins for the A/D converter
$P1_0$ to $P1_7$	I/O Port P1	I/O	8-bit I/O ports having functions equivalent to P0
$\overline{INT3}$ to $\overline{INT5}$	$\overline{INT}$ Interrupt Input Pin	I	Input pins for the $\overline{INT}$ interrupt
D_8 to D_{15}	Data Bus	I/O	Inputs and outputs data (D_8 to D_{15}) when these pins are set as the separate bus.
$P2_0$ to $P2_7$	I/O Port P2	I/O	8-bit I/O ports having functions equivalent to P0
A_0 to A_7	Address Bus	O	Outputs 8 low-order address bits (A_0 to A_7).
A_0/D_0 to A_7/D_7	Address Bus/Data Bus	I/O	Inputs and outputs data (D_0 to D_7) and outputs 8 low-order address bits (A_0 to A_7) by timesharing when these pins are set as the multiplexed bus.
$AN2_0$ to $AN2_7$	Analog Input Pin	I	Analog input pins for A/D converter
$P3_0$ to $P3_7$	I/O Port P3	I/O	8-bit I/O ports having functions equivalent to P0
A_8 to A_{15}	Address Bus	O	Outputs 8 middle-order address bits (A_8 to A_{15}).
A_8/D_8 to A_{15}/D_{15}	Address Bus/Data Bus	I/O	Inputs and outputs data (D_8 to D_{15}) and outputs 8 middle-order address bits (A_8 to A_{15}) by timesharing when external 16-bit data bus is set as the multi-plexed bus.
MA_0 to MA_7	Address Bus	O	Outputs row addresses and column addresses by timesharing when accessing the DRAM area.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
$P4_0$ to $P4_7$	I/O Port P4	I/O	8-bit I/O ports having functions equivalent to P0
$A16$ to $A22$, $\overline{A23}$	Address Bus	O O	Outputs 8 high-order address bits ($A16$ to $A22$, $\overline{A23}$). The inversed highest-order bit ($\overline{A23}$) is also output.
$\overline{CS0}$ to $\overline{CS3}$	Chip-Select	O	Outputs $\overline{CS0}$ to $\overline{CS3}$ signals. $\overline{CS0}$ to $\overline{CS3}$ are chip-select signals specifying an external space.
$MA8$ to $MA12$	Address Bus	O	Outputs row addresses and column addresses by timesharing when accessing the DRAM area.
$P5_0$ to $P5_7$	I/O Port P5	I/O	8-bit I/O ports having functions equivalent to P0
CLKOUT	Clock Output	O	Outputs XIN divided by 8 or divided by 32 or the clock having the same frequency as XCIN from $P5_3$.
$\overline{WRL}$ $\overline{WR}$ $\overline{WRH}$ $\overline{BHE}$ $\overline{RD}$ BCLK $\overline{HLDA}$ $\overline{HOLD}$ ALE $\overline{RDY}$	Bus Control Pin	O O O O O O O I O I	Outputs $\overline{WRL}$, $\overline{WRH}$, ($\overline{WR}$, $\overline{BHE}$), $\overline{RD}$, BCLK, $\overline{HLDA}$ and ALE signals. $\overline{WRL}$ and $\overline{WRH}$ or $\overline{BHE}$ and $\overline{WR}$ can be switched by program. ■ $\overline{WRL}$, $\overline{WRH}$ and $\overline{RD}$ are selected The $\overline{WRL}$ signal becomes "L" when data is written to an even address in an external memory space. The $\overline{WRH}$ signal becomes "L" when data is written to an odd address in an external memory space. The $\overline{RD}$ pin signal becomes "L" when data in an external memory space is read. ■ $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ are selected The $\overline{WR}$ signal becomes "L" when data is written to an external memory space. The $\overline{RD}$ signal becomes "L" when data in an external memory space is read. The $\overline{BHE}$ signal becomes "L" when an odd address is accessed. Select $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ for an external 8-bit data bus. The microcomputer is placed in a hold state while the $\overline{HOLD}$ pin is held "L". $\overline{HLDA}$ outputs a "L" signal in a hold state. ALE is a signal latching the address. The microcomputer is placed in a wait state while the $\overline{RDY}$ pin is held "L".
$\overline{DW}$ $\overline{CASL}$ $\overline{CASH}$ $\overline{RAS}$	DRAM Bus Control Pin	O O O O	The $\overline{DW}$ signal becomes "L" when data is written to the DRAM area. $\overline{CASL}$ and $\overline{CASH}$ are signals indicating the timing to latch column addresses. The $\overline{CASL}$ signal becomes "L" when an even address is accessed. The $\overline{CASH}$ signal becomes "L" when an odd address is accessed. $\overline{RAS}$ is a signal latching row addresses.
$P6_0$ to $P6_7$	I/O Port P6	I/O	8-bit I/O ports having functions equivalent to P0
$\overline{CTS0}$, $\overline{CTS1}$ $\overline{RTS0}$, $\overline{RTS1}$ $\overline{SS0}$, $\overline{SS1}$ CLK0, CLK1 RxD0, RxD1 SCL0, SCL1 STxD0, STxD1 TxD0, TxD1 SDA0, SDA1 SRxD0, SRxD1	UART Pin	I O I I/O I I/O O O I/O I	I/O pins for UART0 ($P6_0$ to $P6_3$) and UART1 ($P6_4$ to $P6_7$)
ISCLK2 $OUTC2_1$	Intelligent I/O Pin	I/O O	ISCKL2 inputs and outputs the clock for the intelligent I/O communication function. $OUTC2_1$ outputs the clock for the waveform generating function.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
$P7_0$ to $P7_7$	I/O Port P7	I/O	8-bit I/O ports having functions equivalent to P0 ($P7_0$ and $P7_1$ are ports for the N-channel open drain output.)
$TA0_{OUT}$ to $TA3_{OUT}$	Timer A Pin	I/O	I/O pins for timer A0 to A3
$TA0_{IN}$ to $TA3_{IN}$		I	
$TB5_{IN}$	Timer B Pin	I	Input pin for timer B5
V, $\overline{V}$	Three-Phase Motor	O	V-phase output pin
W, $\overline{W}$	Control Output Pin	O	W-phase output pin
$\overline{CTS2}$	UART Pin	I	I/O pins for UART2
$\overline{RTS2}$		O	
$\overline{SS2}$		I	
CLK2		I/O	
RxD2		I	
SCL2		I/O	
STxD2		O	
TxD2		O	
SDA2		I/O	
SRxD2		I	
$INPC0_0$, $INPC0_1$	Intelligent I/O Pin	I	$INPC0_0$, $INPC0_1$, $INPC1_1$ and $INPC1_2$ are input pins for the time measurement function.
$INPC1_1$, $INPC1_2$			
$OUTC0_0$, $OUTC0_1$		O	$OUTC0_0$, $OUTC0_1$, $OUTC1_0$ to $OUTC1_2$, $OUTC2_0$ and $OUTC2_2$ are output pins for the waveform generating function.
$OUTC1_0$ to $OUTC1_2$			
$OUTC2_0$, $OUTC2_2$			ISCLK0 and ISCLK1 input and output the clock for the intelligent I/O communication function.
ISCLK0, ISCLK1		I/O	
ISTxD0 to ISTxD2		O	ISRxD1, ISRxD2, $BE1_{IN}$ and IE_{IN} input received data for the intelligent I/O communication function.
ISRxD1, ISRxD2		I	
IE_{OUT}		O	ISTxD0 to ISTxD2, IE_{OUT}, $BE0_{OUT}$ and $BE1_{OUT}$ output transmit data for the intelligent I/O communication function.
IE_{IN}		I	
$BE0_{OUT}$		O	
$BE1_{OUT}$		O	
$BE1_{IN}$		I	
$CAN0_{OUT}$	CAN Pin	O	I/O pins for the CAN communication function
$CAN0_{IN}$		I	

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
P80 to P84, P86, P87	I/O Port P8	I/O	I/O ports having functions equivalent to P0
XCIN XCOUT	Sub Clock	I O	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
VCONT	Low-Pass Filter Connect Pin for PLL Frequency Synthesizer Pin		Connects the low-pass filter to the VCONT pin when using the PLL frequency synthesizer. Connect P86 to VSS to stabilize the PLL frequency.
TA4OUT TA4IN	Timer A Pin	I/O I	I/O pins for timer A4
U, $\overline{U}$	Three-phase Motor Control Output Pin	O	U-phase output pins
$\overline{INT0}$ to $\overline{INT2}$	$\overline{INT}$ Interrupt Input Pin	I	Input pins for the $\overline{INT}$ interrupt
INPC02 ISRxD0 BE0IN OUTC30 ISTxD3 OUTC32 ISRxD3	Intelligent I/O Pin	I I I O O O I	INPC02 is an input pin for the time measurement function. OUTC30 and OUTC32 are output pins for the waveform generating function. ISRxD0 and BE0IN input received data for the intelligent I/O communication function. ISTxD3 outputs transmit data for the intelligent I/O communication function. ISRxD3 inputs received data for the intelligent I/O communication function.
CANOUT CANIN	CAN Pin	O I	I/O pins for the CAN communication function
P85/$\overline{NMI}$	$\overline{NMI}$ Interrupt Input Pin	I	Input pin for the $\overline{NMI}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
$P9_0$ to $P9_7$	I/O Port P9	I/O	8-bit I/O ports having functions equivalent to P0. The PRCR register prevents PD9 and PS3 registers from rewriting.
$TB0_{IN}$ to $TB4_{IN}$	Timer B Pin	I	Input pins for timers B0 to B4
$\overline{CTS3}$, $\overline{CTS4}$	UART Pin	I	I/O pins for UART3 ($P9_0$ to $P9_3$) and UART4 ($P9_4$ to $P9_7$)
$\overline{RTS3}$, $\overline{RTS4}$		O	
$\overline{SS3}$, $\overline{SS4}$		I	
CLK3, CLK4		I/O	
RxD3, RxD4		I	
SCL3, SCL4		I/O	
STxD3, STxD4		O	
TxD3, TxD4		O	
SDA3, SDA4		I/O	
SRxD3, SRxD4		I	
DA0, DA1	D/A Output Pin	O	Output pins for the D/A converter
ANEX0,	A/D Related Pin	I/O	ANEX0 is an extended analog I/O pin for the A/D converter.
ANEX1,		I	ANEX1 is an extended analog input pin for the A/D converter.
$\overline{ADTRG}$		I	$\overline{ADTRG}$ is an A/D trigger input pin.
$OUTC2_0$	Intelligent I/O Pin	O	$OUTC2_0$ is an output pin for the waveform generating function.
ISTxD2		O	ISTxD2 and IE_{OUT} output transmit data for the intelligent I/O communication
IE_{OUT}		O	function.
IE_{IN}		I	ISRxD2 and IE_{IN} input received data for the intelligent I/O communication
ISRxD2		I	function.
$P10_0$ to $P10_7$	I/O Port P10	I/O	8-bit I/O ports having functions equivalent to P0
$\overline{KI0}$ to $\overline{KI3}$	Key Input Interrupt Pin	I	Input pins for the key input interrupt
AN_0 to AN_7	Analog Input Pin	I	Analog input pins for the A/D converter

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (144-Pin Package only) (Continued)

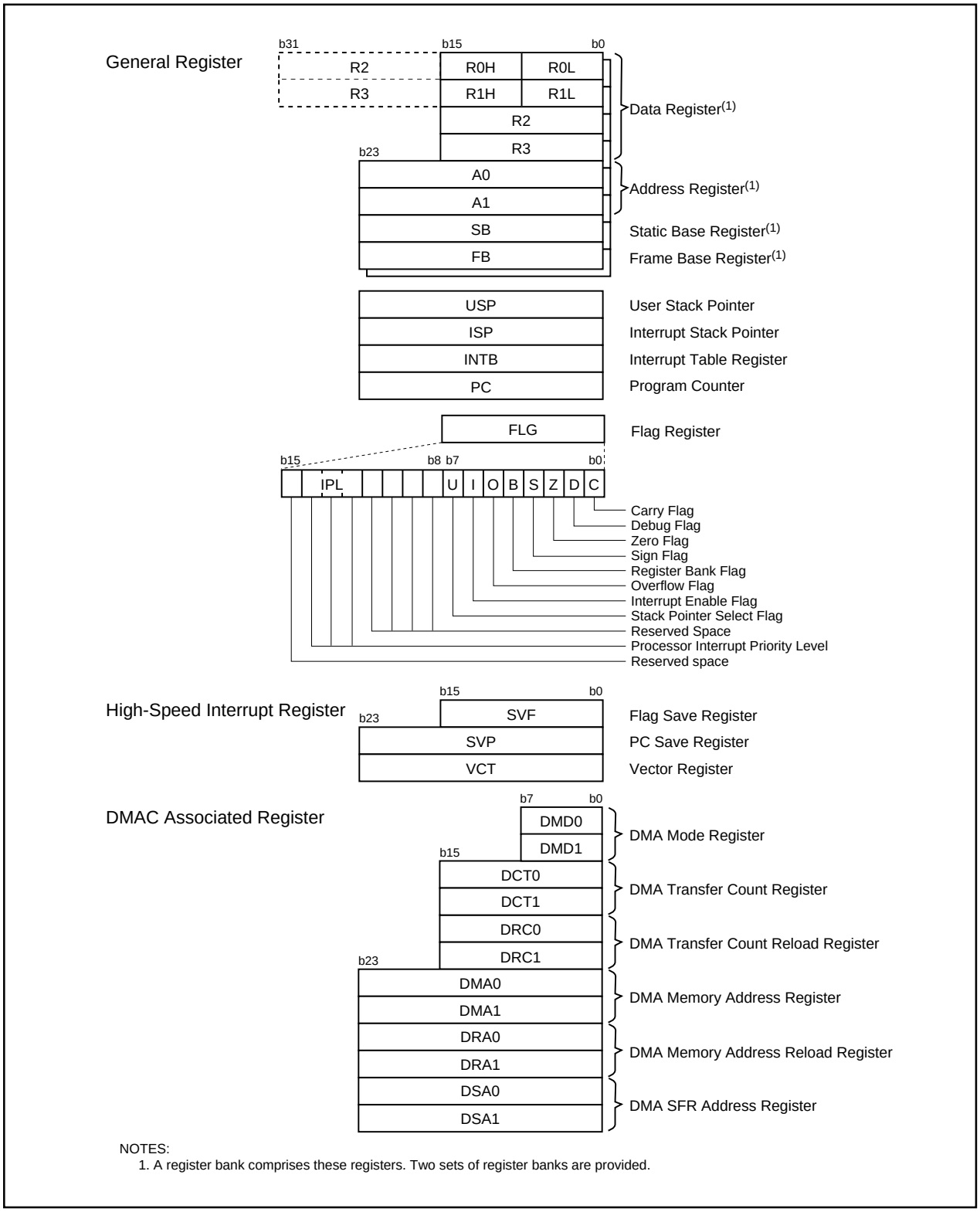
Symbol	Function	I/O type	Description
$P11_0$ to $P11_4$	I/O Port P11	I/O	5-bit I/O ports having functions equivalent to P0.
$INPC11$, $INPC12$	Intelligent I/O Pin	I	$INPC11$ and $INPC12$ are input pins for the time measurement function.
$OUTC10$ to $OUTC13$		O	$OUTC10$ to $OUTC13$ are output pins for the waveform generating function.
ISCLK1		I/O	ISCLK1 inputs and outputs the clock for the intelligent I/O communication
ISRxD1		I	function.
$BE1_{IN}$		I	ISRxD1 and $BE1_{IN}$ input received data for the intelligent I/O communication
ISTxD1		O	function.
$BE1_{OUT}$		O	ISTxD1 and $BE1_{OUT}$ output transmit data for the intelligent I/O communication function.
$P12_0$ to $P12_7$	I/O Port P12	I/O	8-bit I/O ports having functions equivalent to P0
$OUTC30$ to $OUTC37$	Intelligent I/O Pin	O	$OUTC30$ to $OUTC37$ are output pins for the waveform generating function.
ISCLK3		I/O	ISCLK3 inputs and outputs the clock for the intelligent I/O communication
ISRxD3		I	function.
ISTxD3		O	ISRxD3 inputs received data for the intelligent I/O communication function. ISTxD3 outputs transmit data for the intelligent I/O communication function.
$P13_0$ to $P13_7$	I/O Port P13	I/O	8-bit I/O ports having functions equivalent to P0
$OUTC20$ to $OUTC27$	Intelligent I/O Pin	O	$OUTC20$ to $OUTC27$ are output pins for the waveform generating function.
ISCLK2		I/O	ISCLK2 inputs and outputs the clock for the intelligent I/O communication
ISRxD2		I	function.
IE_{IN}		I	ISRxD2 and IE_{IN} input received data for the intelligent I/O communication
ISTxD2		O	function.
IE_{OUT}		O	ISTxD2 and IE_{OUT} output transmit data for the intelligent I/O communication function.
$P14_0$ to $P14_6$	I/O Port P14	I/O	7-bit I/O ports having functions equivalent to P0
$INPC16$, $INPC17$	Intelligent I/O Pin	I	$INPC16$ and $INPC17$ are input pins for the time measurement function.
$OUTC14$ to $OUTC17$		O	$OUTC14$ to $OUTC17$ are output pins for the waveform generating function.
$P15_0$ to $P15_7$	I/O Port P15	I/O	8-bit I/O ports having functions equivalent to P0
$INPC00$ to $INPC07$	Intelligent I/O Pin	I	$INPC00$ to $INPC07$ are input pins for the time measurement function.
$OUTC00$, $OUTC01$		O	$OUTC00$, $OUTC01$, $OUTC04$ and $OUTC05$ are output pins for the waveform
$OUTC04$, $OUTC05$			generating function.
ISCLK0		I/O	ISCLK0 inputs and outputs the clock for the intelligent I/O communication
ISRxD0		I	function.
$BE0_{IN}$		I	ISRxD0 and $BE0_{IN}$ input received data for the intelligent I/O communication
ISTxD0		O	function.
$BE0_{OUT}$		O	ISTxD0 and $BE0_{OUT}$ output transmit data for the intelligent I/O communication function.
$AN15_0$ to $AN15_7$	Analog Input Port	I	Analog input pins for the A/D converter

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

A register bank comprises 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTES:
1. A register bank comprises these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to "2.1.8 Flag Register (FLG)" for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows. Refer to **10.4 High-Speed Interrupt** for details.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows. Refer to **12. DMAC** for details.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/83 group.

M32C/83 provides 16-Mbyte address space from addresses 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated lower addresses beginning with address FFFFFF$_{16}$. For example, a 64-Kbyte internal ROM is allocated addresses FF0000$_{16}$ to FFFFFF$_{16}$.

The fixed interrupt vectors are allocated addresses FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine. Refer to **10. Interrupts** for details.

The internal RAM is allocated higher addresses beginning with address 000400$_{16}$. For example, a 10-Kbyte internal RAM is allocated addresses 000400$_{16}$ to 002BFF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D conversion, serial I/O, and timers, is allocated addresses 000000$_{16}$ to 0003FF$_{16}$. All addresses, which have nothing allocated within SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated addresses FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.

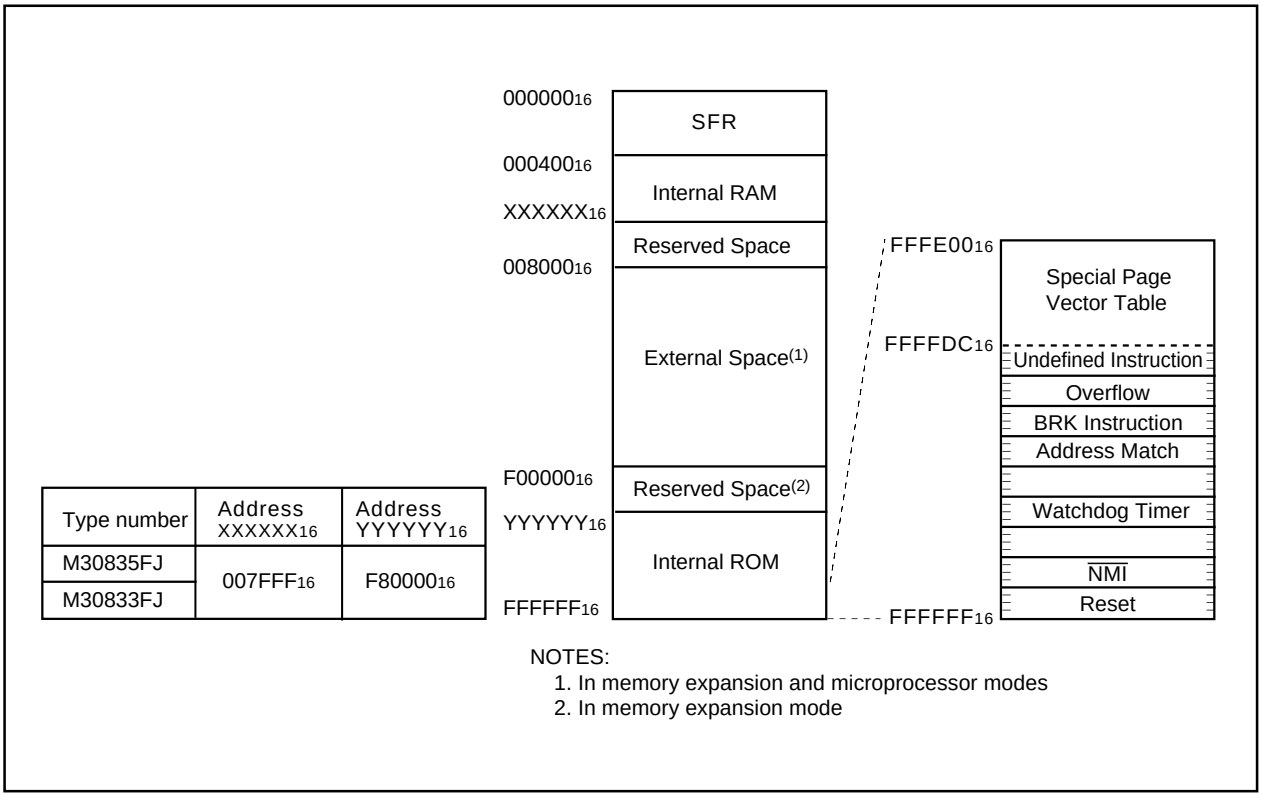


Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000$_{16}$			
0001$_{16}$			
0002$_{16}$			
0003$_{16}$			
0004$_{16}$	Processor Mode Register 0(1)	PM0	1000 0000$_2$ (CNVss pin ="L") 0000 0011$_2$ (CNVss pin ="H")
0005$_{16}$	Processor Mode Register 1	PM1	0X00 0000$_2$
0006$_{16}$	System Clock Control Register 0	CM0	0000 X000$_2$
0007$_{16}$	System Clock Control Register 1	CM1	0010 0000$_2$
0008$_{16}$	Wait Control Register	WCR	1111 1111$_2$
0009$_{16}$	Address Match Interrupt Enable Register	AIER	XXXX 0000$_2$
000A$_{16}$	Protect Register	PRCR	XXXX 0000$_2$
000B$_{16}$	External Data Bus Width Control Register	DS	XXXX 1000$_2$ (BYTE pin ="L") XXXX 0000$_2$ (BYTE pin ="H")
000C$_{16}$	Main Clock Division Register	MCD	XXX0 1000$_2$
000D$_{16}$	Oscillation Stop Detection Register	CM2	00$_{16}$
000E$_{16}$	Watchdog Timer Start Register	WDTS	XX$_{16}$
000F$_{16}$	Watchdog Timer Control Register	WDC	000X XXXX$_2$
0010$_{16}$ 0011$_{16}$ 0012$_{16}$	Address Match Interrupt Register 0	RMAD0	00 00 00$_{16}$
0013$_{16}$			
0014$_{16}$ 0015$_{16}$ 0016$_{16}$	Address Match Interrupt Register 1	RMAD1	00 00 00$_{16}$
0017$_{16}$	VDC Control Register for PLL	PLV	XXXX XX01$_2$
0018$_{16}$ 0019$_{16}$ 001A$_{16}$	Address Match Interrupt Register 2	RMAD2	00 00 00$_{16}$
001B$_{16}$	VDC Control Register 0	VDC0	00$_{16}$
001C$_{16}$ 001D$_{16}$ 001E$_{16}$	Address Match Interrupt Register 3	RMAD3	00 00 00$_{16}$
001F$_{16}$			
0020$_{16}$			
0021$_{16}$			
0022$_{16}$			
0023$_{16}$			
0024$_{16}$			
0025$_{16}$			
0026$_{16}$			
0027$_{16}$			
0028$_{16}$			
0029$_{16}$			
002A$_{16}$			
002B$_{16}$			
002C$_{16}$			
002D$_{16}$			
002E$_{16}$			
002F$_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The PM00 and PM01 bits in the PM1 register maintain values set before reset even if software reset or watchdog timer reset is performed.

Address	Register	Symbol	Value after RESET
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			
0040₁₆	DRAM Control Register	DRAMCONT	XX₁₆
0041₁₆	DRAM Refresh Interval Set Register	REFCNT	XX₁₆
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆			
004E₁₆			
004F₁₆			
0050₁₆			
0051₁₆			
0052₁₆			
0053₁₆			
0054₁₆			
0055₁₆			
0056₁₆			
0057₁₆	Flash Memory Control Register 0	FMR0	XX00 0001₂
0058₁₆			
0059₁₆			
005A₁₆			
005B₁₆			
005C₁₆			
005D₁₆			
005E₁₆			
005F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 Interrupt Control Register	DM0IC	XXXX X0002
006916	Timer B5 Interrupt Control Register	TB5IC	XXXX X0002
006A16	DMA2 Interrupt Control Register	DM2IC	XXXX X0002
006B16	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X0002
006C16	Timer A0 Interrupt Control Register	TA0IC	XXXX X0002
006D16	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X0002
006E16	Timer A2 Interrupt Control Register	TA2IC	XXXX X0002
006F16	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X0002
007016	Timer A4 Interrupt Control Register	TA4IC	XXXX X0002
007116	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X0002
007316	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X0002
007416	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X0002
007516	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X0002
007616	Timer B1 Interrupt Control Register	TB1IC	XXXX X0002
007716	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X0002
007816	Timer B3 Interrupt Control Register	TB3IC	XXXX X0002
007916	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X0002
007A16	INT5 Interrupt Control Register	INT5IC	XX00 X0002
007B16	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X0002
007C16	INT3 Interrupt Control Register	INT3IC	XX00 X0002
007D16	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X0002
007E16	INT1 Interrupt Control Register	INT1IC	XX00 X0002
007F16	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC CAN1IC	XXXX X0002
008016			
008116	Intelligent I/O Interrupt Control Register 11/ CAN Interrupt 2 Control Register	IIO11IC CAN2IC	XXXX X0002
008216			
008316			
008416			
008516			
008616	A/D1 Conversion Interrupt Control Register	AD1IC	XXXX X0002
008716			
008816	DMA1 Interrupt Control Register	DM1IC	XXXX X0002
008916	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X0002
008A16	DMA3 Interrupt Control Register	DM3IC	XXXX X0002
008B16	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X0002
008C16	Timer A1 Interrupt Control Register	TA1IC	XXXX X0002
008D16	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X0002
008E16	Timer A3 Interrupt Control Register	TA3IC	XXXX X0002
008F16	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
009016	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X0002
009116	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X0002
009216	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X0002
009316	Key Input Interrupt Control Register	KUPIC	XXXX X0002
009416	Timer B0 Interrupt Control Register	TB0IC	XXXX X0002
009516	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X0002
009616	Timer B2 Interrupt Control Register	TB2IC	XXXX X0002
009716	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X0002
009816	Timer B4 Interrupt Control Register	TB4IC	XXXX X0002
009916	Intelligent I/O Interrupt Control Register 5	IIO5IC	XXXX X0002
009A16	INT4 Interrupt Control Register	INT4IC	XX00 X0002
009B16	Intelligent I/O Interrupt Control Register 7	IIO7IC	XXXX X0002
009C16	INT2 Interrupt Control Register	INT2IC	XX00 X0002
009D16	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC CAN0IC	XXXX X0002
009E16	INT0 Interrupt Control Register	INT0IC	XX00 X0002
009F16	Exit Priority Control Register	RLVL	XXXX 00002
00A016	Interrupt Request Register 0	IIO0IR	0000 000X2
00A116	Interrupt Request Register 1	IIO1IR	0000 000X2
00A216	Interrupt Request Register 2	IIO2IR	0000 000X2
00A316	Interrupt Request Register 3	IIO3IR	0000 000X2
00A416	Interrupt Request Register 4	IIO4IR	0000 000X2
00A516	Interrupt Request Register 5	IIO5IR	0000 000X2
00A616	Interrupt Request Register 6	IIO6IR	0000 000X2
00A716	Interrupt Request Register 7	IIO7IR	0000 000X2
00A816	Interrupt Request Register 8	IIO8IR	0000 000X2
00A916	Interrupt Request Register 9	IIO9IR	0000 000X2
00AA16	Interrupt Request Register 10	IIO10IR	0000 000X2
00AB16	Interrupt Request Register 11	IIO11IR	0000 000X2
00AC16			
00AD16			
00AE16			
00AF16			
00B016	Interrupt Enable Register 0	IIO0IE	0016
00B116	Interrupt Enable Register 1	IIO1IE	0016
00B216	Interrupt Enable Register 2	IIO2IE	0016
00B316	Interrupt Enable Register 3	IIO3IE	0016
00B416	Interrupt Enable Register 4	IIO4IE	0016
00B516	Interrupt Enable Register 5	IIO5IE	0016
00B616	Interrupt Enable Register 6	IIO6IE	0016
00B716	Interrupt Enable Register 7	IIO7IE	0016
00B816	Interrupt Enable Register 8	IIO8IE	0016
00B916	Interrupt Enable Register 9	IIO9IE	0016
00BA16	Interrupt Enable Register 10	IIO10IE	0016
00BB16	Interrupt Enable Register 11	IIO11IE	0016
00BC16			
00BD16			
00BE16			
00BF16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0₁₆	Group 0 Time Measurement/Waveform Generating Register 0	G0TM0/G0PO0	XX₁₆
00C1₁₆			XX₁₆
00C2₁₆	Group 0 Time Measurement/Waveform Generating Register 1	G0TM1/G0PO1	XX₁₆
00C3₁₆			XX₁₆
00C4₁₆	Group 0 Time Measurement/Waveform Generating Register 2	G0TM2/G0PO2	XX₁₆
00C5₁₆			XX₁₆
00C6₁₆	Group 0 Time Measurement/Waveform Generating Register 3	G0TM3/G0PO3	XX₁₆
00C7₁₆			XX₁₆
00C8₁₆	Group 0 Time Measurement/Waveform Generating Register 4	G0TM4/G0PO4	XX₁₆
00C9₁₆			XX₁₆
00CA₁₆	Group 0 Time Measurement/Waveform Generating Register 5	G0TM5/G0PO5	XX₁₆
00CB₁₆			XX₁₆
00CC₁₆	Group 0 Time Measurement/Waveform Generating Register 6	G0TM6/G0PO6	XX₁₆
00CD₁₆			XX₁₆
00CE₁₆	Group 0 Time Measurement/Waveform Generating Register 7	G0TM7/G0PO7	XX₁₆
00CF₁₆			XX₁₆
00D0₁₆	Group 0 Waveform Generating Control Register 0	G0POCR0	0X00 X000₂
00D1₁₆	Group 0 Waveform Generating Control Register 1	G0POCR1	0X00 X000₂
00D2₁₆	Group 0 Waveform Generating Control Register 2	G0POCR2	0X00 X000₂
00D3₁₆	Group 0 Waveform Generating Control Register 3	G0POCR3	0X00 X000₂
00D4₁₆	Group 0 Waveform Generating Control Register 4	G0POCR4	0X00 X000₂
00D5₁₆	Group 0 Waveform Generating Control Register 5	G0POCR5	0X00 X000₂
00D6₁₆	Group 0 Waveform Generating Control Register 6	G0POCR6	0X00 X000₂
00D7₁₆	Group 0 Waveform Generating Control Register 7	G0POCR7	0X00 X000₂
00D8₁₆	Group 0 Time Measurement Control Register 0	G0TMCR0	00₁₆
00D9₁₆	Group 0 Time Measurement Control Register 1	G0TMCR1	00₁₆
00DA₁₆	Group 0 Time Measurement Control Register 2	G0TMCR2	00₁₆
00DB₁₆	Group 0 Time Measurement Control Register 3	G0TMCR3	00₁₆
00DC₁₆	Group 0 Time Measurement Control Register 4	G0TMCR4	00₁₆
00DD₁₆	Group 0 Time Measurement Control Register 5	G0TMCR5	00₁₆
00DE₁₆	Group 0 Time Measurement Control Register 6	G0TMCR6	00₁₆
00DF₁₆	Group 0 Time Measurement Control Register 7	G0TMCR7	00₁₆
00E0₁₆	Group 0 Base Timer Register	G0BT	XX₁₆
00E1₁₆			XX₁₆
00E2₁₆	Group 0 Base Timer Control Register 0	G0BCR0	00₁₆
00E3₁₆	Group 0 Base Timer Control Register 1	G0BCR1	00₁₆
00E4₁₆	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00₁₆
00E5₁₆	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00₁₆
00E6₁₆	Group 0 Function Enable Register	G0FE	00₁₆
00E7₁₆	Group 0 Function Select Register	G0FS	00₁₆
00E8₁₆	Group 0 SI/O Receive Buffer Register	G0RB	XXXX XXXX₂
00E9₁₆			XX00 XXXX₂
00EA₁₆	Group 0 Transmit Buffer/Receive Data Register	G0TB/G0DR	XX₁₆
00EB₁₆			
00EC₁₆	Group 0 Receive Input Register	G0RI	XX₁₆
00ED₁₆	Group 0 SI/O Communication Mode Register	G0MR	00₁₆
00EE₁₆	Group 0 Transmit Output Register	G0TO	XX₁₆
00EF₁₆	Group 0 SI/O Communication Control Register	G0CR	0000 X000₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0$_{16}$	Group 0 Data Compare Register 0	G0CMP0	XX$_{16}$
00F1$_{16}$	Group 0 Data Compare Register 1	G0CMP1	XX$_{16}$
00F2$_{16}$	Group 0 Data Compare Register 2	G0CMP2	XX$_{16}$
00F3$_{16}$	Group 0 Data Compare Register 3	G0CMP3	XX$_{16}$
00F4$_{16}$	Group 0 Data Mask Register 0	G0MSK0	XX$_{16}$
00F5$_{16}$	Group 0 Data Mask Register 1	G0MSK1	XX$_{16}$
00F6$_{16}$			
00F7$_{16}$			
00F8$_{16}$ 00F9$_{16}$	Group 0 Receive CRC Code Register	G0RCRC	XX$_{16}$ XX$_{16}$
00FA$_{16}$ 00FB$_{16}$	Group 0 Transmit CRC Code Register	G0TCRC	00$_{16}$ 00$_{16}$
00FC$_{16}$	Group 0 SI/O Extended Mode Register	G0EMR	00$_{16}$
00FD$_{16}$	Group 0 SI/O Extended Receive Control Register	G0ERC	00$_{16}$
00FE$_{16}$	Group 0 SI/O Special Communication Interrupt Detect Register	G0IRF	0000 00XX$_2$
00FF$_{16}$	Group 0 SI/O Extended Transmit Control Register	G0ETC	0000 0XXX$_2$
0100$_{16}$ 0101$_{16}$	Group 1 Time Measurement/Waveform Generating Register 0	G1TM0/G1PO0	XX$_{16}$ XX$_{16}$
0102$_{16}$ 0103$_{16}$	Group 1 Time Measurement/Waveform Generating Register 1	G1TM1/G1PO1	XX$_{16}$ XX$_{16}$
0104$_{16}$ 0105$_{16}$	Group 1 Time Measurement/Waveform Generating Register 2	G1TM2/G1PO2	XX$_{16}$ XX$_{16}$
0106$_{16}$ 0107$_{16}$	Group 1 Time Measurement/Waveform Generating Register 3	G1TM3/G1PO3	XX$_{16}$ XX$_{16}$
0108$_{16}$ 0109$_{16}$	Group 1 Time Measurement/Waveform Generating Register 4	G1TM4/G1PO4	XX$_{16}$ XX$_{16}$
010A$_{16}$ 010B$_{16}$	Group 1 Time Measurement/Waveform Generating Register 5	G1TM5/G1PO5	XX$_{16}$ XX$_{16}$
010C$_{16}$ 010D$_{16}$	Group 1 Time Measurement/Waveform Generating Register 6	G1TM6/G1PO6	XX$_{16}$ XX$_{16}$
010E$_{16}$ 010F$_{16}$	Group 1 Time Measurement/Waveform Generating Register 7	G1TM7/G1PO7	XX$_{16}$ XX$_{16}$
0110$_{16}$	Group 1 Waveform Generating Control Register 0	G1POCR0	0X00 X000$_2$
0111$_{16}$	Group 1 Waveform Generating Control Register 1	G1POCR1	0X00 X000$_2$
0112$_{16}$	Group 1 Waveform Generating Control Register 2	G1POCR2	0X00 X000$_2$
0113$_{16}$	Group 1 Waveform Generating Control Register 3	G1POCR3	0X00 X000$_2$
0114$_{16}$	Group 1 Waveform Generating Control Register 4	G1POCR4	0X00 X000$_2$
0115$_{16}$	Group 1 Waveform Generating Control Register 5	G1POCR5	0X00 X000$_2$
0116$_{16}$	Group 1 Waveform Generating Control Register 6	G1POCR6	0X00 X000$_2$
0117$_{16}$	Group 1 Waveform Generating Control Register 7	G1POCR7	0X00 X000$_2$
0118$_{16}$	Group 1 Time Measurement Control Register 0	G1TMCR0	00$_{16}$
0119$_{16}$	Group 1 Time Measurement Control Register 1	G1TMCR1	00$_{16}$
011A$_{16}$	Group 1 Time Measurement Control Register 2	G1TMCR2	00$_{16}$
011B$_{16}$	Group 1 Time Measurement Control Register 3	G1TMCR3	00$_{16}$
011C$_{16}$	Group 1 Time Measurement Control Register 4	G1TMCR4	00$_{16}$
011D$_{16}$	Group 1 Time Measurement Control Register 5	G1TMCR5	00$_{16}$
011E$_{16}$	Group 1 Time Measurement Control Register 6	G1TMCR6	00$_{16}$
011F$_{16}$	Group 1 Time Measurement Control Register 7	G1TMCR7	00$_{16}$

X: Indeterminate

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Address	Register	Symbol	Value after RESET
012016 012116	Group 1 Base Timer Register	G1BT	XX16 XX16
012216	Group 1 Base Timer Control Register 0	G1BCR0	0016
012316	Group 1 Base Timer Control Register 1	G1BCR1	0016
012416	Group 1 Time Measurement Prescaler Register 6	G1TPR6	0016
012516	Group 1 Time Measurement Prescaler Register 7	G1TPR7	0016
012616	Group 1 Function Enable Register	G1FE	0016
012716	Group 1 Function Select Register	G1FS	0016
012816 012916	Group 1 SI/O Receive Buffer Register	G1RB	XXXX XXXX2 XX00 XXXX2
012A16	Group 1 Transmit Buffer/Receive Data Register	G1TB/G1DR	XX16
012B16			
012C16	Group 1 Receive Input Register	G1RI	XX16
012D16	Group 1 SI/O Communication Mode Register	G1MR	0016
012E16	Group 1 Transmit Output Register	G1TO	XX16
012F16	Group 1 SI/O Communication Control Register	G1CR	0000 X0002
013016	Group 1 Data Compare Register 0	G1CMP0	XX16
013116	Group 1 Data Compare Register 1	G1CMP1	XX16
013216	Group 1 Data Compare Register 2	G1CMP2	XX16
013316	Group 1 Data Compare Register 3	G1CMP3	XX16
013416	Group 1 Data Mask Register 0	G1MSK0	XX16
013516	Group 1 Data Mask Register 1	G1MSK1	XX16
013616			
013716			
013816 013916	Group 1 Receive CRC Code Register	G1RCRC	XX16 XX16
013A16 013B16	Group 1 Transmit CRC Code Register	G1TCRC	0016 0016
013C16	Group 1 SI/O Extended Mode Register	G1EMR	0016
013D16	Group 1 SI/O Extended Receive Control Register	G1ERC	0016
013E16	Group 1 SI/O Special Communication Interrupt Detect Register	G1IRF	0000 00XX2
013F16	Group 1 SI/O Extended Transmit Control Register	G1ETC	0000 0XXX2
014016 014116	Group 2 Waveform Generating Register 0	G2PO0	XX16 XX16
014216 014316	Group 2 Waveform Generating Register 1	G2PO1	XX16 XX16
014416 014516	Group 2 Waveform Generating Register 2	G2PO2	XX16 XX16
014616 014716	Group 2 Waveform Generating Register 3	G2PO3	XX16 XX16
014816 014916	Group 2 Waveform Generating Register 4	G2PO4	XX16 XX16
014A16 014B16	Group 2 Waveform Generating Register 5	G2PO5	XX16 XX16
014C16 014D16	Group 2 Waveform Generating Register 6	G2PO6	XX16 XX16
014E16 014F16	Group 2 Waveform Generating Register 7	G2PO7	XX16 XX16

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0150₁₆	Group 2 Waveform Generating Control Register 0	G2POCR0	00₁₆
0151₁₆	Group 2 Waveform Generating Control Register 1	G2POCR1	00₁₆
0152₁₆	Group 2 Waveform Generating Control Register 2	G2POCR2	00₁₆
0153₁₆	Group 2 Waveform Generating Control Register 3	G2POCR3	00₁₆
0154₁₆	Group 2 Waveform Generating Control Register 4	G2POCR4	00₁₆
0155₁₆	Group 2 Waveform Generating Control Register 5	G2POCR5	00₁₆
0156₁₆	Group 2 Waveform Generating Control Register 6	G2POCR6	00₁₆
0157₁₆	Group 2 Waveform Generating Control Register 7	G2POCR7	00₁₆
0158₁₆			
0159₁₆			
015A₁₆			
015B₁₆			
015C₁₆			
015D₁₆			
015E₁₆			
015F₁₆			
0160₁₆ 0161₁₆	Group 2 Base Timer Register	G2BT	XX₁₆ XX₁₆
0162₁₆	Group 2 Base Timer Control Register 0	G2BCR0	00₁₆
0163₁₆	Group 2 Base Timer Control Register 1	G2BCR1	00₁₆
0164₁₆	Base Timer Start Register	BTSR	XXXX 0000₂
0165₁₆			
0166₁₆	Group 2 Function Enable Register	G2FE	00₁₆
0167₁₆	Group 2 RTP Output Buffer Register	G2RTP	00₁₆
0168₁₆			
0169₁₆			
016A₁₆	Group 2 SI/O Communication Mode Register	G2MR	00XX X000₂
016B₁₆	Group 2 SI/O Communication Control Register	G2CR	0000 X000₂
016C₁₆ 016D₁₆	Group 2 SI/O Transmit Buffer Register	G2TB	XX₁₆ XX₁₆
016E₁₆ 016F₁₆	Group 2 SI/O Receive Buffer Register	G2RB	XX₁₆ XX₁₆
0170₁₆ 0171₁₆	Group 2 IEBus Address Register	IEAR	XX₁₆ XX₁₆
0172₁₆	Group 2 IEBus Control Register	IECR	00XX X000₂
0173₁₆	Group 2 IEBus Transmit Interrupt Cause Detect Register	IETIF	XXX0 0000₂
0174₁₆	Group 2 IEBus Receive Interrupt Cause Detect Register	IERIF	XXX0 0000₂
0175₁₆			
0176₁₆			
0177₁₆			
0178₁₆	Input Function Select Register	IPS	00₁₆
0179₁₆			
017A₁₆	Group 3 SI/O Communication Mode Register	G3MR	00XX 0000₂
017B₁₆	Group 3 SI/O Communication Control Register	G3CR	0000 X000₂
017C₁₆ 017D₁₆	Group 3 SI/O Transmit Buffer Register	G3TB	XX₁₆ XX₁₆
017E₁₆ 017F₁₆	Group 3 SI/O Receive Buffer Register	G3RB	XX₁₆ XX₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
018016 018116	Group 3 Waveform Generating Register 0	G3PO0	XX16 XX16
018216 018316	Group 3 Waveform Generating Register 1	G3PO1	XX16 XX16
018416 018516	Group 3 Waveform Generating Register 2	G3PO2	XX16 XX16
018616 018716	Group 3 Waveform Generating Register 3	G3PO3	XX16 XX16
018816 018916	Group 3 Waveform Generating Register 4	G3PO4	XX16 XX16
018A16 018B16	Group 3 Waveform Generating Register 5	G3PO5	XX16 XX16
018C16 018D16	Group 3 Waveform Generating Register 6	G3PO6	XX16 XX16
018E16 018F16	Group 3 Waveform Generating Register 7	G3PO7	XX16 XX16
019016	Group 3 Waveform Generating Control Register 0	G3POCR0	0016
019116	Group 3 Waveform Generating Control Register 1	G3POCR1	0016
019216	Group 3 Waveform Generating Control Register 2	G3POCR2	0016
019316	Group 3 Waveform Generating Control Register 3	G3POCR3	0016
019416	Group 3 Waveform Generating Control Register 4	G3POCR4	0016
019516	Group 3 Waveform Generating Control Register 5	G3POCR5	0016
019616	Group 3 Waveform Generating Control Register 6	G3POCR6	0016
019716	Group 3 Waveform Generating Control Register 7	G3POCR7	0016
019816 019916	Group 3 Waveform Generating Mask Register 4	G3MK4	XX16 XX16
019A16 019B16	Group 3 Waveform Generating Mask Register 5	G3MK5	XX16 XX16
019C16 019D16	Group 3 Waveform Generating Mask Register 6	G3MK6	XX16 XX16
019E16 019F16	Group 3 Waveform Generating Mask Register 7	G3MK7	XX16 XX16
01A016 01A116	Group 3 Base Timer Register	G3BT	XX16 XX16
01A216	Group 3 Base Timer Control Register 0	G3BCR0	0016
01A316	Group 3 Base Timer Control Register 1	G3BCR1	0016
01A416			
01A516			
01A616	Group 3 Function Enable Register	G3FE	0016
01A716	Group 3 RTP Output Buffer Register	G3RTP	0016
01A816			
01A916			
01AA16			
01AB16			
01AC16			
01AD16	Group 3 SI/O Communication Flag Register	G3FLG	XXXX XXX02
01AE16			
01AF16			

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Address	Register	Symbol	Value after RESET
01B0₁₆			
01B1₁₆			
01B2₁₆			
01B3₁₆			
01B4₁₆			
01B5₁₆			
01B6₁₆			
01B7₁₆			
01B8₁₆			
01B9₁₆			
01BA₁₆			
01BB₁₆			
01BC₁₆			
01BD₁₆			
01BE₁₆			
01BF₁₆			
01C0₁₆ 01C1₁₆	A/D1 Register 0	AD10	XX₁₆ XX₁₆
01C2₁₆ 01C3₁₆	A/D1 Register 1	AD11	XX₁₆ XX₁₆
01C4₁₆ 01C5₁₆	A/D1 Register 2	AD12	XX₁₆ XX₁₆
01C6₁₆ 01C7₁₆	A/D1 Register 3	AD13	XX₁₆ XX₁₆
01C8₁₆ 01C9₁₆	A/D1 Register 4	AD14	XX₁₆ XX₁₆
01CA₁₆ 01CB₁₆	A/D1 Register 5	AD15	XX₁₆ XX₁₆
01CC₁₆ 01CD₁₆	A/D1 Register 6	AD16	XX₁₆ XX₁₆
01CE₁₆ 01CF₁₆	A/D1 Register 7	AD17	XX₁₆ XX₁₆
01D0₁₆			
01D1₁₆			
01D2₁₆			
01D3₁₆			
01D4₁₆	A/D1 Control Register 2	AD1CON2	X00X X000₂
01D5₁₆			
01D6₁₆	A/D1 Control Register 0	AD1CON0	00₁₆
01D7₁₆	A/D1 Control Register 1	AD1CON1	XX00 0000₂
01D8₁₆			
01D9₁₆			
01DA₁₆			
01DB₁₆			
01DC₁₆			
01DD₁₆			
01DE₁₆			
01DF₁₆			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
01E016	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX16
01E116	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX16
01E216	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX16
01E316	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX16
01E416	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX16
01E516	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX16
01E616	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX16
01E716	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX16
01E816	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX16
01E916	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX16
01EA16	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX16
01EB16	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX16
01EC16	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX16
01ED16	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX16
01EE16	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX16
01EF16	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX16
01F016	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX16
01F116	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX16
01F216	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX16
01F316	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX16
01F416	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX16
01F516	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX16
01F616	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX16
01F716	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX16
01F816	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX16
01F916	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX16
01FA16	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX16
01FB16	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX16
01FC16	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX16
01FD16	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX16
01FE16	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX16
01FF16	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX16
020016 020116	CAN0 Control Register 0	C0CTLR0	XX01 0X012(1) XXXX 00002(1)
020216 020316	CAN0 Status Register	C0STR	0000 00002(1) X000 0X012(1)
020416 020516	CAN0 Extended ID Register	C0IDR	0016(1) 0016(1)
020616 020716	CAN0 Configuration Register	C0CONR	0000 XXXX2(1) 0000 00002(1)
020816 020916	CAN0 Time Stamp Register	C0TSR	0016(1) 0016(1)
020A16	CAN0 Transmit Error Count Register	C0TEC	0016(1)
020B16	CAN0 Receive Error Count Register	C0REC	0016(1)
020C16 020D16	CAN0 Slot Interrupt Status Register	C0SISTR	0016(1) 0016(1)
020E16			
020F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
021016 021116	CAN0 Slot Interrupt Mask Register	C0SIMKR	0016(2) 0016(2)
021216			
021316			
021416	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X0002(2)
021516	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X0002(2)
021616			
021716	CAN0 Baud Rate Prescaler	C0BRP	0000 00012(2)
021816			
021916			
021A16			
021B16			
021C16			
021D16			
021E16			
021F16			
022016			
022116			
022216			
022316			
022416			
022516			
022616			
022716			
022816	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 00002(2)
022916	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 00002(2)
022A16	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 00002(2)
022B16	CAN0 Global Mask Register Extended ID1	C0GMR3	0016(2)
022C16	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 00002(2)
022D16			
022E16			
022F16			
023016	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 00002(2) XXX0 00002(2)
023116	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 00002(2) XX00 00002(2)
023216	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 00002(2) XXXX 00002(2)
023316	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	0016(2) 0016(2)
023416	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 00002(2) XX00 00002(2)
023516	CAN0 Message Slot 5 Control Register	C0MCTL5	0016(2)
023616	CAN0 Message Slot 6 Control Register	C0MCTL6	0016(2)
023716	CAN0 Message Slot 7 Control Register	C0MCTL7	0016(2)
023816	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 00002(2) XXX0 00002(2)

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
023916	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 00002(2) XX00 00002(2)
023A16	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 00002(2) XXXX 00002(2)
023B16	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	0016(2) 0016(2)
023C16	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 00002(2) XX00 00002(2)
023D16	CAN0 Message Slot 13 Control Register	C0MCTL13	0016(2)
023E16	CAN0 Message Slot 14 Control Register	C0MCTL14	0016(2)
023F16	CAN0 Message Slot 15 Control Register	C0MCTL15	0016(2)
024016	CAN0 Slot Buffer Select Register	C0SBS	0016(2)
024116	CAN0 Control Register 1	C0CTLR1	XX00 00XX2(2)
024216	CAN0 Sleep Control Register	C0SLPR	XXXX XXX02
024316			
024416 024516	CAN0 Acceptance Filter Support Register	C0AFS	0016(2) 0116(2)
024616			
024716			
024816			
024916			
024A16			
024B16			
024C16			
024D16			
024E16			
024F16			
025016			
025116			
025216			
025316			
025416			
025516			
025616			
025716			
025816			
025916			
025A16			
025B16			
025C16			
025D16			
025E16			
025F16			
026016			
026116 to 02BF16			

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02C0₁₆ 02C1₁₆	X0 Register Y0 Register	X0R,Y0R	XX₁₆ XX₁₆
02C2₁₆ 02C3₁₆	X1 Register Y1 Register	X1R,Y1R	XX₁₆ XX₁₆
02C4₁₆ 02C5₁₆	X2 Register Y2 Register	X2R,Y2R	XX₁₆ XX₁₆
02C6₁₆ 02C7₁₆	X3 Register Y3 Register	X3R,Y3R	XX₁₆ XX₁₆
02C8₁₆ 02C9₁₆	X4 Register Y4 Register	X4R,Y4R	XX₁₆ XX₁₆
02CA₁₆ 02CB₁₆	X5 Register Y5 Register	X5R,Y5R	XX₁₆ XX₁₆
02CC₁₆ 02CD₁₆	X6 Register Y6 Register	X6R,Y6R	XX₁₆ XX₁₆
02CE₁₆ 02CF₁₆	X7 Register Y7 Register	X7R,Y7R	XX₁₆ XX₁₆
02D0₁₆ 02D1₁₆	X8 Register Y8 Register	X8R,Y8R	XX₁₆ XX₁₆
02D2₁₆ 02D3₁₆	X9 Register Y9 Register	X9R,Y9R	XX₁₆ XX₁₆
02D4₁₆ 02D5₁₆	X10 Register Y10 Register	X10R,Y10R	XX₁₆ XX₁₆
02D6₁₆ 02D7₁₆	X11 Register Y11 Register	X11R,Y11R	XX₁₆ XX₁₆
02D8₁₆ 02D9₁₆	X12 Register Y12 Register	X12R,Y12R	XX₁₆ XX₁₆
02DA₁₆ 02DB₁₆	X13 Register Y13 Register	X13R,Y13R	XX₁₆ XX₁₆
02DC₁₆ 02DD₁₆	X14 Register Y14 Register	X14R,Y14R	XX₁₆ XX₁₆
02DE₁₆ 02DF₁₆	X15 Register Y15 Register	X15R,Y15R	XX₁₆ XX₁₆
02E0₁₆	XY Control Register	XYC	XXXX XX00₂
02E1₁₆			
02E2₁₆			
02E3₁₆			
02E4₁₆	UART1 Special Mode Register 4	U1SMR4	00₁₆
02E5₁₆	UART1 Special Mode Register 3	U1SMR3	00₁₆
02E6₁₆	UART1 Special Mode Register 2	U1SMR2	00₁₆
02E7₁₆	UART1 Special Mode Register	U1SMR	00₁₆
02E8₁₆	UART1 Transmit/Receive Mode Register	U1MR	00₁₆
02E9₁₆	UART1 Baud Rate Register	U1BRG	XX₁₆
02EA₁₆ 02EB₁₆	UART1 Transmit Buffer Register	U1TB	XX₁₆ XX₁₆
02EC₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000₂
02ED₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010₂
02EE₁₆ 02EF₁₆	UART1 Receive Buffer Register	U1RB	XX₁₆ XX₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Baud Rate Register	U4BRG	XX₁₆
02FA₁₆ 02FB₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆ XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆ 02FF₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆ XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆ 0303₁₆	Timer A1-1 Register	TA11	XX₁₆ XX₁₆
0304₁₆ 0305₁₆	Timer A2-1 Register	TA21	XX₁₆ XX₁₆
0306₁₆ 0307₁₆	Timer A4-1 Register	TA41	XX₁₆ XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			
0310₁₆ 0311₁₆	Timer B3 Register	TB3	XX₁₆ XX₁₆
0312₁₆ 0313₁₆	Timer B4 Register	TB4	XX₁₆ XX₁₆
0314₁₆ 0315₁₆	Timer B5 Register	TB5	XX₁₆ XX₁₆
0316₁₆			
0317₁₆			
0318₁₆			
0319₁₆			
031A₁₆			
031B₁₆	Timer B3 Mode Register	TB3MR	00XX 0000₂
031C₁₆	Timer B4 Mode Register	TB4MR	00XX 0000₂
031D₁₆	Timer B5 Mode Register	TB5MR	00XX 0000₂
031E₁₆			
031F₁₆	External Interrupt Cause Select Register	IFSR	00₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
032016			
032116			
032216			
032316			
032416	UART3 Special Mode Register 4	U3SMR4	0016
032516	UART3 Special Mode Register 3	U3SMR3	0016
032616	UART3 Special Mode Register 2	U3SMR2	0016
032716	UART3 Special Mode Register	U3SMR	0016
032816	UART3 Transmit/Receive Mode Register	U3MR	0016
032916	UART3 Baud Rate Register	U3BRG	XX16
032A16 032B16	UART3 Transmit Buffer Register	U3TB	XX16 XX16
032C16	UART3 Transmit/Receive Control Register 0	U3C0	0000 10002
032D16	UART3 Transmit/Receive Control Register 1	U3C1	0000 00102
032E16 032F16	UART3 Receive Buffer Register	U3RB	XX16 XX16
033016			
033116			
033216			
033316			
033416	UART2 Special Mode Register 4	U2SMR4	0016
033516	UART2 Special Mode Register 3	U2SMR3	0016
033616	UART2 Special Mode Register 2	U2SMR2	0016
033716	UART2 Special Mode Register	U2SMR	0016
033816	UART2 Transmit/Receive Mode Register	U2MR	0016
033916	UART2 Baud Rate Register	U2BRG	XX16
033A16 033B16	UART2 Transmit Buffer Register	U2TB	XX16 XX16
033C16	UART2 Transmit/Receive Control Register 0	U2C0	0000 10002
033D16	UART2 Transmit/Receive Control Register 1	U2C1	0000 00102
033E16 033F16	UART2 Receive Buffer Register	U2RB	XX16 XX16
034016	Count Start Flag	TABSR	0016
034116	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX2
034216	One-Shot Start Flag	ONSF	0016
034316	Trigger Select Register	TRGSR	0016
034416	Up-Down Flag	UDF	0016
034516			
034616 034716	Timer A0 Register	TA0	XX16 XX16
034816 034916	Timer A1 Register	TA1	XX16 XX16
034A16 034B16	Timer A2 Register	TA2	XX16 XX16
034C16 034D16	Timer A3 Register	TA3	XX16 XX16
034E16 034F16	Timer A4 Register	TA4	XX16 XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
035016	Timer B0 Register	TB0	XX16
035116			XX16
035216	Timer B1 Register	TB1	XX16
035316			XX16
035416	Timer B2 Register	TB2	XX16
035516			XX16
035616	Timer A0 Mode Register	TA0MR	0000 0X002
035716	Timer A1 Mode Register	TA1MR	0000 0X002
035816	Timer A2 Mode Register	TA2MR	0000 0X002
035916	Timer A3 Mode Register	TA3MR	0000 0X002
035A16	Timer A4 Mode Register	TA4MR	0000 0X002
035B16	Timer B0 Mode Register	TB0MR	00XX 00002
035C16	Timer B1 Mode register	TB1MR	00XX 00002
035D16	Timer B2 Mode Register	TB2MR	00XX 00002
035E16	Timer B2 Special Mode Register	TB2SC	XXXX XXX02
035F16	Count Source Prescaler Register(1)	TCSPR	0XXX 00002
036016			
036116			
036216			
036316			
036416	UART0 Special Mode Register 4	U0SMR4	0016
036516	UART0 Special Mode Register 3	U0SMR3	0016
036616	UART0 Special Mode Register 2	U0SMR2	0016
036716	UART0 Special Mode Register	U0SMR	0016
036816	UART0 Transmit/Receive Mode Register	U0MR	0016
036916	UART0 Baud Rate Register	U0BRG	XX16
036A16	UART0 Transmit Buffer Register	U0TB	XX16
036B16			XX16
036C16	UART0 Transmit/Receive Control Register 0	U0C0	0000 10002
036D16	UART0 Transmit/Receive Control Register 1	U0C1	0000 00102
036E16	UART0 Receive Buffer Register	U0RB	XX16
036F16			XX16
037016			
037116			
037216			
037316			
037416			
037516			
037616	PLL Control Register 0	PLC0	0011 X1002
037716	PLL Control Register 1	PLC1	XXXX 00002
037816	DMA0 Cause Select Register	DM0SL	0X00 00002
037916	DMA1 Cause Select Register	DM1SL	0X00 00002
037A16	DMA2 Cause Select Register	DM2SL	0X00 00002
037B16	DMA3 Cause Select Register	DM3SL	0X00 00002
037C16	CRC Data Register	CRCD	XX16
037D16			XX16
037E16	CRC Input Register	CRCIN	XX16
037F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The TCSPR register maintains the values set before reset even if software reset or watchdog timer reset is performed.

Address	Register	Symbol	Value after RESET
038016 038116	A/D0 Register 0	AD00	XX16 XX16
038216 038316	A/D0 Register 1	AD01	XX16 XX16
038416 038516	A/D0 Register 2	AD02	XX16 XX16
038616 038716	A/D0 Register 3	AD03	XX16 XX16
038816 038916	A/D0 Register 4	AD04	XX16 XX16
038A16 038B16	A/D0 Register 5	AD05	XX16 XX16
038C16 038D16	A/D0 Register 6	AD06	XX16 XX16
038E16 038F16	A/D0 Register 7	AD07	XX16 XX16
039016			
039116			
039216			
039316			
039416	A/D0 Control Register 2	AD0CON2	X000 00002
039516			
039616	A/D0 Control Register 0	AD0CON0	0016
039716	A/D0 Control Register 1	AD0CON1	0016
039816	D/A Register 0	DA0	XX16
039916			
039A16	D/A Register 1	DA1	XX16
039B16			
039C16	D/A Control Register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03A0₁₆	Function Select Register A8	PS8	X000 0000₂
03A1₁₆	Function Select Register A9	PS9	00₁₆
03A2₁₆			
03A3₁₆			
03A4₁₆			
03A5₁₆			
03A6₁₆			
03A7₁₆			
03A8₁₆			
03A9₁₆			
03AA₁₆			
03AB₁₆			
03AC₁₆			
03AD₁₆			
03AE₁₆			
03AF₁₆	Function Select Register C	PSC	00X0 0000₂
03B0₁₆	Function Select Register A0	PS0	00₁₆
03B1₁₆	Function Select Register A1	PS1	00₁₆
03B2₁₆	Function Select Register B0	PSL0	00₁₆
03B3₁₆	Function Select Register B1	PSL1	00₁₆
03B4₁₆	Function Select Register A2	PS2	00X0 0000₂
03B5₁₆	Function Select Register A3	PS3	00₁₆
03B6₁₆	Function Select Register B2	PSL2	00X0 0000₂
03B7₁₆	Function Select Register B3	PSL3	00₁₆
03B8₁₆			
03B9₁₆	Function Select Register A5	PS5	XXX0 0000₂
03BA₁₆			
03BB₁₆			
03BC₁₆	Function Select Register A6	PS6	00₁₆
03BD₁₆	Function Select Register A7	PS7	00₁₆
03BE₁₆			
03BF₁₆			
03C0₁₆	Port P6 Register	P6	XX₁₆
03C1₁₆	Port P7 Register	P7	XX₁₆
03C2₁₆	Port P6 Direction Register	PD6	00₁₆
03C3₁₆	Port P7 Direction Register	PD7	00₁₆
03C4₁₆	Port P8 Register	P8	XX₁₆
03C5₁₆	Port P9 Register	P9	XX₁₆
03C6₁₆	Port P8 Direction Register	PD8	00X0 0000₂
03C7₁₆	Port P9 Direction Register	PD9	00₁₆
03C8₁₆	Port P10 Register	P10	XX₁₆
03C9₁₆	Port P11 Register	P11	XX₁₆
03CA₁₆	Port P10 Direction Register	PD10	00₁₆
03CB₁₆	Port P11 Direction Register	PD11	XXX0 0000₂
03CC₁₆	Port P12 Register	P12	XX₁₆
03CD₁₆	Port P13 Register	P13	XX₁₆
03CE₁₆	Port P12 Direction Register	PD12	00₁₆
03CF₁₆	Port P13 Direction Register	PD13	00₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03D0₁₆	Port P14 Register	P14	XX₁₆
03D1₁₆	Port P15 Register	P15	XX₁₆
03D2₁₆	Port P14 Direction Register	PD14	X000 0000₂
03D3₁₆	Port P15 Direction Register	PD15	00₁₆
03D4₁₆			
03D5₁₆			
03D6₁₆			
03D7₁₆			
03D8₁₆			
03D9₁₆			
03DA₁₆	Pull-Up Control Register 2	PUR2	00₁₆
03DB₁₆	Pull-Up Control Register 3	PUR3	00₁₆
03DC₁₆	Pull-Up Control Register 4	PUR4	XXXX 0000₂
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 Register	P0	XX₁₆
03E1₁₆	Port P1 Register	P1	XX₁₆
03E2₁₆	Port P0 Direction Register	PD0	00₁₆
03E3₁₆	Port P1 Direction Register	PD1	00₁₆
03E4₁₆	Port P2 Register	P2	XX₁₆
03E5₁₆	Port P3 Register	P3	XX₁₆
03E6₁₆	Port P2 Direction Register	PD2	00₁₆
03E7₁₆	Port P3 Direction Register	PD3	00₁₆
03E8₁₆	Port P4 Register	P4	XX₁₆
03E9₁₆	Port P5 Register	P5	XX₁₆
03EA₁₆	Port P4 Direction Register	PD4	00₁₆
03EB₁₆	Port P5 Direction Register	PD5	00₁₆
03EC₁₆			
03ED₁₆			
03EE₁₆			
03EF₁₆			
03F0₁₆	Pull-Up Control Register 0	PUR0	00₁₆
03F1₁₆	Pull-Up Control Register 1	PUR1	XXXX 0000₂
03F2₁₆			
03F3₁₆			
03F4₁₆			
03F5₁₆			
03F6₁₆			
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆			
03FD₁₆			
03FE₁₆			
03FF₁₆	Port Control Register	PCR	XXXX XXX0₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET	
03A016				(Note 2)
03A116				
03A216				
03A316				
03A416				
03A516				
03A616				
03A716				
03A816				
03A916				
03AA16				
03AB16				
03AC16				
03AD16				
03AE16				
03AF16	Function Select Register C	PSC	0X00 00002	
03B016	Function Select Register A0	PS0	0016	
03B116	Function Select Register A1	PS1	0016	
03B216	Function Select Register B0	PSL0	0016	
03B316	Function Select Register B1	PSL1	0016	
03B416	Function Select Register A2	PS2	00X0 00002	
03B516	Function Select Register A3	PS3	0016	
03B616	Function Select Register B2	PSL2	00X0 00002	
03B716	Function Select Register B3	PSL3	0016	
03B816				
03B916				(Note 2)
03BA16				
03BB16				
03BC16				(Note 2)
03BD16				
03BE16				
03BF16				
03C016	Port P6 Register	P6	XX16	
03C116	Port P7 Register	P7	XX16	
03C216	Port P6 Direction Register	PD6	0016	
03C316	Port P7 Direction Register	PD7	0016	
03C416	Port P8 Register	P8	XX16	
03C516	Port P9 Register	P9	XX16	
03C616	Port P8 Direction Register	PD8	00X0 00002	
03C716	Port P9 Direction Register	PD9	0016	
03C816	Port P10 Register	P10	XX16	
03C916				(Note 2)
03CA16	Port P10 Direction Register	PD10	0016	
03CB16				(Note 1)
03CC16				(Note 2)
03CD16				
03CE16				(Note 1)
03CF16				

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Set address spaces 03CB16, 03CE16 and 03CF16 to "FF16" in the 100-pin package.
2. Address spaces 03A016, 03A116, 03B916, 03BC16, 03BD16, 03C916, 03CC16 and 03CD16 are not provided in the 100-pin package.

<100-pin package>

Address	Register	Symbol	Value after RESET	
03D016				(Note 3)
03D116				
03D216				(Note 1)
03D316				
03D416				
03D516				
03D616				
03D716				
03D816				
03D916				
03DA16	Pull-up Control Register 2	PUR2	0016	
03DB16	Pull-up Control Register 3	PUR3	0016	
03DC16				(Note 2)
03DD16				
03DE16				
03DF16				
03E016	Port P0 Register	P0	XX16	
03E116	Port P1 Register	P1	XX16	
03E216	Port P0 Direction Register	PD0	0016	
03E316	Port P1 Direction Register	PD1	0016	
03E416	Port P2 Register	P2	XX16	
03E516	Port P3 Register	P3	XX16	
03E616	Port P2 Direction Register	PD2	0016	
03E716	Port P3 Direction Register	PD3	0016	
03E816	Port P4 Register	P4	XX16	
03E916	Port P5 Register	P5	XX16	
03EA16	Port P4 Direction Register	PD4	0016	
03EB16	Port P5 Direction Register	PD5	0016	
03EC16				
03ED16				
03EE16				
03EF16				
03F016	Pull-Up Control Register 0	PUR0	0016	
03F116	Pull-Up Control Register 1	PUR1	XXXX 00002	
03F216				
03F316				
03F416				
03F516				
03F616				
03F716				
03F816				
03F916				
03FA16				
03FB16				
03FC16				
03FD16				
03FE16				
03FF16	Port Control Register	PCR	XXXX XXX02	

X: Indeterminate
Blank spaces are reserved. No access is allowed.

NOTES:

1. Set address spaces 03D216 and 03D316 to "FF16" in the 100-pin package.
2. Set address spaces 03DC16 to "0016" in the 100-pin package.
3. Address spaces 03D016 and 03D116 are not provided in the 100-pin package.

5. Reset

Hardware reset, software reset, and watchdog timer reset are available to reset the microcomputer.

5.1 Hardware Reset

5.1.1 Reset on a Stable Supply Voltage

The microcomputer resets pins, the CPU and SFR when the supply voltage meets the recommended performance conditions while an "L" signal is applied to the $\overline{\text{RESET}}$ pin (see **Table 5.1**). Apply an "H" signal to the $\overline{\text{RESET}}$ pin again after 20 or more clock cycles are input to the XIN pin while applying an "L" to the $\overline{\text{RESET}}$ pin. The CPU and SFR are reset and programs run from the address indicated by the reset vector.

The internal RAM is not reset. When the $\overline{\text{RESET}}$ pin becomes "L" while writing data to the internal RAM, the internal RAM is in an indeterminate state.

5.1.2 Power-on Reset

The microcomputer resets pins, the CPU and SFR when the supply voltage applied to the VCC pin meets the recommended performance conditions while an "L" signal is applied to the $\overline{\text{RESET}}$ pin. (See **Table 5.1**.)

The CPU and SFR are reset when the signal applied to the $\overline{\text{RESET}}$ pin changes low ("L") to high ("H") after the main clock oscillation stabilizes and 20 or more clock cycles are applied to the XIN pin. Programs run from the address indicated by the reset vector. The internal RAM is in a indeterminate state

Figure 5.1 shows a reset circuit. Figure 5.2 shows a reset sequence. Figure 5.3 shows CPU register conditions after reset. Table 5.1 lists pin states while the $\overline{\text{RESET}}$ pin is held "L". Refer to **4. SFR** for SFR states after reset.

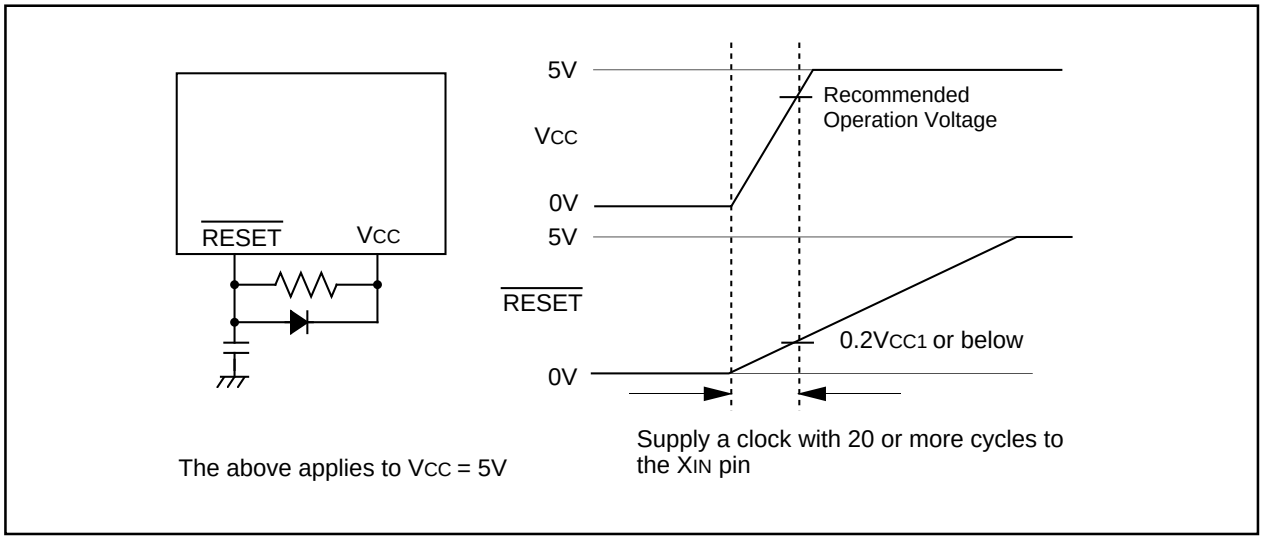


Figure 5.1 Reset Circuit

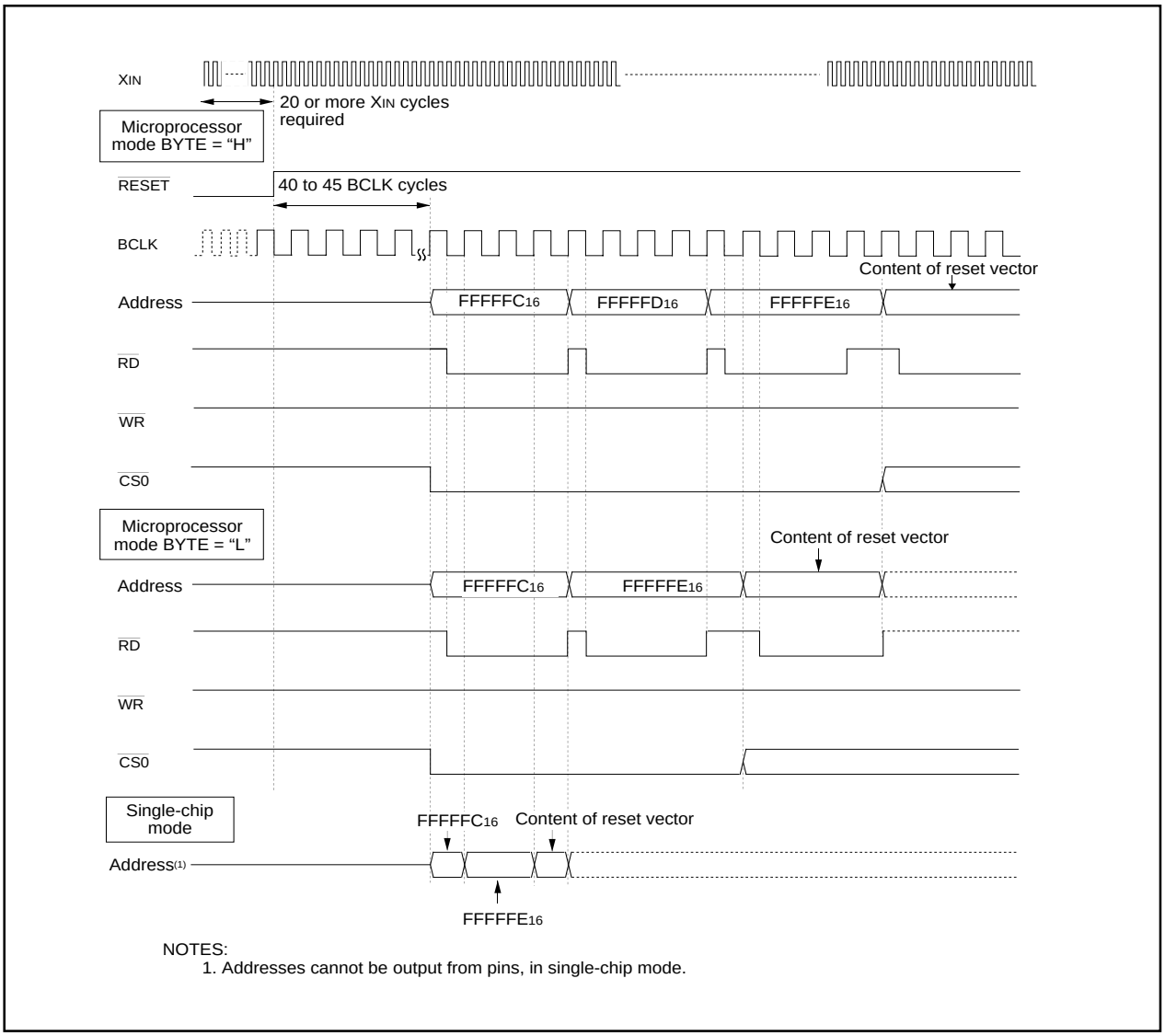


Figure 5.2 Reset Sequence

Table 5.1 Pin States while $\overline{\text{RESET}}$ Pin is Held "L"

Pin Name	Pin States		
	CNVSS = VSS	CNVSS = VCC	
		BYTE = VSS	BYTE = VCC
P0	Input port (high-impedance)	Data input (high-impedance)	
P1	Input port (high-impedance)	Data input (high-impedance)	Input port (high-impedance)
P2, P3, P4	Input port (high-impedance)	Address output (indeterminate)	
P5$_0$	Input port (high-impedance)	$\overline{\text{WR}}$ output (output "H")	
P5$_1$	Input port (high-impedance)	$\overline{\text{BHE}}$ output (indeterminate)	
P5$_2$	Input port (high-impedance)	$\overline{\text{RD}}$ output (output "H")	
P5$_3$	Input port (high-impedance)	BCLK output	
P5$_4$	Input port (high-impedance)	$\overline{\text{HLDA}}$ output (output value depends on an input to $\overline{\text{HOLD}}$ pin)	
P5$_5$	Input port (high-impedance)	$\overline{\text{HOLD}}$ input (high-impedance)	
P5$_6$	Input port (high-impedance)	$\overline{\text{RAS}}$ output	
P5$_7$	Input port (high-impedance)	$\overline{\text{RDY}}$ input (high-impedance)	
P6 to P15 (1)	Input port (high-impedance)	Input port (high-impedance)	

NOTES:
1. Ports P11 to P15 are provided in the 144-pin package.

5.2 Software Reset

When the PM03 bit in the PM0 register is set to "1" (microcomputer reset), pins, the CPU and SFR are reset. Then the microcomputer executes the program from an address determined by the reset vector.
When software reset is performed, some registers in the SFR are not reset. Refer to **4. SFR** for details.
Set the PM03 bit to "1" while the main clock is selected as the CPU clock and the main clock oscillation is stable.

5.3 Watchdog Timer Reset

The microcomputer resets pins, the CPU and the SFR when the watchdog timer underflows while the CM06 bit in the CM0 register is set to "1" (reset). Then the microcomputer executes the program from an address indicated by the reset vector.
When watchdog timer reset is performed, some registers in the SFR are not reset. Refer to **4. SFR** for details. Because the PM01 to PM00 bits in the PM0 register are not reset, the processor mode remains unchanged.

5.4 Internal Space

Figure 5.3 shows CPU register states after reset. Refer to **4. SFR** for SFR states after reset.

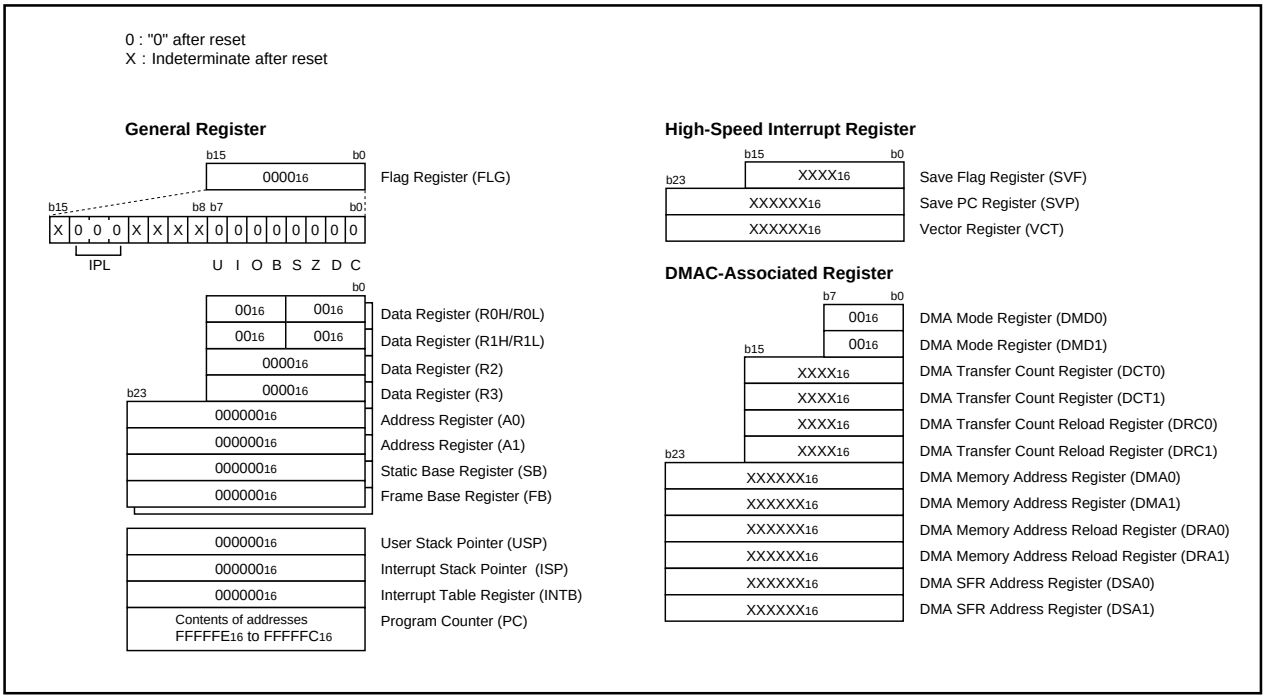


Figure 5.3 CPU Register after Reset

6. Processor Mode

6.1 Types of Processor Mode

Single-chip mode, memory expansion mode, or microprocessor mode can be selected as processor mode. Pin functions, memory map and accessible space vary depending on the selected processor mode.

6.1.1 Single-chip Mode

In single-chip mode, internal memory space (the SFR, internal RAM and internal ROM) can be accessed. All I/O ports can be used.

6.1.2 Memory Expansion Mode

In memory expansion mode, both external memory space and internal memory space can be accessed . Some pins function as pins for bus control signals. The BYTE pin and register settings determine how many pins are assigned for these pin functions. Refer to **7. Bus** for details.

6.1.3 Microprocessor Mode

In microprocessor mode, SFR, internal RAM and external memory space can be accessed. Internal ROM cannot be accessed.

Some pins function as pins for bus control signals. The BYTE pin and register settings determine how many pins are assigned for these pin functions. (Refer to **7. Bus** for details.)

6.2 Setting Processor Mode

The processor mode is set by the combination of CNVSS pin and the PM01 to PM00 bit settings in the PM0 register. Do not set the PM01 to PM00 bits to "10$_2$".

If the PM01 to PM00 bits are rewritten, the mode corresponding to the PM01 to PM00 bits is selected regardless of CNVSS pin level.

Do not change the PM01 to PM00 bits when the PM02 to PM07 bits in the PM0 register are being rewritten.

Do not enter microprocessor mode while the CPU is executing a program in the internal ROM . Do not enter single-chip mode while the CPU is executing a program in an external memory space.

Figures 6.1 and 6.2 show the PM0 register and PM1 register. Figure 6.3 shows a memory map in each processor mode.

6.2.1 Applying VSS to CNVSS Pin

The microcomputer enters single-chip mode after reset. Set the PM01 to PM00 bits to "01$_2$" (memory expansion mode) to switch to memory expansion mode after the microcomputer starts operating.

6.2.2 Applying VCC to CNVSS Pin

The microcomputer enters microprocessor mode after reset.

When using the flash memory version, apply VCC to P5$_5$ (HOLD) as well as to the CNVSS.

Processor Mode Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
	0						

Symbol: PM0
Address: 0004₁₆
After Reset: 1000 0000₂ (CNVss = "L")
0000 0011₂ (CNVss = "H")

Bit Symbol	Bit Name	Function	RW
PM00	Processor Mode Bit(2, 3)	b1 b0 0 0: Single-chip mode 0 1: Memory expansion mode 1 0: Do not set to this value 1 1: Microprocessor mode	RW
PM01			RW
PM02	R/W Mode Select Bit(4)	0: $\overline{RD}$ / $\overline{BHE}$ / $\overline{WR}$ 1: $\overline{RD}$ / $\overline{WRH}$ / $\overline{WRL}$	RW
PM03	Software Reset Bit	The microcomputer is reset when this bit is set to "1". When read, its content is "0".	RW
PM04	Multiplexed Bus Space Select Bit(5)	b5 b4 0 0 : Multiplexed bus is not used 0 1 : Access the $\overline{CS2}$ area with the bus 0 1 : Access the $\overline{CS1}$ area with the bus 1 1 : Access all $\overline{CS}$ areas with the bus(6)	RW
PM05			RW
—— (b6)	Reserved Bit	Set to "0"	RW
PM07	BCLK Output Disable Bit(7)	0 : BCLK is output(8) 1 : BCLK is not output The CM01 and CM00 bits in the CM0 register determine pin functions.	RW

NOTES:
1. Rewrite the PM0 register after the PRC1 bit in the PRCR register is set to "1" (write enable).
2. Processor mode is not changed even if the PM03 bit is set to "1" (software reset).
3. Set the PM01 to PM00 bits to "01₂" or "11₂" separately. Rewrite other bits before rewriting the PM01 to PM00 bits.
4. When using the 16-bit data bus in the DRAMC, set the PM02 bit to "1".
5. The PM05 to PM04 bits are available in memory expansion mode or microprocessor mode.
   - Set the PM05 to PM04 bits to "00₂" in mode 0.
   - Do not set the PM05 to PM04 bits to "01₂" in mode 2.
6. The PM05 to PM04 bits cannot be set to "11₂" in microprocessor mode because the microcomputer starts operation using the separate bus after reset.
   When the PM05 to PM04 bits are set to "11₂" in memory expansion mode, the microcomputer can access each 64K-byte chip-select-assigned address space. The multiplexed bus is not available in mode 0. The microcomputer accesses $\overline{CS0}$ to $\overline{CS2}$ in mode 1, $\overline{CS0}$ and $\overline{CS1}$ in mode 2 and $\overline{CS0}$ to $\overline{CS3}$ in mode 3.
7. No BCLK is output in single-chip mode even if the PM07 bit is set to "0". When a clock output is terminated in microprocessor mode or memory expansion mode, set the PM07 bit to "1" and the CM01 to CM00 bits in the CM0 register to "00₂" (I/O port P5₃). P5₃ outputs "L" .
8. When the PM07 bit is set to "0" (BCLK output), set the CM01 and CM00 bits to "00₂".

Figure 6.1 PM0 Register

Processor Mode Register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
0								PM1	0005₁₆	0X00 0000₂

Bit Symbol	Bit Name	Function	RW
PM10	External Memory Space Mode Bit(2)	b1 b0 0 0 : Mode 0 (A20 to A23 for P44 to P47) 0 1 : Mode 1 (A20 for P44, CS2 to CS0 for P45 to P47) 1 0 : Mode 2 (A20, A21 for P44, P45, CS1, CS0 for P46, P47) 1 1 : Mode 3(3) (CS3 to CS0 for P44 to P47)	RW
PM11			RW
PM12	Internal Memory Wait Bit	0 : No wait state 1 : Wait state	RW
PM13	SFR Area Wait Bit 0	0 : 1 wait state 1 : 2 wait states(4)	RW
PM14	ALE Pin Select Bit(2)	b5 b4 0 0 : No ALE 0 1 : P53/BCLK(5) 1 0 : P56/RAS 1 1 : P54/HLDA	RW
PM15			RW
(b6)	Nothing is assigned. When read, its content is indeterminate.		–
(b7)	Reserved Bit	Set to "0"	RW

NOTES:
1. Rewrite the PM1 register after the PRC1 bit in the PRCR register is set to "1" (write enable).
2. The PM10 and PM11 bits are available in memory expansion mode or microprocessor mode.
3. The DRAMC is not available when the PM11 and PM1 bits are set to "11₂" (mode 3).
4. Set the PM13 bit to "1" (2 wait states) to access CAN-associated registers (addresses 01E0₁₆ to 0245₁₆).
5. Set the CM01 and CM00 bits in the CM0 register to "00₂" (I/O port P53) when the PM15 and PM14 bits are set to "01₂" (P53/BCLK select).

Figure 6.2 PM1 Register

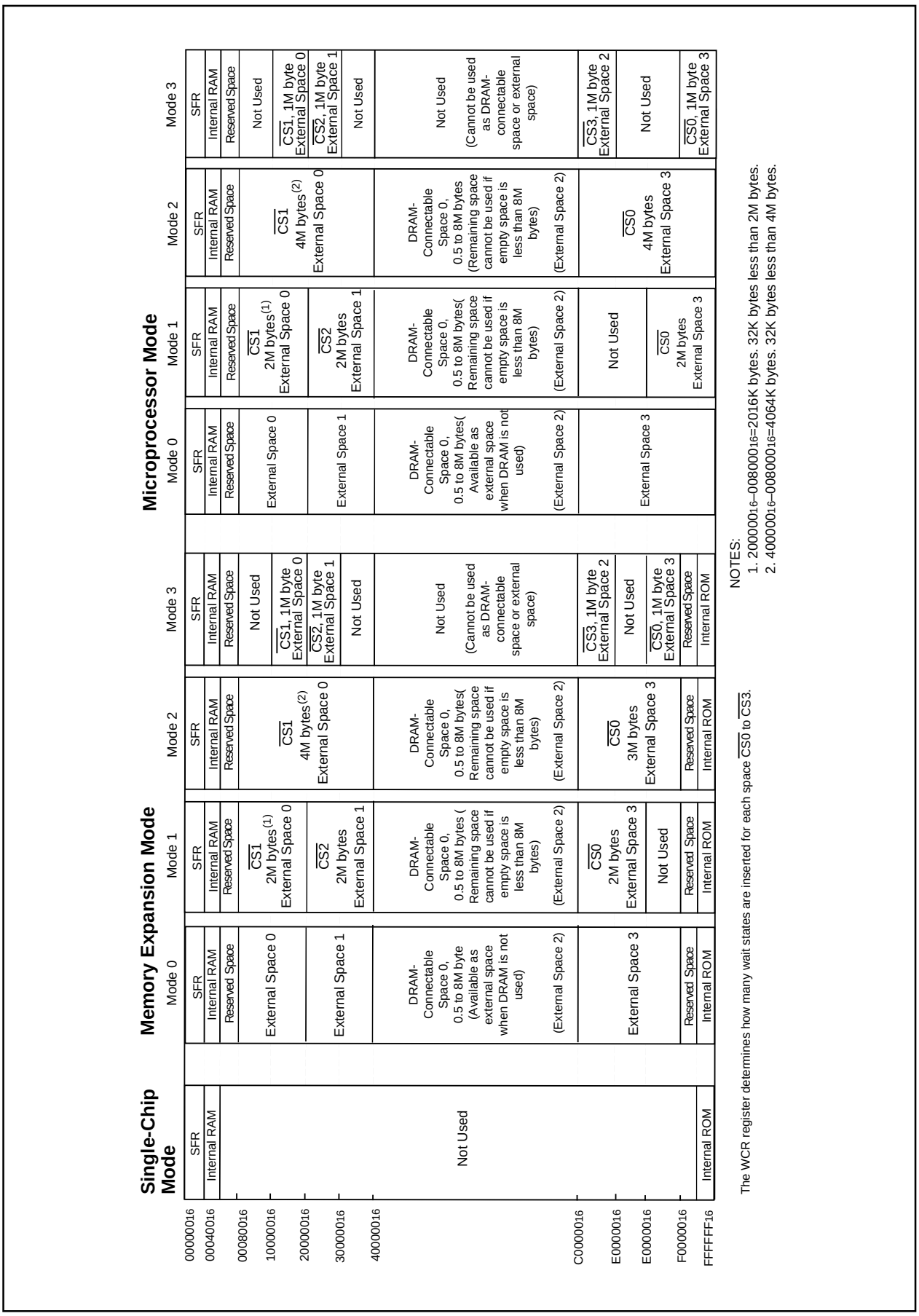


Figure 6.3 Memory Map in Each Processor Mode

7. Bus

In memory expansion mode or microprocessor mode, some pins function as bus control pins to input and output data from external devices. A_0 to A_{22}, $\overline{A_{23}}$, D_0 to D_{15}, MA_0 to MA_{12}, $\overline{CS_0}$ to $\overline{CS_3}$, $\overline{WRL}/\overline{WR}/\overline{CASL}$, $\overline{WRH}/\overline{BHE}/\overline{CASH}$, $\overline{RD}/\overline{DW}$, BCLK/ALE, $\overline{HLDA}$/ALE, $\overline{HOLD}$, ALE/$\overline{RAS}$, and $\overline{RDY}$ are used as bus control pins.

7.1 Bus Settings

The BYTE pin, the DS register, the PM05 to PM04 bits in the PM0 register and the PM11 to PM10 bits in the PM1 register determine bus settings.

Table 7.1 lists how to change a bus setting. Figure 7.1 shows the DS register.

Table 7.1 Bus Settings

Bus Setting	Changed By
Selecting external address bus width	DS register
Setting bus width after reset	BYTE pin (external space 3 only)
Switching between separate bus or multiplexed bus	PM05 to PM04 bits in PM0 register
Number of chip-select	PM11 to PM10 bits in PM1 register

External Data Bus Width Control Register

b7	b6	b5	b4	b3	b2	b1	b0
✕	✕	✕	✕				

Symbol: DS
Address: $000B_{16}$
After Reset: XXXX 1000_2 (BYTE pin = "L")
XXXX 0000_2 (BYTE pin = "H")

Bit Symbol	Bit Name	Function	RW
DS0	External Space 0 Data Bus Width Select Bit	0 : 8 bits wide 1 : 16 bits wide	RW
DS1	External Space 1 Data Bus Width Select Bit	0 : 8 bits wide 1 : 16 bits wide	RW
DS2	External Space 2 Data Bus Width Select Bit	0 : 8 bits wide 1 : 16 bits wide	RW
DS3	External Space 3 Data Bus Width Select Bit(1)	0 : 8 bits wide 1 : 16 bits wide	RW
—— (b7 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. After reset, the DS3 bit is set to "1" when the BYTE pin is held "L". It is set to "0" when the BYTE pin is held "H".

Figure 7.1 DS Register

7.1.1 Selecting External Address Bus

The number of externally-output address bus, chip-select signals and chip-select-assigned address space ($\overline{CS}$ area) varies depending on each external space mode. The PM11 to PM10 bits in the PM1 register determine the external space mode.

When using the DRAMC, row addresses and column addresses are multiplexed to output in the DRAM area.

7.1.2 Selecting External Data Bus

The DS register selects either external 8-bit or 16-bit data bus per external space. The data bus in the external space 3, after reset, becomes 16 bits wide when an "L" signal is applied to the BYTE pin and 8 bits wide when an "H" signal is applied. Do not change the BYTE pin level while the microcomputer is operating. The internal bus is always 16 bits wide.

7.1.3 Selecting Separate/Multiplexed Bus

The PM05 to PM04 bits in the PM0 register determine either a separate or multiplexed bus as bus format .

7.1.3.1 Separate Bus

The separate bus is a bus format which allows the microcomputer to input and output data and address using separate buses. The DS register selects 8-bit or 16-bit data bus as the external data bus width per external space. If all DSi bits in the DS register (i=0 to 3) are set to "0" (8-bit data bus), port P_0 becomes the data bus and port P_1 becomes the programmable I/O port. If one of the DSi bits is set to "1" (16-bit data bus), ports P0 and P1 become the data bus. When the microcomputer accesses a space while the DSi bit set to "0", port P1 is indeterminate.

If the microcomputer accesses a space with the separate bus, the WCR register determines whether a software wait state is inserted or not.

7.1.3.2 Multiplexed Bus

The multiplexed bus is a bus format which allows the microcomputer to input and output data and address via bus by timesharing. D_0 to D_7 are multiplexed with A_0 to A_7 in space accessed by the 8-bit data bus. D_0 to D_{15} are multiplexed with A_0 to A_{15} in space accessed by the 16-bit data bus. If the microcomputer accesses a space with the multiplexed bus, the WCR register can be set to either two wait states or three wait states. Two-wait-state access is automatically selected if the WCR register is set to no wait state or one wait state. Refer to **7.2.4 Bus Timing** for details.

The microcomputer starts operation using the separate bus after reset. Therefore, the multiplexed bus can be assigned to access the $\overline{CS1}$ area, the $\overline{CS2}$ area, or all $\overline{CS}$ areas. However, the multiplexed bus cannot be assigned to access all $\overline{CS}$ areas in microprocessor mode. When the PM05 and PM04 bits in the PM0 register are set to "11_2" (access all $\overline{CS}$ areas with the bus), only 16 low-order bits, from A_0 to A_{15}, of an address are output. See Table 7.2 for details.

Table 7.2 Processor Mode and Port Function

Processor Mode	Single-Chip Mode	Memory Expansion Mode/ Microprocessor Mode				Memory Expansion Mode	
PM05 to PM04 Bits in PM0 Register		"01_2", "10_2" (Access $\overline{CS1}$ or $\overline{CS2}$ using the Multiplexed Bus Access All Other $\overline{CS}$ Areas using the Separate Bus)		"00_2" (Access all $\overline{CS}$ Areas using the Separate Bus)		"11_2"(1) (Access all $\overline{CS}$ Areas using the Multiplexed Bus)	
Data Bus Width		Access all external space with 8-bit data bus	Access one or more external space with 16-bit data bus	Access all external space with 8-bit data bus	Access one or more external space with 16-bit data bus	Access all external space with 8-bit data bus	Access one or more external space with 16-bit data bus
$P0_0$ to $P0_7$	I/O port	Data bus D_0 to D_7	Data bus D_0 to D_7	Data bus D_0 to D_7	Data bus D_0 to D_7	I/O port	I/O port
$P1_0$ to $P1_7$	I/O port	I/O port	Data bus D_8 to D_{15}	I/O port	Data bus D_8 to D_{15}	I/O port	I/O port
$P2_0$ to $P2_7$	I/O port	Address bus/ Data bus(2) A_0/D_0 to A_7/D_7	Address bus/ Data bus(2) A_0/D_0 to A_7/D_7	Address bus A_0 to A_7	Address bus A_0 to A_7	Address bus/ Data bus A_0/D_0 to A_7/D_7	Address bus/ Data bus A_0/D_0 to A_7/D_7
$P3_0$ to $P3_7$	I/O port	Address bus A_8 to A_{15}	Address bus/ Data bus(2) A_8/D_8 to A_{15}/D_{15}	Address bus A_8 to A_{15}	Address bus A_8 to A_{15}	Address bus A_8 to A_{15}	Address bus/ Data bus A_8/D_8 to A_{15}/D_{15}
$P4_0$ to $P4_3$	I/O port	Address bus A_{16} to A_{19}	Address bus A_{16} to A_{19}	Address bus A_{16} to A_{19}	Address bus A_{16} to A_{19}	I/O port	I/O port
$P4_4$ to $P4_6$	I/O port	$\overline{CS}$ (Chip-select signal) or Address bus (A_{20} to A_{22}) (Refer to 7.2 Bus Control for details)(4)					
$P4_7$	I/O port	$\overline{CS}$ (Chip-select signal) or Address bus (A_{23}) (Refer to 7.2 Bus Control for details)(4)					
$P5_0$ to $P5_3$	I/O port	Outputs $\overline{RD}$, $\overline{WRL}$, $\overline{WRH}$ and BCLK or outputs $\overline{RD}$, $\overline{BHE}$, $\overline{WR}$ and BCLK (Refer to 7.2 Bus Control for details)(3)					
$P5_4$	I/O port	$\overline{HLDA}$ (3)	$\overline{HLDA}$ (3)	$\overline{HLDA}$ (3)	$\overline{HLDA}$ (3)	$\overline{HLDA}$ (3)	$\overline{HLDA}$ (3)
$P5_5$	I/O port	$\overline{HOLD}$	$\overline{HOLD}$	$\overline{HOLD}$	$\overline{HOLD}$	$\overline{HOLD}$	$\overline{HOLD}$
$P5_6$	I/O port	$\overline{RAS}$ (3)	$\overline{RAS}$ (3)	$\overline{RAS}$ (3)	$\overline{RAS}$ (3)	$\overline{RAS}$ (3)	$\overline{RAS}$ (3)
$P5_7$	I/O port	$\overline{RDY}$	$\overline{RDY}$	$\overline{RDY}$	$\overline{RDY}$	$\overline{RDY}$	$\overline{RDY}$

NOTES:
1. Do not set the PM05 to PM04 bits to "11_2" (access all $\overline{CS}$ areas using multiplexed bus) in microprocessor mode because the microcomputer starts operation using the separate bus after reset. When the PM05 to PM04 bits are set to "11_2" in memory expansion mode, the microcomputer accesses 64K-byte memory space per chip select using the address bus .
2. These ports become address buses when accessing space using the separate bus.
3. The PM15 to PM14 bits in the PM1 register determine which pin outputs the ALE signal. The PM02 bit in the PM0 register selects either "$\overline{WRL}$,$\overline{WRH}$" or "$\overline{BHE}$,$\overline{WR}$" combination.
4. When DRAMC is selected to access DRAM area, $\overline{CASL}$, $\overline{CASH}$, $\overline{DW}$, $\overline{BCLK}$ become output pins.
5. The PM11 to PM10 bits in the PM1 register determine the $\overline{CS}$ signal and address bus.

7.2 Bus Control

Signals required to access external devices are provided and software wait states are inserted as follows. The signals are available in memory expansion mode and microprocessor mode only.

7.2.1 Address Bus and Data Bus

The address bus is a signal accessing 16M-byte space and uses 24 control pins; A_0 to A_{22} and $\overline{A_{23}}$. $\overline{A_{23}}$ is the inversed output signal of the highest-order address bit.

The data bus is a signal which inputs and outputs data. The DS register selects the 8-bit data bus from D_0 to D_7 or the 16-bit data bus from D_0 to D_{15} for each external space. When applying an "H" signal to the BYTE pin, the data bus accessing the external memory space 3 becomes the 8-bit data bus after reset. When applying an "L" signal to the BYTE pin, the data bus accessing the external memory space 3 becomes the 16-bit data bus.

When changing single-chip mode to memory expansion mode, the address bus is in an indeterminate state until the microcomputer accesses an external memory space.

When using the DRAMC to access DRAM area, row addresses and column addresses are multiplexed and output via A_8 to A_{20}.

7.2.2 Chip-Select Signal

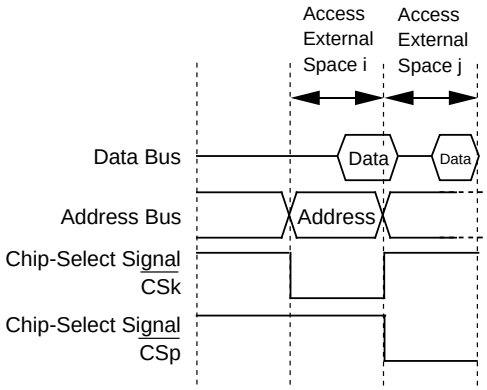
The chip-select signal shares ports with A_0 to A_{22} and $\overline{A_{23}}$. The PM11 to PM10 bits in the PM1 register determine which CS area is accessed and how many chip-select signals are output. A maximum of four chip-select signals can be output.

In microprocessor mode, the chip-select signal is not output after reset. $\overline{A_{23}}$, however, can perform as the chip-signal signal.

The chip-select signal becomes "L" while the microcomputer accesses the external $\overline{CSi}$ area (i=0 to 3). It becomes high ("H") when the microcomputer accesses another external memory space or an internal memory space. Figure 7.2 shows an example of the address bus and chip-select signal output.

Example 1:

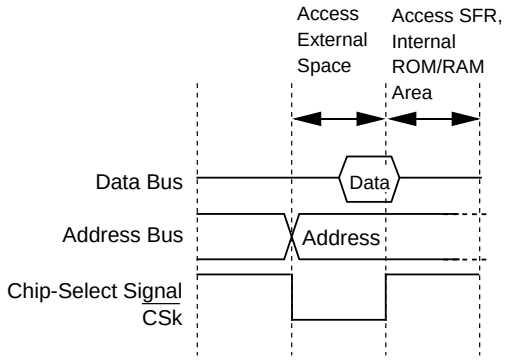
When the microcomputer accesses the external space j specified by another chip-select signal in the next cycle after having accessed the external space i, both address bus and chip-select signal change.



i = 0 to 3
j = 0 to 3, excluding i
k = 0 to 3
p= 0 to 3, excluding k
(See Figure 6.3 for i, j and p, k)

Example 2:

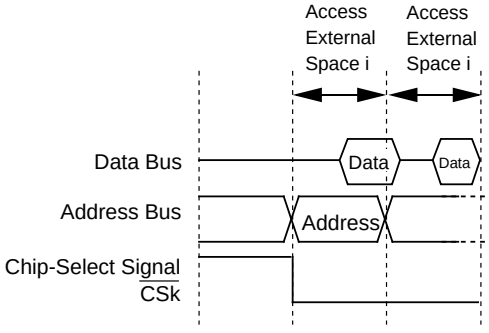
When the microcomputer accesses the SFR or the internal ROM/RAM area in the next cycle after having accessed an external space, the chip-select signal changes but the address bus does not.



k = 0 to 3

Example 3:

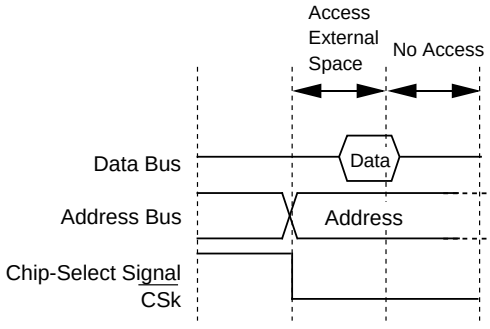
When the microcomputer accesses the space i specified by the same chip-select signal in the next cycle after having accessed the external space i, the address bus changes but the chip-select signal does not.



i = 0 to 3
k = 0 to 3
(See Figure 6.3 for i and k)

Example 4:

When the microcomputer does not access any space in the next cycle after having accessed an external space (no pre-fetch of an instruction is generated), neither address bus nor chip-select signal changes.



k = 0 to 3

NOTES:
1. The above applies to the address bus and chip-select signal in two consecutive cycles.
   By combining these examples, a chip-select signal extended by two or more cycles may be output.

Figure 7.2 Address Bus and Chip-Select Signal Outputs (Separate bus)

7.2.3 Read and Write Signals

When set to the 16-bit data bus, the PM02 bit in the PM0 register selects a combination of the $\overline{RD}$, $\overline{WR}$ and $\overline{BHE}$ signals or the $\overline{RD}$, $\overline{WRL}$ and $\overline{WRH}$ signals to determine the read or write signal. When the DS3 to DS0 bits in the DS register are set to "0" (8-bit data bus), set the PM02 bit to "0" ($\overline{RD}$/$\overline{WR}$/$\overline{BHE}$). If any of the DS3 to DS0 bits are set to "1" (16-bit data bus) when accessing an 8-bit space, the combination of $\overline{RD}$, $\overline{WR}$ and $\overline{BHE}$ is automatically selected regardless of the PM02 bit setting. Tables 7.3 and 7.4 list each signal operations.

The $\overline{RD}$, $\overline{WR}$ and $\overline{BHE}$ signals are combined for the read or write signal after reset.

When changing the combination to $\overline{RD}$, $\overline{WRL}$ and $\overline{WRH}$, set the PM02 bit before writing data to an external memory.

When using the DRAMC to access the DRAM with the 16-bit bus, set the PM02 bit to "1" ($\overline{RD}$/ $\overline{WRL}$/ $\overline{WRH}$).

Table 7.3 $\overline{RD}$, $\overline{WRL}$ and $\overline{WRH}$ Signals

Data Bus	$\overline{RD}$	$\overline{WRL}$	$\overline{WRH}$	Status of External Data Bus
16 Bits	L	H	H	Read data
	H	L	H	Write 1-byte data to even address
	H	H	L	Write 1-byte data to odd address
	H	L	L	Write data to both even and odd addresses
8 Bits	H	L(1)	Not used	Write 1-byte data
	L	H(1)	Not used	Read 1-byte data

NOTES:

1. The $\overline{WR}$ signal is used instead of the $\overline{WRL}$ signal.

Table 7.4 $\overline{RD}$, $\overline{WR}$ and $\overline{BHE}$ Signals

Data Bus	$\overline{RD}$	$\overline{WR}$	$\overline{BHE}$	A_0	Status of External Data Bus
16 Bits	H	L	L	H	Write 1-byte data to odd address
	L	H	L	H	Read 1-byte data from odd address
	H	L	H	L	Write 1-byte data to even address
	L	H	H	L	Read 1-byte data from even address
	H	L	L	L	Write data to both even and odd addresses
	L	H	L	L	Read data from both even and odd addresses
8 Bits	H	L	Not used	H / L	Write 1-byte data
	L	H	Not used	H / L	Read 1-byte data

7.2.4 Bus Timing

Bus cycle for the internal ROM and internal RAM are basically one BCLK cycle. When the PM12 bit in the PM1 register is set to "1" (wait state), the bus cycles are two BCLK cycles.

Bus cycles for the SFR are basically two BCLK cycles. When the PM13 bit in the PM1 register is set to "1" (2 wait states), the bus cycles are three BCLK cycles. To access CAN-associated registers (addresses $01E0_{16}$ to 0245_{16}), set the PM13 bit to "1".

Bus cycle for an external space is basically one BCLK cycle for a read operation and two BCLK cycles for a write operation. The WCR register inserts wait states equivalent to one to three BCLK cycles into an external space. Bus cycles are two BCLK cycles if selecting one wait state. Bus cycles are four BCLK cycles if selecting three wait states.

If applicable to the followings, bus cycles vary from those selected by the WCR register. Figure 7.5 shows each bit status and bus cycle.

- Write cycle with the separate bus and no wait state
- Read cycle and write cycle with the multiplexed bus and no wait state.
- Read cycle and write cycle with the multiplexed bus and one wait state.

Figure 7.3 shows the WCR register. Figures 7.4 and 7.5 show bus timing in an external space.

Wait Control Register(1, 2)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
WCR	0008_{16}	$1111\ 1111_2$

Bit Symbol	Bit Name	Function	RW
WCR0	External Space 0 Wait Bit	b1 b0 0 0: No wait state 0 1: 1 wait state 1 0: 2 wait states 1 1: 3 wait states	RW
WCR1			RW
WCR2	External Space 1 Wait Bit	b3 b2 0 0: No wait state 0 1: 1 wait state 1 0: 2 wait states 1 1: 3 wait states	RW
WCR3			RW
WCR4	External Space 2 Wait Bit	b5 b4 0 0: No wait state 0 1: 1 wait state 1 0: 2 wait states 1 1: 3 wait states	RW
WCR5			RW
WCR6	External Space 3 Wait Bit	b7 b6 0 0: No wait state 0 1: 1 wait state 1 0: 2 wait states 1 1: 3 wait states	RW
WCR7			RW

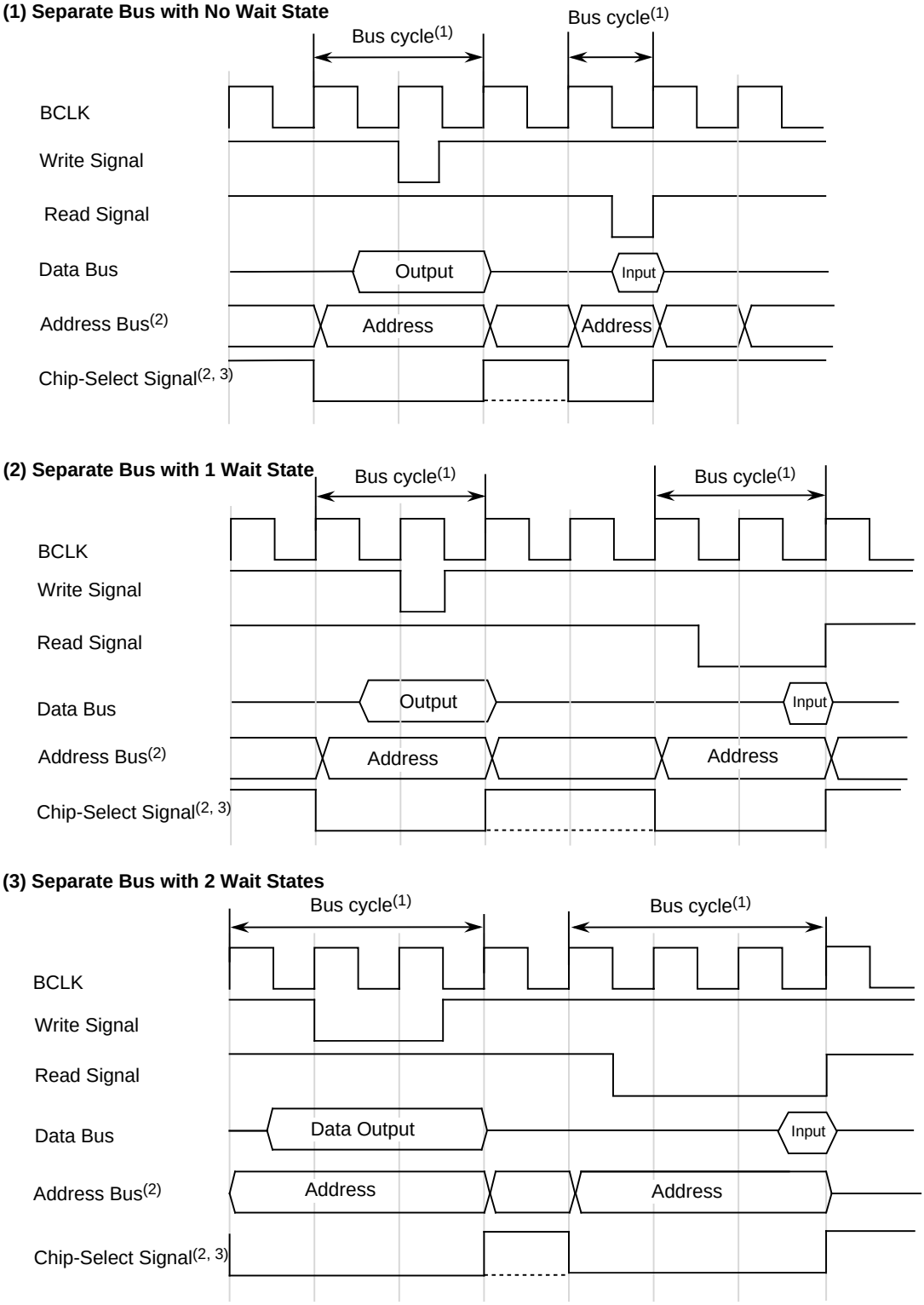
NOTES:
1. When using the multiplexed bus, "2 waits" is selected even if the WCR register is set to "00_2" (no wait state) or "01_2" (1 wait state). "10_2" (2 wait states) and "11_2" (3 wait states) can be selected.
2. When using the separate bus, the read bus runs one BCLK cycle and the write bus runs two BCLK cycles (1 wait state) if the WCR register is set to "00_2".

Figure 7.3 WCR Register

Table 7.5 Software Wait State and Bus Cycle

Space	External Bus Status	PM1 Register		WCR Register	Bus Cycle
		PM13 Bit	PM12 Bit	WCRj to WCRi Bits	
SFR	———	0	———	———	2 BCLK cycles
		1			3 BCLK cycles
Internal ROM/RAM	———	———	0	———	1 BCLK cycle
			1		2 BCLK cycles
External Memory	Separate Bus	———	———	00_2	Read :1 BCLK cycle Write : 2 BCLK cycles
				01_2	2 BCLK cycles
				10_2	3 BCLK cycles
				11_2	4 BCLK cycles
	Multiplexed Bus	———	———	00_2	3 BCLK cycle
				01_2	3 BCLK cycles
				10_2	3 BCLK cycles
				11_2	4 BCLK cycles

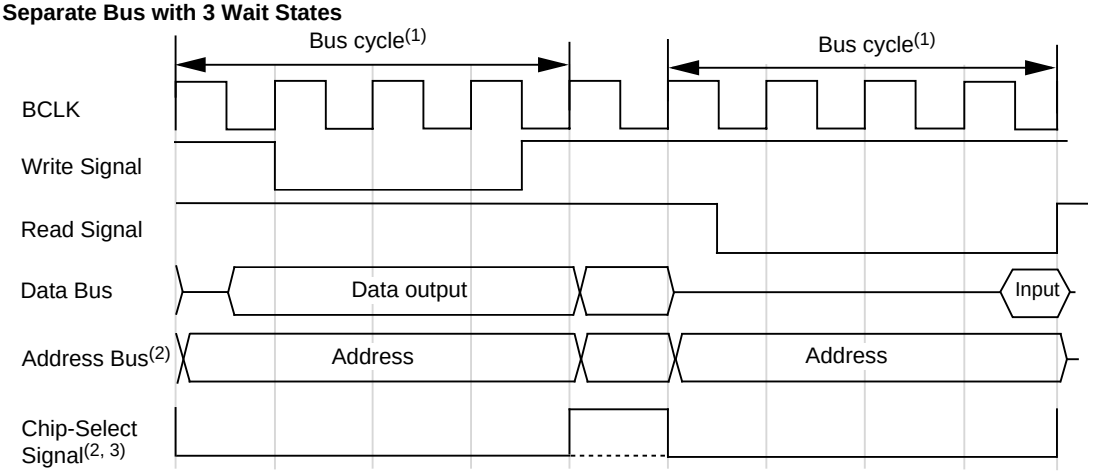
i = 0, 2, 4, 6 j = i + 1



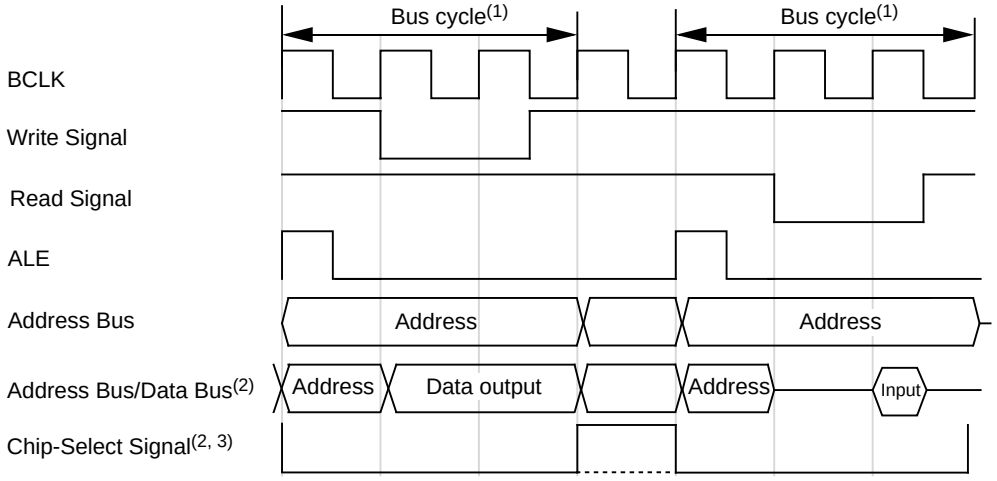
NOTES:
1. This example illustrates bus cycle length. Read cycle and write cycle may occur consecutively.
2. The address bus and chip-select signal may be extended depending on CPU state such as an instruction queue buffer.
3. When the microcomputer continuously accesses the same external space (same $\overline{CS}$ area), the chip-select signal may be output continuously.

Figure 7.4 External Bus Operation with Software Wait State (1)

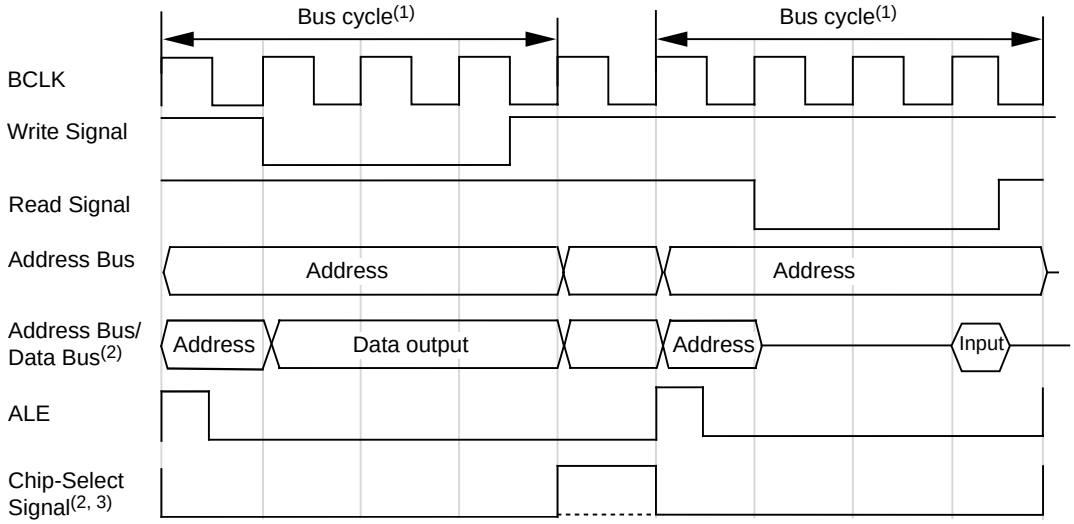
(1) Separate Bus with 3 Wait States



(2) Multiplexed Bus with 2 Wait States



(3) Multiplexed Bus with 3 Wait States



NOTES:
1. This example illustrates bus cycle length. Read cycle and write cycle may occur consecutively.
2. The address bus and chip-select signal may be extended depending on CPU state such as an instruction queue buffer.
3. When the microcomputer continuously accesses the same external space (same $\overline{CS}$ area), the chip-select signal may be output continuously.

Figure 7.5 External Bus Operation with Software Wait State (2)

7.2.5 ALE Signal

The ALE signal latches an address of the multiplexed bus. Latch an address on the falling edge of the ALE signal. The PM15 to PM14 bits in the PM1 register determine the output pin for the ALE signal. The ALE signal is output to an internal space and external space.

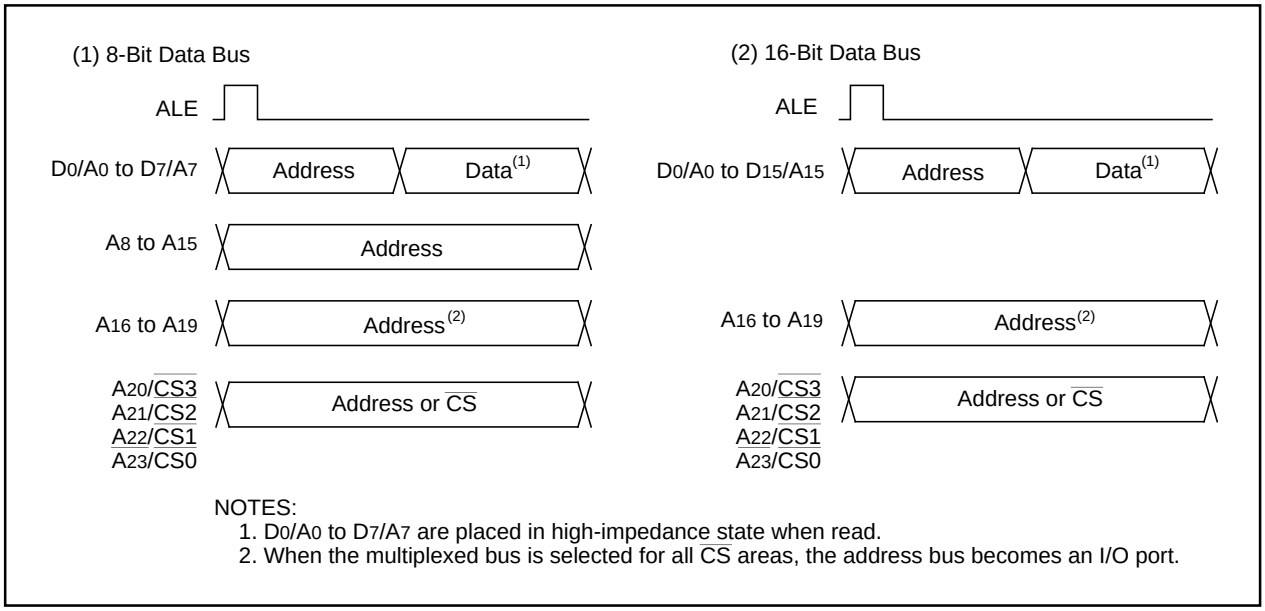


Figure 7.6 ALE Signal and Address/Data Bus

7.2.6 RDY Signal

The RDY signal facilitates access to external devices which need longer access time. When an "L" signal is applied to the RDY pin on the falling edge of last BCLK of the bus cycle, wait states are inserted into the bus cycle. When an "H" signal is applied to the RDY pin on the falling edge of the BCLK, the bus cycle starts running again.

Table 7.6 lists microcomputer states when the RDY signal inserts wait states into the bus cycle. Figure 7.7 shows an example of the RD signal extended by the RDY signal.

Table 7.6 Microcomputer States in a Wait State(1)

Item	State
Oscillation	On
RD Signal, WR Signal, Address Bus, CSi (i=0 to 3), Data Bus, ALE Signal, HLDA, Programmable I/O Ports	Maintains the same state as when RDY signal was received
Internal Peripheral Circuits	On

NOTES:

1. The RDY signal cannot be accepted immediately before software wait states are inserted.

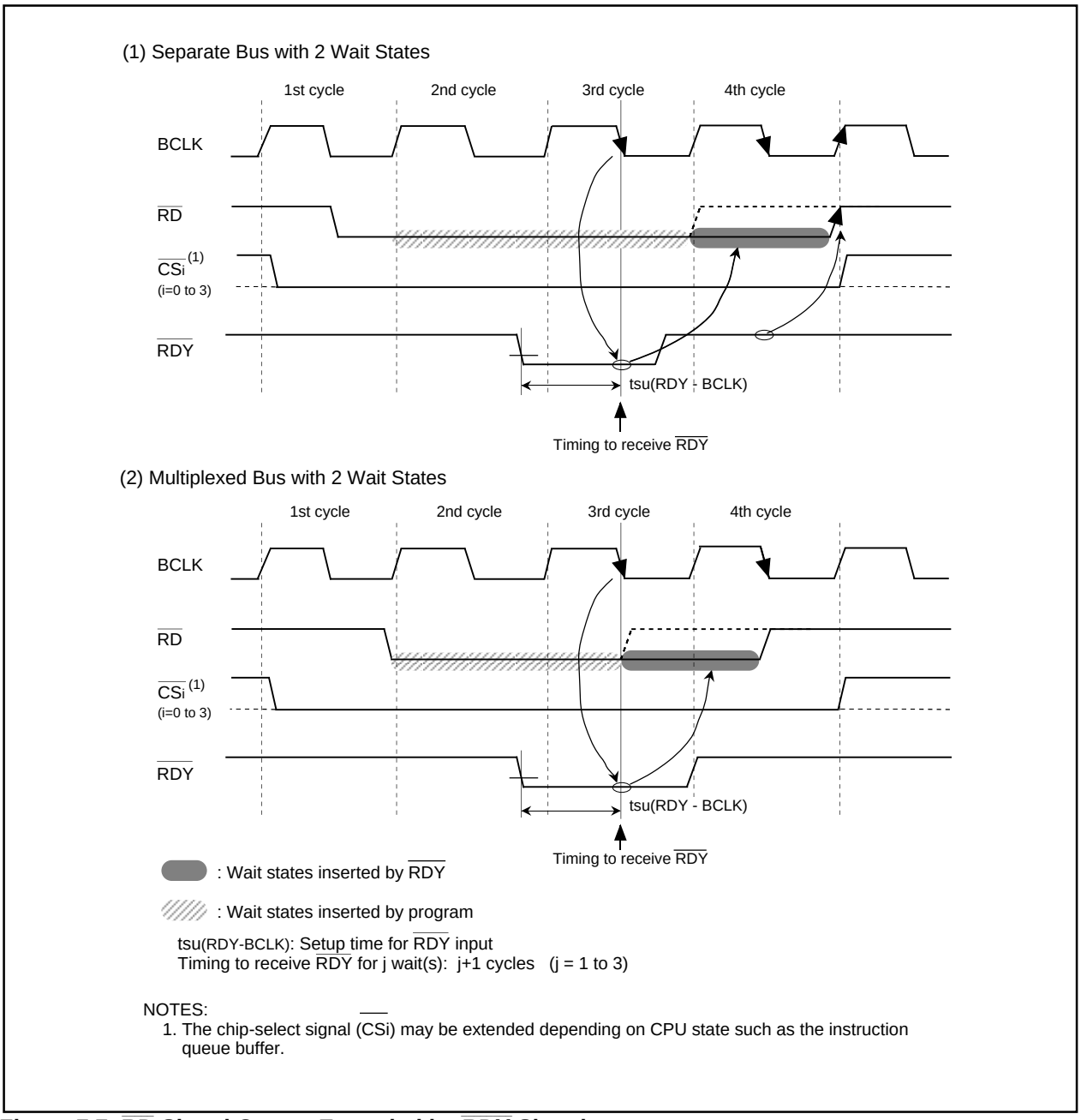


Figure 7.7 RD Signal Output Extended by RDY Signal

7.2.7 HOLD Signal

The HOLD signal transfers bus privileges from the CPU to external circuits. When an "L" signal is applied to the HOLD pin , the microcomputer enters a hold state after bus access is completed. While the HOLD pin is held "L", the microcomputer is in a hold state and the HLDA pin outputs an "L" signal. Table 7.7 shows the microcomputer status in a hold state.

Bus is used in the following order of priority: HOLD, DMAC, CPU.

HOLD > DMAC > CPU

Figure 7.8 Order of Bus Priority

Table 7.7 Microcomputer Status in a Hold State

Item	Status
Oscillation	On
$\overline{RD}$ Signal, $\overline{WR}$ Signal, Address Bus, Data Bus, $\overline{BHE}$, $\overline{CS0}$ to $\overline{CS3}$	High-impedance
Programmable I/O Ports: P0 to P15	Maintains the same state as when $\overline{HOLD}$ signal is received
$\overline{HLDA}$	Output "L"
Internal Peripheral Circuits	On (excluding the watchdog timer)
ALE Signal	Output "L"

7.2.8 External Bus State when Accessing Internal Space

Table 7.8 shows external bus states when an internal space is accessed.

Table 7.8 External Bus State when Accessing Internal Space

Item		State when accessing SFR, internal ROM and internal RAM
Address bus		Holds an address of an external space accessed just before
Data Bus	When Read	High-impedance
	When Write	High-impedance
$\overline{RD}$, $\overline{WR}$, $\overline{WRL}$, $\overline{WRH}$		Output "H"
$\overline{BHE}$		Holds state of external space last accessed
$\overline{CS0}$ to $\overline{CS3}$		Output "H"
ALE		Output ALE

7.2.9 BCLK Output

The CPU clock operates the CPU. When combining the PM07 bit in the PM0 register set to "0" (BCLK output) and the CM01 to CM00 bits in the CM0 register set to "00$_2$", the CPU clock signal is output from P5$_3$ as BCLK.

No BCLK is output in single-chip mode. Refer to **8. Clock Generating Circuit** for details.

7.2.10 DRAM Control Signals ($\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$ and $\overline{DW}$)

The DRAM control signals control the DRAM. The DRAM control signals are output when the DRAM area, determined by the AR0 to AR2 bits in the DRAMCONT register, is output. Table 7.9 lists each signal operation.

Table 7.9 $\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$ and $\overline{DW}$ Signals

Data Bus Width	$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{DW}$	Data Bus State
16 bits	L	L	L	H	Read data from both even and odd addresses
	L	L	H	H	Read 1-byte data from even address
	L	H	L	H	Read 1-byte data from odd address
	L	L	L	L	Write data to both even and odd addresses
	L	L	H	L	Write 1-byte data to even address
	L	H	L	L	Write 1-byte data to odd address
8 bits	L	L	Not used	H	Read 1-byte data
	L	L	Not used	L	Write 1-byte data

8. Clock Generating Circuit

8.1 Types of Clock Generating Circuits

Four circuits are incorporated to generate the system clock signal :

- Main clock oscillation circuit
- Sub clock oscillation circuit
- On-chip oscillator
- PLL frequency synthesizer

Table 8.1 lists specifications of the clock generating circuit. Figure 8.1 shows a block diagram of the clock generating circuit. Figures 8.2 to 8.8 show registers controlling the clock.

Table 8.1 Clock Generating Circuit Specifications

Item	Main Clock Oscillation Circuit	Sub Clock Oscillation Circuit	On-chip Oscillator	PLL Frequency Synthesizer
Use	• CPU clock source • Peripheral function clock source	• CPU clock source • Timer A and B clock source	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source
Clock Frequency	Up to 32 MHz	32.768 kHz	Approximatly 1 MHz	20 MHz to 32 MHz (See Table 8.2)
Connectable Oscillator or Additional Circuit	• Ceramic resonator • Crystal oscillator	• Crystal oscillator	———	• Low pass filter
Pins for Oscillator or for Additional Circuit	XIN, XOUT	XCIN, XCOUT	———	VCOUT (connect to low pass filter) P86 (connect to Vss)
Oscillation Stop/ Restart Function	Available	Available	Available	Available
Oscillator State After Reset	Oscillating	Stopped	Stopped	Stopped
Other	External clock can be input	External clock can be input. The PLL frequency synthesizer cannot be used when using the sub clock oscillation circuit.	When the main clock stops oscillating, the on-chip oscillator starts oscillating automatically and becomes the clock source for the CPU and peripheral functions	The sub clock cannot be used when using the PLL frequency synthesizer

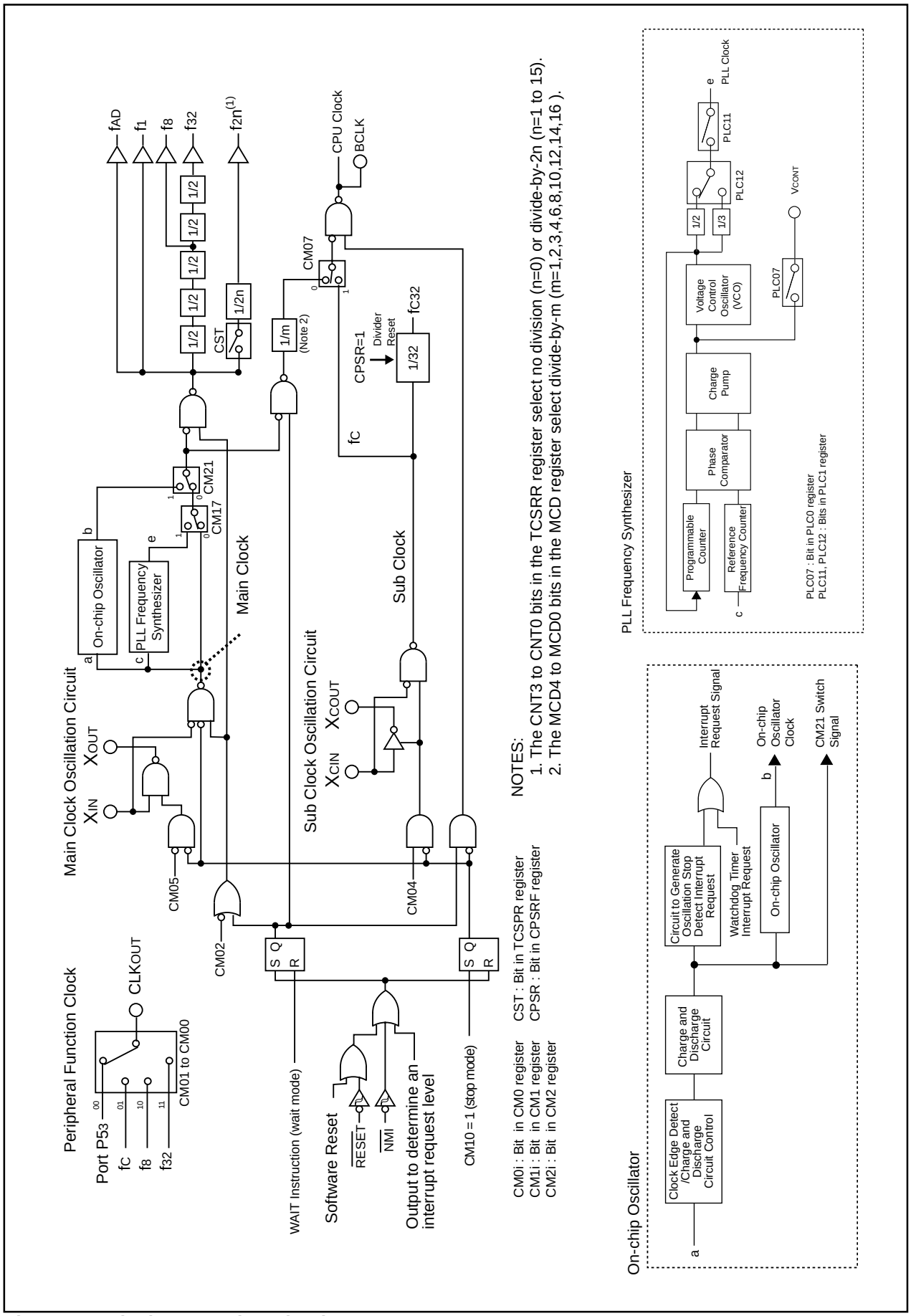


Figure 8.1 Clock Generating Circuit

System Clock Control Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
				1			

Symbol	Address	After Reset
CM0	0006_{16}	$0000\ X000_2$

Bit Symbol	Bit Name	Function	RW
CM00	Clock Output Function Select Bit(2)	b1 b0 0 0 : I/O port P5$_3$ 0 1 : Outputs fc 1 0 : Outputs f$_8$ 1 1 : Outputs f$_{32}$	RW
CM01			RW
CM02	In Wait Mode, Peripheral Function Clock Stop Bit	0 : Peripheral clock does not stop in wait mode 1 : Peripheral clock stops in wait mode(3)	RW
(b3)	Reserved Bit	Set to "1"	RW
CM04	Port Xc Switch Bit	0 : I/O port function 1 : XCIN-XCOUT oscillation function(4)	RW
CM05	Main Clock (XIN-XOUT) Stop Bit(5)	0 : Main clock oscillates 1 : Main clock stops(6)	RW
CM06	Watchdog Timer Function Select Bit	0 : Watchdog timer interrupt 1 : Reset(7)	RW
CM07	System Clock Select Bit(8)	0 : Selects XIN - XOUT 1 : Selects XCIN - XCOUT	RW

NOTES:
1. Rewrite the CM0 register after the PRC0 bit in the PRCR register is set to "1" (write enable).
2. When the PM07 bit in the PM0 register is set to "0" (BCLK output), set the CM01 to CM00 bits to "00_2". When the PM15 to PM14 bits in the PM1 register is set to "01_2" (ALE output to P5$_3$), set the CM01 to CM00 bits to "00_2". When the PM07 bit is set to "1" (function selected in the CM01 to CM00 bits) in microprocessor or memory expansion mode, and the CM01 to CM00 bits are set to "00_2", an "L" signal is output from port P5$_3$ (port P5$_3$ does not function as an I/O port).
3. fc$_{32}$ does not stop. When the CM02 bit is set to "1", the PLL clock cannot be used in wait mode.
4. When setting the CM04 bit to "1" (XCIN-XCOUT oscillation), set the PD8_7 to PD8_6 bits to "00_2" (with port P8$_7$ and P8$_6$ input mode) and the PU25 bit in the PUR2 register to "0" (no pull-up).
5. When entering the low-power consumption mode or on-chip oscillator low-power consumption mode, the CM05 bit stops the main clock. The CM05 bit cannot detect whether the main clock stops or not. To stop the main clock, set the CM05 bit to "1" after the CM07 bit is set to "1" with a stable sub clock oscillation or after the CM21 bit in the CM2 register is set to "1" (on-chip oscillator clock). When the CM05 bit is set to "1", XOUT becomes "H". The internal feedback resistance remains ON. XIN is pulled up to XOUT ("H" level) via the feedback resistance.
6. When the CM05 bit is set to "1", the MCD register is set to "08_{16}" (divide-by-8 mode). In on-chip oscillation mode, the MCD register is not divided by eight even if the CM05 bit terminates XIN-XOUT.
7. Once the CM06 bit is set to "1", it cannot be set "0" by program.
8. After the CM04 bit is set to "1" with a stable sub clock oscillation, set the CM07 bit to "1" from "0". After the CM05 bit is set to "0" with a stable main clock oscillation, set the CM07 bit to "0" from "1". Do not set the CM07 bit and CM04 or CM05 bits simultaneously.

Figure 8.2 CM0 register

System Clock Control Register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0
	0	1	0	0	0	0	

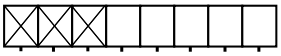
Symbol	Address	After Reset
CM1	0007_{16}	$0010\ 0000_2$

Bit Symbol	Bit Name	Function	RW
CM10	All Clock Stop Control Bit(2)	0 : Clock oscillates 1 : All clocks stop (stop mode)(3)	RW
____ (b4 - b1)	Reserved Bit	Set to "0"	RW
____ (b5)	Reserved Bit	Set to "1"	RW
____ (b6)	Reserved Bit	Set to "0"	RW
CM17	CPU Clock Select Bit 2	0 : Main clock(4) 1 : PLL clock(4)	RW

NOTES:
1. Rewrite the CM1 register after the PRC0 bit in the PRCR register is set to "1" (write enable).
2. When the CM10 bit is set to "1", XOUT becomes "H" and the internal feedback resistance is disabled. XIN, XCIN and XCOUT are placed in high-impedance states.
3. When the CM10 bit is set to "1", the MCD register is set to "08_{16}" (divide-by-8 mode). When the CM20 bit is set to "1" (oscillation stop detect function enabled) or the CM21 bit to "1" (on-chip oscillator selected), do not set the CM10 bit to "1".
4. CM17 bit is enabled only when the CM21 bit in the CM2 register is set to "0". Use the procedure shown in Figure 8.13 to set the CM17 bit to "1".

Figure 8.3 CM1 Register

Main Clock Division Register(1)



Symbol	Address	After Reset
MCD	$000C_{16}$	$XXX01000_2$

Bit Symbol	Bit Name	Function	RW
MCD0	Main Clock Division Select Bit(2, 4)	b4 b3 b2 b1 b0 1 0 0 1 0 : Divide-by-1(no division) mode 0 0 0 1 0 : Divide-by-2 mode 0 0 0 1 1 : Divide-by-3 mode 0 0 1 0 0 : Divide-by-4 mode 0 0 1 1 0 : Divide-by-6 mode 0 1 0 0 0 : Divide-by-8 mode 0 1 0 1 0 : Divide-by-10 mode 0 1 1 0 0 : Divide-by-12 mode 0 1 1 1 0 : Divide-by-14 mode 0 0 0 0 0 : Divide-by-16 mode (Note 3)	RW
MCD1			RW
MCD2			RW
MCD3			RW
MCD4			RW
____ (b7 - b5)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. Rewrite the MCD register after the PRC0 bit in the PRCR register is set to "1" (write enable).
2. While the microcomputer is in stop mode or low-power consumption mode, the MCD register is set to "08_{16}" (divide-by-8 mode).
   In on-chip oscillator mode, divide-by-8 mode cannot be entered even if the CM05 bit in the CM0 register is set to "1"(X_{IN}-X_{OUT} stopped).
3. Do not set to bit combinations not listed above.
4. Access CAN-associated register addresses (addresses $01E0_{16}$ to 0245_{16}) after setting the MCD register to "12_{16}" (no division mode).

Figure 8.4 MCD Register

Oscillation Stop Detect Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

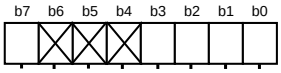
Symbol	Address	After Reset
CM2	000D16	0016

Bit Symbol	Bit Name	Function	RW
CM20	Oscillation Stop Detect Enable Bit	0: Disables oscillation stop detect function 1: Enables oscillation stop detect function	RW
CM21	CPU Clock Select Bit(2, 3)	0: Clock selected by the CM17 bit 1: On-chip oscillator clock	RW
CM22	Oscillation Stop Detect Flag(4)	0: Main clock does not stop 1: Detects main clock stop	RW
CM23	XIN Clock Monitor Flag(5)	0: Main clock oscillates 1: Main clock stops	RO
____ (b7 - b4)	Reserved Bit	Set to "0"	RW

NOTES:
1. Rewrite the CM2 register after the PRC0 bit in the PRCR register is set to "1" (write enable).
2. When the main clock oscillation stop is detected while the CM20 bit is set to "1" (oscillation stop detect function enabled), the CM21 bit is set to "1". Although the main clock starts oscillating, the CM21 bit is not set to "0". When the main clock is used as a CPU clock source after the main clock resumes oscillation, set the CM21 bit to "0" by program.
3. When the CM20 bit is set to "1" (oscillation stop detect function enabled) and the CM22 bit is set to "1", do not set the CM21 bit to "0".
4. When a main clock stop is detected, the CM22 bit is set to "1". The CM22 bit can only be set to "0", not "1", by program.
   If the CM22 bit is set to "0" by program while the main clock is stopped, the CM22 bit cannot be set to "1" until the next main clock stop is detected.
5. Determine the main clock state by reading the CM23 bit several times after the oscillation stop interrupt is generated.

Figure 8.5 CM2 Register

Count Source Prescaler Register

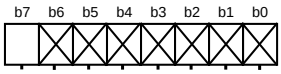


Symbol	Address	After Reset
TCSPR	035F16	0XXX 00002

Bit Symbol	Bit Name	Function	RW
CNT0	Division Rate Select Bit(1)	If setting value is n, f2n is divided the main clock, on-chip oscillator clock or PLL clock by 2n. When n is set to "0", no division is selected.	RW
CNT1			RW
CNT2			RW
CNT3			RW
____ (b6 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
CST	Operation Enable Bit	0: Divider stops 1: Divider starts	RW

NOTES:
1. Rewrite the CNT3 to CNT0 bits after the CST bit is set to "1".

Clock Prescaler Reset Flag



Symbol	Address	After Reset
CPSRF	034116	0XXX XXXX2

Bit Symbol	Bit Name	Function	RW
____ (b6 - b0)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
CPSR	Clock Prescaler Reset Flag	When the CPSR bit is set to "1", fC divided by 32 is reset. When read, its content is "0".	RW

Figure 8.6 TCSPR and CPSRF Registers

PLL Control Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
	0	0	1	X			

Symbol	Address	After Reset
PLC0	037616	0011 X1002

Bit Symbol	Bit Name	Function	RW
PLC00	Programmable Counter Select Bit(2)	See Table 8.2	RW
PLC01			RW
PLC02			RW
____ (b3)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
____ (b4)	Reserved Bit(2)	Set to "1"	RW
____ (b5)	Reserved Bit(2)	Set to "0"	RW
____ (b6)	Reserved Bit	Set to "0"	RW
PLC07	Operation Enable Bit(3, 4)	0: PLL is Off 1: PLL is On	RW

NOTES:
1. Rewrite the PLC0 register after the PRC0 bit in the PRCR register is set to "1" (write enable).
2. Set these bits when the PLC07 bit is set to "0". Once these bits are set, they cannot be changed.
3. To use the PLL function, the PD8_7 bit in the PD8 register is set to "0" (input) and the CM04 bit in the CM0 register is set to "0" (I/O port). Set the PD8_6 bit in the PD8 register to "0" (input) before connecting P86 to Vss.
4. Before the microcomputer enters wait or stop mode, set the CM17 bit to "0" (main clock as CPU clock source), the PLC07 bit to "0" and PLV00 bit to "0" (cut off power to PLL) in this order.

VDC Control Register for PLL(1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	0	

Symbol	Address	After Reset
PLV	001716	XXXX XX012

Bit Symbol	Bit Name	Function	RW
PLV00	PLL VDC Enable Bit(2)	0 : Cut off power to PLL 1 : Power to PLL	RW
____ (b1)	Reserved Bit	Set to "0"	RW
____ (b7 - b2)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. Rewrite the PLV register after the PRC3 bit in the PRCR register is set to "1" (write enable).
2. Before the microcomputer enters wait or stop mode, set the CM17 bit to "0" (main clock as CPU clock source), the PLC07 bit to "0" (PLL off) and PLV00 bit to "0" (cut off power to PLL) in this order.

Figure 8.7 PLC0 and PLV Registers

PLL Control Register 1(1, 2)

b7	b6	b5	b4	b3	b2	b1	b0
				0			0

Symbol	Address	After Reset
PLC1	0377_{16}	$XXXX\ 0000_2$

Bit Symbol	Bit Name	Function	RW
____ (b0)	Reserved Bit	Set to "0"	RW
PLC11	PLL Clock Division Enable Bit(3)	0 : Disables the PLL clock to be divided 1 : Enables the PLL clock to be divided	RW
PLC12	PLL Clock Division Switch Bit(4)	0 : Divide-by-2 1 : Divide-by-3	RW
____ (b3)	Reserved Bit	Set to "0"	RW
____ (b7 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. Rewrite the PLC1 register after the PRC0 bit in the PRCR register is set to "1" (write enable).
2. Rewrite the PLC1 register after the CM17 bit in the CM1 register is set to "0" (main clock) .
3. When the CM21 bit in the CM2 register is set to "0" (clock selected by the CM17 bit), if the PLC11 bit is set to "1" before the CM17 bit is set to "1" (PLL clock as CPU clock source), the PLL clock divided-by-2 or divided-by-3 becomes the clock source of the CPU clock and peripheral function clock.
4. Do not rewrite the PLC12 bit if the PLL clock is the CPU clock source.

Figure 8.8 PLC1 Register

8.1.1 Main Clock

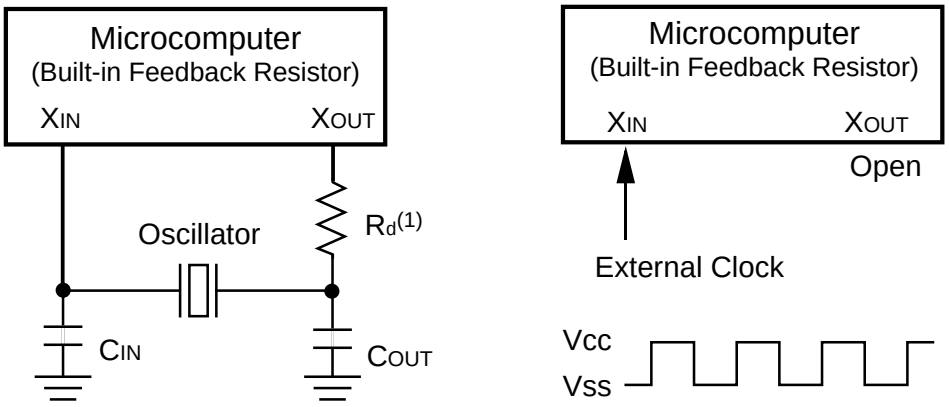
Main clock oscillation circuit generates the main clock. The main clock becomes a clock source for the CPU clock and peripheral function clock.

The main clock oscillation circuit is configured by connecting an oscillator or resonator between the XIN and XOUT pins. The circuit has a built-in feedback resistor. The feedback resistor is separated from the oscillation circuit in stop mode to reduce power consumption. The external clock can be applied to the XIN pin in the main clock oscillation circuit. Figure 8.9 shows an example of a main clock circuit connection. Circuit constants vary with each oscillator. Use the circuit constant recommended by each oscillator manufacturer.

The main clock divided-by-eight becomes the CPU clock after reset.

To reduce power consumption, set the CM05 bit in the CM0 register to "1" (oscillation stop in main clock oscillation circuit) after switching the CPU clock source to the sub clock or on-chip oscillator clock. In this case, XOUT becomes "H". XIN is pulled up by XOUT via the feedback resistor which remains on. When an external clock is input to the XIN pin, the main clock does not stop even if the CM05 bit is set to "1". Terminate main clock operation externally if necessary.

All clocks, including the main clock, stop in stop mode. Refer to **8.5 Power Consumption Control** for details.



NOTES:
1. Place a damping resistor if required. The resistor varies depending on the oscillator setting. Use values recommended by each oscillator manufacturer. Place a feedback resistor between XIN and XOUT if the oscillator manufacturer recommends placing the resistor externally.

Figure 8.9 Main Clock Circuit Connection

8.1.2 Sub Clock

Sub clock oscillation circuit generates the sub clock. The sub clock becomes a clock source for the CPU clock and a count source for the timers A and B. The same frequency fc as the sub clock can be output from the CLKOUT pin.

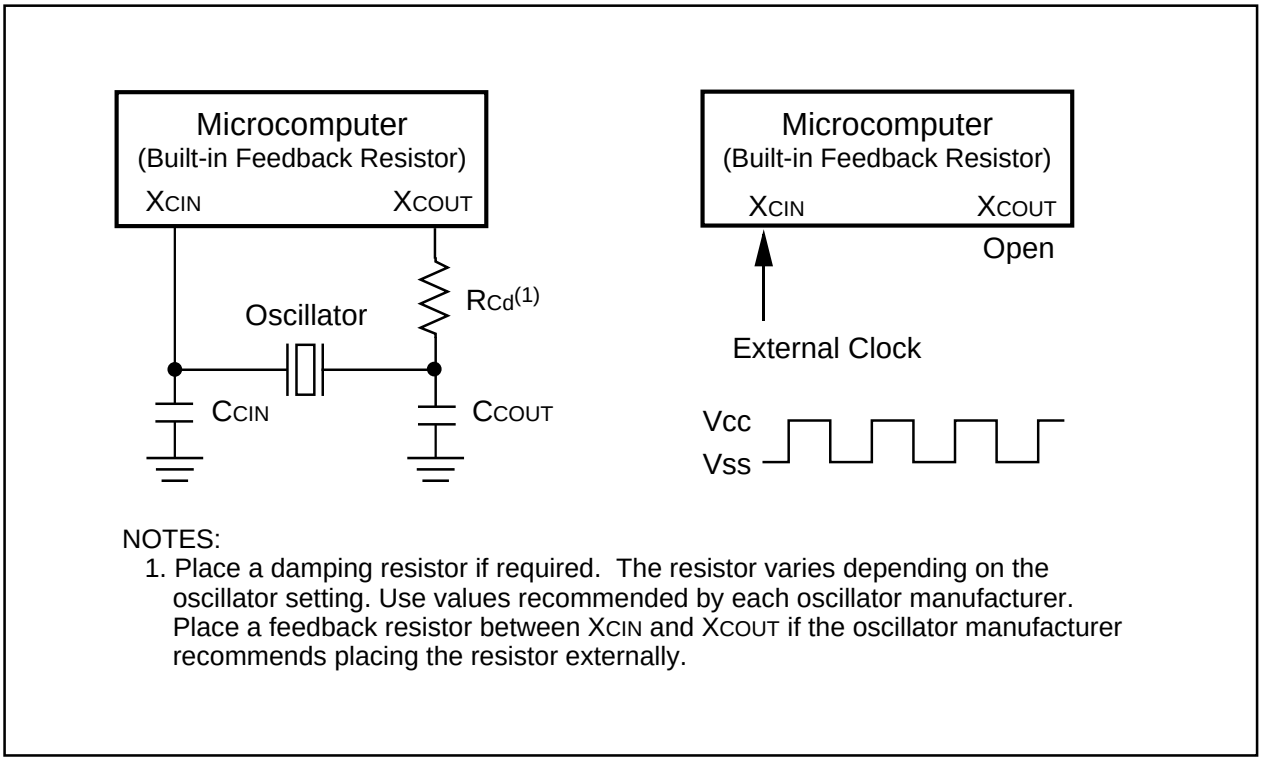
The sub clock oscillation circuit is configured by connecting a crystal oscillator between the XCIN and XCOUT pins. The circuit has a built-in feedback resistor. The feedback resistor is separated from the oscillation circuit in stop mode to reduce power consumption. The external clock can be applied to the XCIN pin. Figure 8.10 shows an example of a sub clock circuit connection. Circuit constants vary with each oscillator. Use the circuit constant recommended by each oscillation manufacturer.

The sub clock stops after reset. The feedback resistor is separated from the oscillation circuit. When the PD8_6 and PD8_7 bits in the PD8 register are set to "0" (input mode) and the PU25 bit in the PUR2 register is set to "0" (no pull-up), set the CM04 bit in the CM0 register to "1" (XCIN-XCOUT oscillation function). The sub clock oscillation circuit starts oscillating. To apply the external clock to the XCIN pin, set the CM04 bit to "1" when the PD8_6 bit is set to "0" and the PU25 bit to "0". The clock applied to the XCIN pin becomes the clock source for the sub clock.

When the CM07 bit of CM0 register is set to "1" (XCIN-XCOUT select) after the sub clock oscillation has stabilized, the sub clock becomes the CPU clock.

All clocks, including the sub clock, stop in stop mode. Refer to **8.5 Power Consumption Control** for details.

XCIN shares pins with VCONT and XCOUT shares pins with P86. The sub clock and PLL frequency synthesizer cannot be used simultaneously.



NOTES:
1. Place a damping resistor if required. The resistor varies depending on the oscillator setting. Use values recommended by each oscillator manufacturer. Place a feedback resistor between XCIN and XCOUT if the oscillator manufacturer recommends placing the resistor externally.

Figure 8.10 Sub Clock Connection Circuit

8.1.3 On-chip Oscillator Clock

On-chip oscillator generates the on-chip oscillator clock. The 1MHz on-chip oscillator clock becomes a clock source for the CPU clock and peripheral function clock.

The on-chip oscillator clock stops after reset. When the CM21 bit in the CM2 register is set to "1" (on-chip oscillator clock), the on-chip oscillator starts oscillating. Instead of the main clock, the on-chip oscillator clock becomes the clock source for the CPU clock and peripheral function clock.

8.1.3.1 Oscillation Stop Detect Function

When the main clock is terminated by external factors, the on-chip oscillator automatically starts oscillating to generate another clock.

When the CM 20 bit is set to "1" (oscillation stop detect function enabled), the oscillation stop detect interrupt request is generated as soon as the main clock stops. Simultaneously, the on-chip oscillator starts oscillating. The on-chip oscillator clock takes place of the main clock as the clock source for the CPU clock and peripheral function clock. Associated bits are set as follows:

- CM21 bit = 1 (on-chip oscillator clock becomes the clock source of the CPU clock.)
- CM22 bit = 1 (main clock stop is detected.)
- CM23 bit = 1 (main clock stops) (See **Figure 8.15**)

8.1.3.2 How to Use Oscillation Stop Detect Function

- The oscillation stop detect interrupt shares vectors with the watchdog timer interrupt. When both oscillation stop detect interrupt and watchdog timer interrupt are used, read the CM22 bit with an interrupt processing program to determine which interrupt request has been generated.
- When the main clock resumes running after an oscillation stop is detected, set the main clock as the clock source for the CPU clock and peripheral function clock. Figure 8.11 shows the procedure to switch the on-chip oscillator clock to the main clock.
- In low-speed mode, when the main clock is stopped by setting the CM20 bit to "1", the oscillation stop detect interrupt request is generated. Simultaneously, the on-chip oscillator starts oscillating. The sub clock remains the CPU clock. The on-chip oscillator clock becomes the clock source for the peripheral function clock.
- To enter wait mode while the oscillation stop detect interrupt function is in use, set the CM02 bit to "0" (peripheral function clock does not stop in wait mode).
- When the oscillation stop detect interrupt request is generated in wait mode, wait mode cannot be exited by the oscillation stop detect interrupt. After the microcomputer exits wait mode, the oscillation stop detect interrupt is acknowledged first, followed by the interrupt used to exit wait mode.
- The oscillation stop detect function is provided to handle main clock stop caused by external factors. If the main clock is terminated by program in stop mode or the CM05 bit is set to "1" (main clock oscillation stop), set the CM20 bit to "0" (oscillation stop detect function disabled).
- When the main clock frequency is 2 MHz or less, the oscillation stop detect function is not available. Set the CM20 bit to "0".

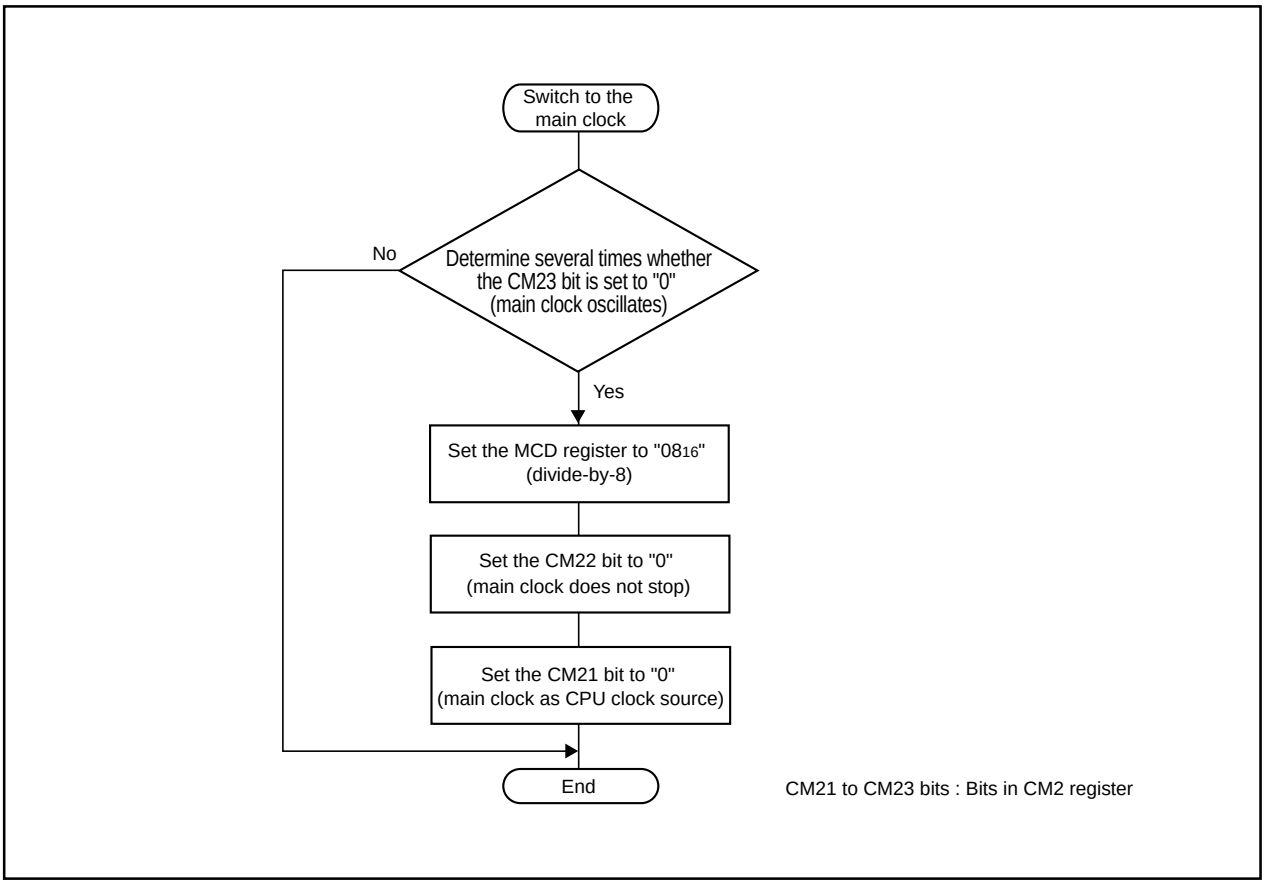


Figure 8.11 Switching Procedure from On-chip Oscillator Clock to Main Clock

8.1.4 PLL Clock

The PLL frequency synthesizer generates the PLL clock based on the main clock. The PLL clock can be used as a clock source for the CPU clock or peripheral function clock.

Connect a resistor and capacitor to the V_{CONT} pin when using the PLL frequency synthesizer.

Set the PD8_6 and PD8_7 bits in the PD8 register to "0" (input mode) and the CM04 bit to "0" (the X_{CIN} and X_{COUT} pins as ports). After that, connect the V_{CONT} pin, the $P8_6$ pin, and the V_{SS} pin to the circuit as is shown in Figure 8.12. Set the PLV00 bit in the PLV register to "1" (power to PLL).

The PLL frequency synthesizer stops after reset. When the PLC07 bit is set to "1" (PLL on), the PLL frequency synthesizer starts operating. Wait 20 ms (5 V operation) to 50 ms (3.3 V operation) for the PLL clock to stabilize.

The PLL clock can either be the clock output from the voltage controlled oscillator (VCO) divided-by-2 or divided-by-3.

When the PLL clock is used as a clock source for the CPU clock or peripheral function clock, set each bit as is shown in Table 8.2. Figure 8.13 shows the procedure for using the PLL clock as the CPU clock source.

When the microcomputer enters wait or stop mode, set the CM17 bit to "0" (main clock as CPU clock source). Set the PLC07 bit in the PLC0 register to "0" (PLL off) and the PLV00 bit to "0" (no power to PLL) before the microcomputer enters wait or stop mode.

The V_{CONT} and $P8_6$ pins share pins with X_{CIN} and X_{COUT} pins. When the PLL frequency synthesizer is being used, the sub clock cannot be used.

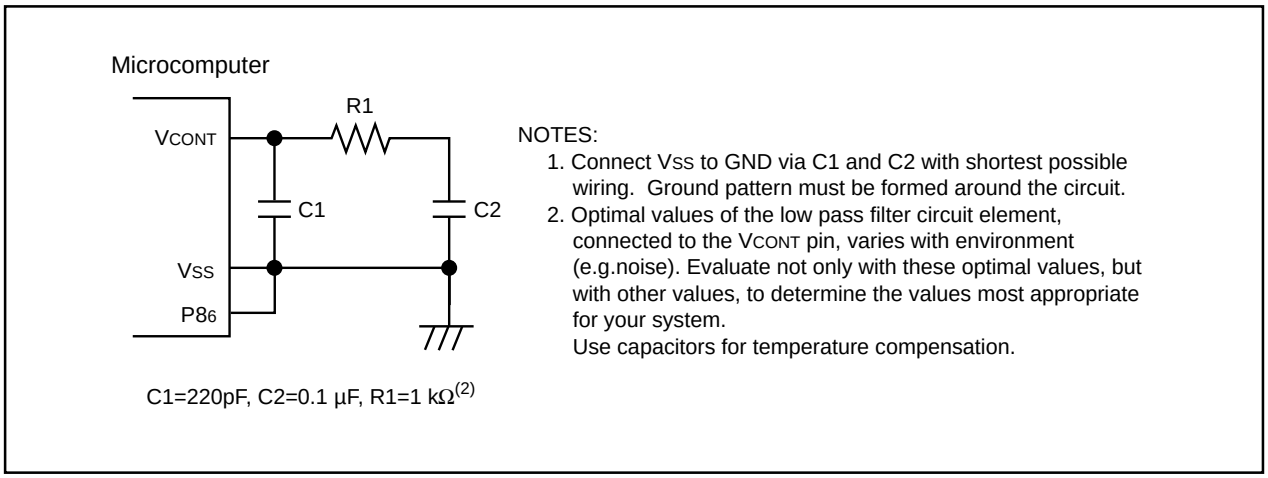


Figure 8.12 External Circuit with PLL Frequency Synthesizer

Table 8.2 Bit Settings to Use PLL Clock as CPU Clock Source

f(XIN)	PLC0 Register			PLC1 Register	PLL Clock
	PLC02	PLC01	PLC00	PLC12	
10MHz	0	1	1	0	30 MHz
				1	20 MHz
8MHz	1	0	0	0	32MHz
				1	21.3MHz

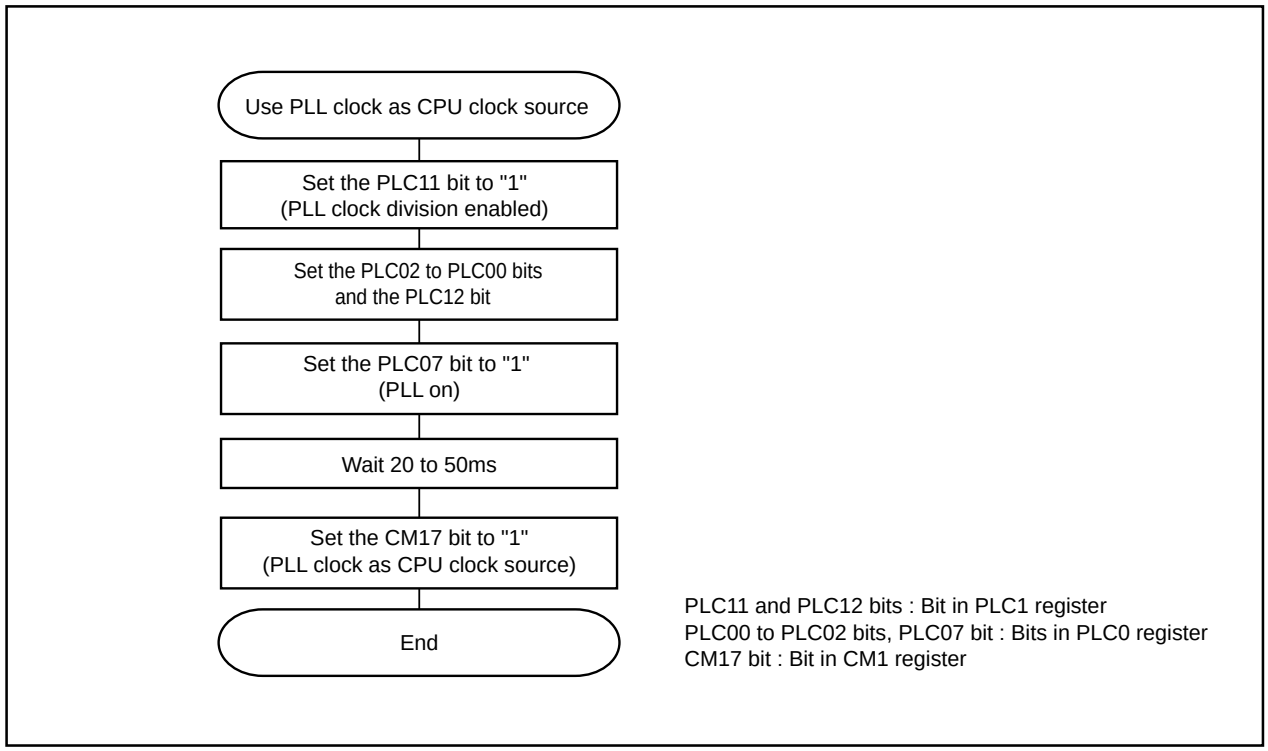


Figure 8.13 Procedure to Use PLL Clock as CPU Clock Source

8.2 CPU Clock and BCLK

The CPU operation clock is referred to as the CPU clock. The CPU clock is also the count source for the watchdog timer. After reset, the CPU clock is the main clock divided-by-8. In memory expansion or microprocessor mode, the clock having the same frequency as the CPU clock can be output from the BCLK pin as BCLK. Refer to **8.4 Clock Output Function** for details.

The main clock, sub clock, on-chip oscillator clock or PLL clock can be selected as a clock source for the CPU clock. Table 8.3 shows CPU clock source and bit settings.

When the main clock, on-chip oscillator clock or PLL clock is selected as a clock source of the CPU clock, the selected clock divided-by-1 (no division), -2, -3, -4, -6, -8, -10, -12, -14 or -16 becomes the CPU clock. The MCD register selects the clock division.

When the microcomputer enters stop mode or low-power consumption mode (except when the on-chip oscillator clock is the CPU clock), the MCD register is set to "08_{16}" (divide-by-8 mode). Therefore, when the main clock starts running, the CPU clock enters middle-speed mode (divide-by-8).

Table 8.3 CPU Clock Source and Bit Settings

CPU Clock Source	CM0 Register	CM2 Register	CM1 Register
	CM07	CM21	CM17
Main Clock	0	0	0
Sub Clock	1	0	0
On-chip Oscillator Clock	0	1	0
PLL Clock	0	0	1

8.3 Peripheral Function Clock

The peripheral function clock becomes the operation clock or count source for peripheral functions excluding the watchdog timer.

8.3.1 f_1, f_8, f_{32} and f_{2n}

f_1, f_8, f_{32} and f_{2n} are the main clock(1) or on-chip oscillator clock divided-by-1, -8, -32 ,or -2n (n=1 to 15. No division when n=0). The CM21 bit determines which clock is selected.

When the CM02 bit is set to "1" (peripheral function stops in wait mode) when entering wait mode, f_1, f_8, f_{32} and f_{2n} stop running. These clocks also stop in low-power consumption mode.

f_1, f_8 and f_{2n} are used as the operation clock for the serial I/O and the count source for timers A and B. The CNT3 to CNT0 bits in the TCSPR register selects a f_{2n} division. f_1 is also used as the operation clock for the intelligent I/O.

The CLK_{OUT} pin outputs f_8 and f_{32} . Refer to **8.4 Clock Output Function** for details.

8.3.2 f_{AD}

f_{AD} is the operation clock for the A/D convertor and has the same frequency as the main clock(1) and on-chip oscillator clock. The CM21 bit determines which clock is selected.

When the CM02 bit is set to "1" (peripheral function stop in wait mode) when entering wait mode, f_{AD} stops. f_{AD} also stops in low-power consumption mode.

NOTES:

1. When the CM17 bit is set to "1" (PLL clock as CPU clock source), the PLL clock is the main clock.

8.3.3 f_{C32}

f_{C32} is the sub clock divided by 32. f_{C32} is used for as a count source for the timers A and B. f_{C32} is available when the sub clock is running.

8.4 Clock Output Function

The CLK_{OUT} pin outputs f_C, f_8 or f_{32}.

In memory expansion and microprocessor modes, a clock having the same frequency as the CPU clock can be output from the BCLK pin as BCLK.

Table 8.4 lists CLK_{OUT} pin function in single-chip mode. Table 8.5 lists CLK_{OUT} pin functions in memory expansion and microprocessor modes.

Table 8.4 CLK_{OUT} Pin in Single-Chip Mode

PM0 Register (1)	CM0 Register (2)		CLK_{OUT} Pin Function
PM07	CM01	CM00	
—	0	0	$P5_3$ I/O port
1	0	1	Outputs fc
1	1	0	Outputs f_8
1	1	1	Outputs f_{32}

- : Can be set to either "0" or "1"

NOTES:

1. Rewrite the PM0 register after the PRC1 bit in the PRCR register is set to "1" (write enable)
2. Rewrite the CM0 register after the PRC0 bit in the PRCR register is set to "1" (write enable)

Table 8.5 BLCK/CLK_{OUT} Pin in Memory Expansion Mode and Microprocessor Mode

PM1 Register(1)		PM0 Register(1)	CM0 Register(2)		CLK_{OUT} Pin Function
PM15	PM14	PM07	CM01	CM00	
00_2, 10_2, 11_2,		0	0 (3)	0 (3)	Outputs BCLK
		1	0	0	Outputs "L" (not $P5_3$)
		1	0	1	Outputs fc
		1	1	0	Outputs f_8
		1	1	1	Outputs f_{32}
0	1	—	0 (3)	0 (3)	Outputs ALE

- : Can be set to either "0" or "1"

NOTES:

1. Rewrite the PM0 and PM1 register after the PRC1 bit in the PRCR register is set to "1" (write enable)
2. Rewrite the CM0 register after the PRC0 bit in the PRCR register is set to "1" (write enable)
3. When the PM07 bit is set to "0" (selected in the CM01 to CM00 bits) or the PM15 to PM14 bits are set to "01_2" ($P5_3$/BCLK), set the CM01 to CM00 bits to "00_2" (I/O port $P5_3$)

8.5 Power Consumption Control

Normal operation mode, wait mode and stop mode are provided as the power consumption control.

All mode states, except wait mode and stop mode, are called normal operation mode in this document.

Figure 8.14 shows a block diagram of status transition in wait mode and stop mode. Figure 8.15 shows a block diagram of status transition in all modes.

8.5.1 Normal Operation Mode

The normal operation mode is further separated into six modes.

In normal operation mode, the CPU clock and peripheral function clock are supplied to operate the CPU and peripheral function. The power consumption control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. When unnecessary oscillation circuits stop, power consumption is further reduced.

8.5.1.1 High-Speed Mode

The main clock(1) becomes the CPU clock and the clock source for the peripheral function clock. When the sub clock runs, f_{C32} can be used as a count source for the timers A and B.

8.5.1.2 Medium-Speed Mode

The main clock divided-by-2, -3, -4, -6, -8, -10, -12, -14, or -16 becomes the CPU clock. The main clock is a clock source for the peripheral function clock. When the sub clock runs, f_{C32} can be used as the count source for the timers A and B.

8.5.1.3 Low-Speed Mode

The sub clock becomes the CPU clock. The main clock is the count source for the peripheral function clock. f_{C32} can be used as the count source for the timers A and B.

8.5.1.4 Low-Power Consumption Mode

Low-power consumption mode is entered when the main clock stops in low-speed mode. The sub clock becomes the CPU clock. f_{C32} can be used as the count source for timers A and B. Only f_{C32} can be used as the peripheral function clock. In low-power consumption mode, the MCD register is set to "08_{16}" (divide-by-8 mode). Therefore, when the main clock resumes running, the microcomputer is in middle-speed mode (divide-by-8 mode).

8.5.1.5 On-chip Oscillator Mode

The on-chip oscillator clock divided-by-1(no division), -2, -3, -4, -6, -8, -10, -12, -14, or -16 becomes the CPU clock. The on-chip oscillator clock is the clock source for the peripheral function clock. When the sub clock runs, f_{C32} can be used as the count source for the timers A and B.

8.5.1.6 On-chip Oscillator Low-Power Consumption Mode

The microcomputer enters on-chip oscillator low-power consumption mode when the main clock stops in on-chip oscillator mode. The on-chip oscillator clock divided-by-1(no division), -2, -3, -4, -6, -8, -10, -12, -14, or -16 becomes the CPU clock. The on-chip oscillator clock is the clock source for the peripheral function clock. When the sub clock runs, f_{C32} can be used as the count source for the timers A and B.

Switch the CPU clock after the clock to be switched to stabilizes. Sub clock oscillation will take longer(2) to stabilize. Wait, by program, until the clock stabilizes.

To switch the on-chip oscillator to the main clock, enter medium-speed mode (divide-by-8) after the main clock is divided by eight in on-chip oscillator mode (MCD register=08_{16}).

Do not enter on-chip oscillator mode or on-chip oscillator low-power consumption mode from low-speed mode or low-power consumption mode and vice versa.

NOTES:

1. When the CM17 bit is set to "1" (PLL clock as CPU clock source), the PLL clock is the main clock .
2. Contact your oscillator manufacturer for oscillation stabilization time.

8.5.2 Wait Mode

In wait mode, the CPU clock stops. The CPU and watchdog timer, operated by the CPU clock, also stop. Because the main clock, sub clock, on-chip oscillator clock and PLL clock continue running, the peripheral functions using these clocks also continue to operate.

8.5.2.1 Peripheral Function Clock Stop Function

If the CM02 bit is set to "1" (peripheral function clock stops in wait mode), f_1, f_8, f_{32}, f_{2n} and f_{AD} stop in wait mode. Power consumption can be reduced. f_{C32} does not stop.

8.5.2.2 Before Entering Wait Mode

If the CM17 bit is set to "1" (PLL clock as CPU clock source), set the CM17 bit to "0" (main clock as CPU clock source) first. Then set the PLC07 bit in the PLC0 register to "0" (PLL stop), the PLV00 bit in the PLV register to "0" (cut off power to PLL), and enter wait mode

8.5.2.3 Pin Status in Wait Mode

Table 8.6 lists pin states in wait mode.

Table 8.6 Pin States in Wait Mode

Pin		Memory Expansion Mode Microprocessor Mode	Single-Chip Mode
Address Bus, Data Bus, $\overline{CS0}$ to $\overline{CS3}$, $\overline{BHE}$		Maintains state immediately before entering wait mode	
$\overline{RD}$, $\overline{WR}$, $\overline{WRL}$, $\overline{WRH}$, $\overline{DW}$, $\overline{CASL}$, $\overline{CASH}$		"H" (1)	
$\overline{RAS}$		"H" (1)	
$\overline{HLDA}$, BCLK		"H"	
ALE		"L"	
Port		Maintains state immediately before entering wait mode	
CLK_{OUT}	When f_C is selected	Outputs clock	
	When f_8, f_{32} are selected	When the CM02 bit in the CM0 register is set to "0" (peripheral function clock not stop in wait mode), the clock is output. When the CM02 bit is set to "1" (peripheral function clock stopped in wait mode), the state immediately before entering wait mode is maintained.	

NOTES:

1. When performing a self-refresh operation using the DRAMC, $\overline{CAS}$ and $\overline{RAS}$ become low ("L").

8.5.2.4 Exiting Wait Mode

Wait mode is exited by the hardware reset, $\overline{\text{NMI}}$ interrupt or peripheral function interrupts.

When the hardware reset or $\overline{\text{NMI}}$ interrupt, but not the peripheral function interrupts, is used to exit wait mode, set the ILVL2 to ILVL0 bits for the peripheral function interrupts to "000_2" (interrupt disabled) before executing the WAIT instruction.

The CM02 bit affects the peripheral function interrupts. When the CM02 bit is set to "0" (peripheral function clock does not stop in wait mode), all peripheral function interrupts can be used to exit wait mode. When the CM02 bit is set to "1" (peripheral function clock stops in wait mode), peripheral functions using the peripheral function clock stop. Therefore, the peripheral function interrupts cannot be used to exit wait mode. However, peripheral function interrupts caused by an external signal can be used to exit wait mode.

The CPU clock used when exiting wait mode by the peripheral function interrupts or $\overline{\text{NMI}}$ interrupt is the same CPU clock used when WAIT instructions are executed.

Table 8.7 shows interrupts to be used to exit wait mode and usage conditions.

Table 8.7 Interrupts to Exit Wait Mode

Interrupt	When CM02=0	When CM02=1
$\overline{\text{NMI}}$ Interrupt	Available	Available
Serial I/O Interrupt	Available when the internal and external clocks are used	Available only when the external clock is used
Key Input Interrupt	Available	Available
A/D Conversion Interrupt	Available in single or single-sweep mode	Do not use
Timer A Interrupt Timer B Interrupt	Available in all modes	Available in event counter mode or when the count source is fC_{32}
$\overline{\text{INT}}$ Interrupt	Available	Available
CAN Interrupt	Available	Do not use
Intelligent I/O Interrupt	Available	Do not use

8.5.2.5 Entering Wait Mode

The microcomputer enters wait mode when WAIT instructions are executed.

Follow the procedure below to enter wait mode.

- Initial Setting

  Set each interrupt priority level after setting the minimum interrupt priority level required to exit stop mode and wait mode, controlled by the RLVL2 to RLVL0 bits in the RLVL register, to "7".
- Before Execution of WAIT Instruction

  (1) Set the interrupt priority level of the interrupt being used to exit wait mode

  (2) Set the interrupt priority levels of the interrupts not being used to exit wait mode

  (3) Set the IPL in the FLG register. Then, set the minimum interrupt priority level required to exit stop mode and wait mode to the same level as the IPL. (Interrupt priority level of the interrupt used to exit wait mode > minimum interrupt priority level to exit wait mode ≥ interrupt priority level of the interrupts not used to exit wait mode)

  (4) Set the I flag to "1"

  (5) Execute WAIT instruction
- After Exiting Wait Mode

Set the interrupt priority level required to exit wait mode to "7" immediately after exiting wait mode.

8.5.3 Stop Mode

In stop mode, all oscillators and resonators stop. The CPU clock and peripheral function clock, as well as the CPU and peripheral functions operated by these clocks, also stop. The least power required to operate the microcomputer is in stop mode. The internal RAM holds its data if the voltage applied to the Vcc pin is 2.5V or more.
Interrupts used to exit stop mode are $\overline{NMI}$ interrupt, key input interrupt and $\overline{INT}$ interrupt.

8.5.3.1 Before Entering Stop Mode

When the CM10 bit in the CM1 register is set to "1" (all clocks stop), stop mode is entered. The MCD register is simultaneously set to "08_{16}" (divide-by-8 mode).
Do not enter stop mode when the CM21 bit in the CM2 register is set to "1" (on-chip oscillator clock as CPU clock source). Enter stop mode after setting the CM20 bit to "0" (oscillation stop detect function disabled) and the CM21 bit to "0" (main clock as CPU clock source).
To enter stop mode when the CM17 bit is set to "1" (PLL clock as CPU clock source), set the CM17 bit to "0" (main clock as CPU clock source) first. Then, set the PLC07 bit to "0" (PLL off), the PLV00 bit to "0" (cut off power to PLL) and enter stop mode.

8.5.3.2 Pin Status in Stop Mode

Table 8.8 lists pin status in stop mode.

Table 8.8 Pin Status in Stop Mode

Pin		Memory Expansion Mode Microprocessor Mode	Single-Chip Mode
Address Bus, Data Bus, $\overline{CS0}$ to $\overline{CS3}$, $\overline{BHE}$		Maintains state immediately before entering stop mode	
$\overline{RD}$, $\overline{WR}$, $\overline{WRL}$, $\overline{WRH}$, $\overline{DW}$, $\overline{CASL}$, $\overline{CASH}$		"H" (1)	
$\overline{RAS}$		"H" (1)	
$\overline{HLDA}$, BCLK		"H"	
ALE		"H"	
Port		Maintains state immediately before entering stop mode	
CLK_{OUT}	When f_C selected	"H"	
	When f_8, f_{32} selected	Maintains state immediately before entering stop mode	
X_{IN}		High-impedance	
X_{OUT}		"H"	
X_{CIN}, X_{COUT}		High-impedance	

NOTES:
1. When performing a self-refresh operation using the DRAMC, $\overline{CAS}$ and $\overline{RAS}$ become low ("L").

8.5.3.3 Exiting Stop Mode

Stop mode is exited by a hardware reset, $\overline{NMI}$ interrupt or peripheral function interrupts (key input interrupt and $\overline{INT}$ interrupt).
When the hardware reset or $\overline{NMI}$ interrupt, but not the peripheral function interrupts, is used to exit wait mode, set all ILVL2 to ILVL0 bits in the interrupt control registers for the peripheral function interrupt to "000_2" (interrupt disabled) before setting the CM10 bit to "1".
When stop mode is exited by the peripheral function interrupt or $\overline{NMI}$ interrupt, the CPU clock source is as follows, in accordance with the CPU clock source setting before the microcomputer had entered stop mode.

- When the sub clock is the CPU clock before entering stop mode : Sub clock
- When the main clock is the CPU clock before entering stop mode : Main clock divided by 8

8.5.3.4 Entering Stop Mode

Follow the procedure below to enter stop mode.

- Initial Setting

  Set each interrupt priority level after setting the minimum interrupt priority level required to exit stop mode and wait mode, controlled by the RLVL2 to RLVL0 bits in the RLVL register, to "7".

- Before Entering Stop Mode

  (1) Set the interrupt priority level of the interrupt being used to exit stop mode

  (2) Set the interrupt priority levels of the interrupts not being used to exit stop mode

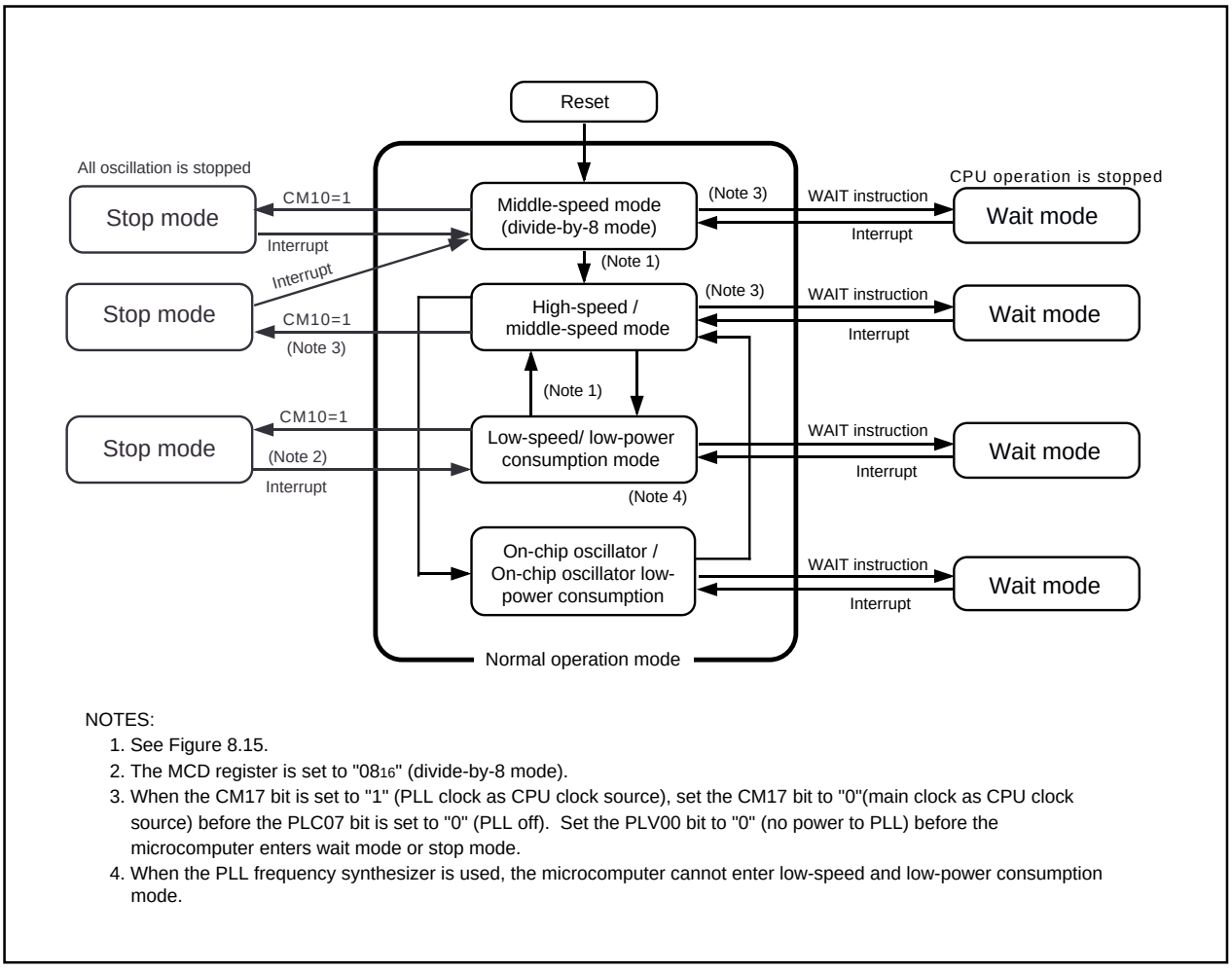
  (3) Set the IPL in the FLG register. Then set the minimum interrupt priority level required to exit stop mode and wait mode to the same level as the IPL. (Interrupt priority level of the interrupt used to exit stop mode > minimum interrupt priority level to exit stop mode ≥ interrupt priority level of the interrupts not used to exit stop mode)

  (4) Set the I flag to "1"

  (5) Set the CM10 bit in the CM1 register to "1" (all clocks stop) after setting the PRC0 bit in the PRCR register to "1" (write enabled)

- After Exiting Stop Mode

  Set the interrupt priority level required to exit stop mode to "7" immediately after exiting stop mode.



NOTES:

1. See Figure 8.15.
2. The MCD register is set to "08_{16}" (divide-by-8 mode).
3. When the CM17 bit is set to "1" (PLL clock as CPU clock source), set the CM17 bit to "0"(main clock as CPU clock source) before the PLC07 bit is set to "0" (PLL off). Set the PLV00 bit to "0" (no power to PLL) before the microcomputer enters wait mode or stop mode.
4. When the PLL frequency synthesizer is used, the microcomputer cannot enter low-speed and low-power consumption mode.

Figure 8.14 Status Transition in Wait Mode and Stop Mode

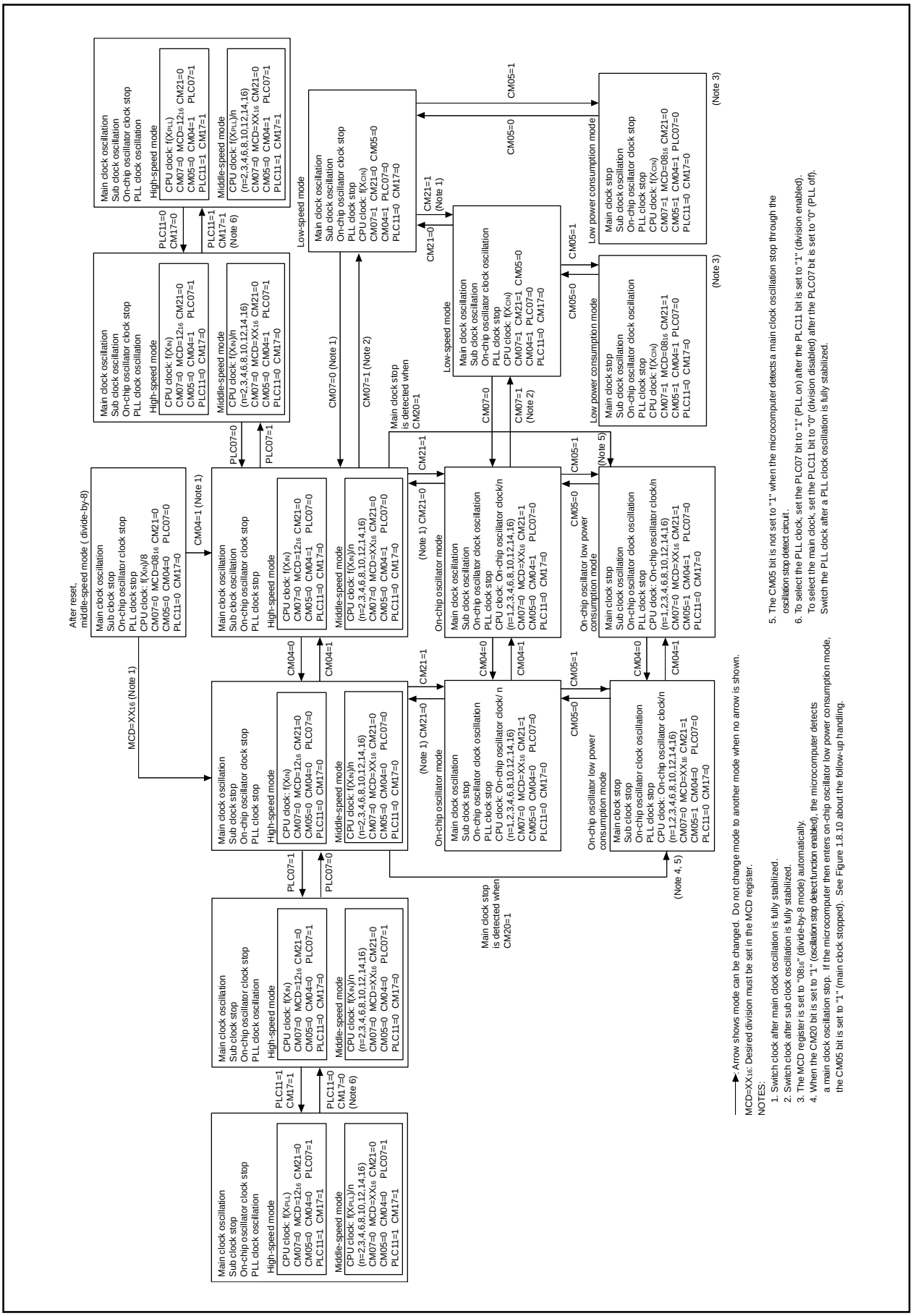


Figure 8.15 Status Transition

9. Protection

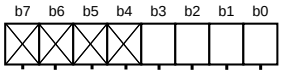
The protection function protects important registers from being easily overwritten when a program runs out of control.

Figure 9.1 shows the PRCR register. Each bit in the PRCR register protects the following registers:

- The PRC0 bit protects the CM0, CM1, CM2, MCD, PLC0 and PLC1 registers;
- The PRC1 bit protects the PM0, PM1, PM2, INVC0 and INVC1 registers;
- The PRC2 bit protects the PD9 and PS3 registers;
- The PRC3 bit protects the PLV and VDC0 registers.

The PRC2 bit is set to "0" (write disable) when data is written to a desired address after setting the PRC2 bit to "1" (write enable) . Set the PD9 and PS3 registers immediately after setting the PRC2 bit in the PRCR register to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the following instruction. The PRC0, PRC1 and PRC3 bits are not set to "0" even if data is written to desired addresses. Set the PRC0, PRC1 and PRC3 bits to "0" by program.

Protect Register



Symbol	Address	After Reset
PRCR	$000A_{16}$	$XXXX\ 0000_2$

Bit Symbol	Bit Name	Function	RW
PRC0	Protect Bit 0	Enables writing to CM0, CM1, CM2, MCD, PLC0, PLC1 registers 0 : Write disable 1 : Write enable	RW
PRC1	Protect Bit 1	Enables writing to PM0, PM1, INVC0, INVC1 registers 0 : Write disable 1 : Write enable	RW
PRC2	Protect Bit 2(1)	Enables writing to PD9, PS3 registers 0 : Write disable 1 : Write enable	RW
PRC3	Protect Bit 3	Enables writing to PLV, VDC0 and VDC1 registers 0 : Write disable 1 : Write enable	RW
____ (b7 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

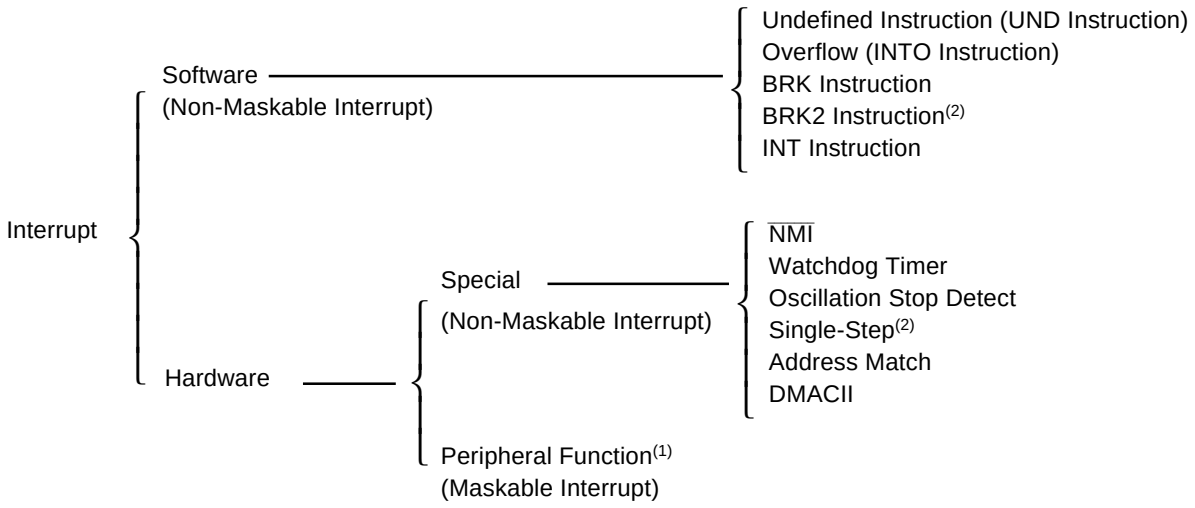
NOTES:
1. The PRC2 bit can be set to "0" by writing to a desired address after the PRC2 bit is set to "1". The PRC0, PRC1 and PRC3 bits are not automatically set to "0". Set to"0" by program.

Figure 9.1 PRCR Register

10. Interrupts

10.1 Types of Interrupts

Figure 10.1 shows types of interrupts.



NOTES:
1. The peripheral functions in the microcomputer are used to generate the peripheral interrupt.
2. Do not use this interrupt. For development support tools only.

Figure 10.1 Interrupts

- Maskable Interrupt
  The I flag enables or disables an interrupt.
  The interrupt priority order based on interrupt priority level **can be changed**.

- Non-maskable Interrupt
  The I flag does not enable nor disable an interrupt .
  The interrupt priority order based on interrupt priority level **cannot be changed**.

10.2 Software Interrupts

Software interrupt occurs when an instruction is executed. The software interrupts are non-maskable interrupts.

10.2.1 Undefined Instruction Interrupt

The undefined instruction interrupt occurs when the UND instruction is executed.

10.2.2 Overflow Interrupt

The overflow interrupt occurs when the O flag in the FLG register is set to "1" (arithmetic operation overflow) and the INTO instruction is executed.
Instructions to set the O flag are :
ABS, ADC, ADCF, ADD, ADDX, CMP, CMPX, DIV, DIVU, DIVX, NEG, RMPA, SBB, SCMPU, SHA, SUB, SUBX

10.2.3 BRK Interrupt

The BRK interrupt occurs when the BRK instruction is executed.

10.2.4 BRK2 Interrupt

The BRK2 interrupt occurs when the BRK2 instruction is executed.
Do not use this interrupt. For development support tools only.

10.2.5 INT Instruction Interrupt

The INT instruction interrupt occurs when the INT instruction is executed. The INT instruction can select software interrupt numbers 0 to 63. Software interrupt numbers 7 to 54, and 57 are assigned to the vector table used for the peripheral function interrupt. Therefore, the microcomputer executes the same routine when the INT instruction is executed as when a peripheral function interrupt occurs.
When the INT instruction is executed, the FLG register and PC are saved to the stack. PC also stores the relocatable vector of the specified software interrupt number. Where the stack is saved varies, depending on the software interrupt number. ISP is selected as the stack for the software interrupt numbers 0 to 31 (the U flag is set to "0"). SP, which is set before the INT instruction is executed, is selected as the stack for the software interrupt numbers 32 to 63 (the U flag is not changed).
With the peripheral function interrupt, the FLG register is saved and the U flag is set to "0" (ISP select) when an interrupt request is acknowledged. With software interrupt numbers 32 to 54 and 57, the SP to be used varies, depending on whether the interrupt is generated by the peripheral function interrupt request or by the INT instruction.

10.3 Hardware Interrupts

Special interrupts and peripheral function interrupts are available as hardware interrupts.

10.3.1 Special Interrupts

Special interrupts are non-maskable interrupts.

10.3.1.1 $\overline{\text{NMI}}$ Interrupt

The $\overline{\text{NMI}}$ interrupt occurs when a signal applied to the $\overline{\text{NMI}}$ pin changes from an "H" signal to an "L" signal. Refer to **10.8 $\overline{\text{NMI}}$ Interrupt** for details.

10.3.1.2 Watchdog Timer Interrupt

The watchdog timer interrupt occurs when the count source of the watchdog timer underflows. Refer to **11. Watchdog Timer** for details.

10.3.1.3 Oscillation Stop Detection Interrupt

The oscillation stop detection interrupt occurs when the microcomputer detects a main clock oscillation stop. Refer to **8. Clock Generating Circuit** for details.

10.3.1.4 Single-Step Interrupt

Do not use the single-step interrupt. For development support tool only.

10.3.1.5 Address Match Interrupt

The address match interrupt occurs immediately before executing an instruction that is stored into an address indicated by the RMADi register (i=0 to 3) when the AIERi bit in the AIER register is set to "1" (address match interrupt enabled). Set the starting address of the instruction in the RMADi register. The address match interrupt does not occur when a table data or addresses of the instruction other than the starting address, if the instruction has multiple addresses, is set. Refer to **10.10 Address Match Interrupt** for details.

10.3.2 Peripheral Function Interrupt

The peripheral function interrupt occurs when a request from the peripheral functions in the microcomputer is acknowledged. The peripheral function interrupts and software interrupt numbers 7 to 54 and 57 for the INT instruction use the same interrupt vector table. The peripheral function interrupt is a maskable interrupt.

See **Table 10.2** about how the peripheral function interrupt occurs. Refer to the descriptions of each function for details.

10.4 High-Speed Interrupt

The high-speed interrupt executes an interrupt sequence in 5 cycles and returns from the interrupt in 3 cycles.

When the FSIT bit in the RLVL register is set to "1" (interrupt priority level 7 available for the high-speed interrupt), the ILVL2 to ILVL0 bits in the interrupt control registers can be set to "111_2" (level 7) to use the high-speed interrupt.

Only one interrupt can be set as the high-speed interrupt. When using the high-speed interrupt, do not set multiple interrupts to interrupt priority level 7. Set the DMAII bit in the RLVL register to "0" (interrupt priority level 7 available for interrupts).

Set the starting address of the high-speed interrupt routine in the VCT register.

When the high-speed interrupt is acknowledged, the FLG register is saved to the SVF register and PC is saved to the SVP registers. The program is executed from an address indicated by the VCT register.

Execute the FREIT instruction to return from the high-speed interrupt routine.

The values saved to the SVF and SVP registers are restored to the FLG register and PC by executing the FREIT instruction.

The high-speed interrupt and the DMA2 and DMA3 use the same register. When using the high-speed interrupt, neither DMA2 nor DMA3 is available. DMA0 and DMA1 can be used.

10.5 Interrupts and Interrupt Vectors

There are four bytes in one vector. Set the starting address of interrupt routine in each vector table. When an interrupt request is acknowledged, the program is executed from the address set in the interrupt vectors. Figure 10.2 shows the interrupt vector.

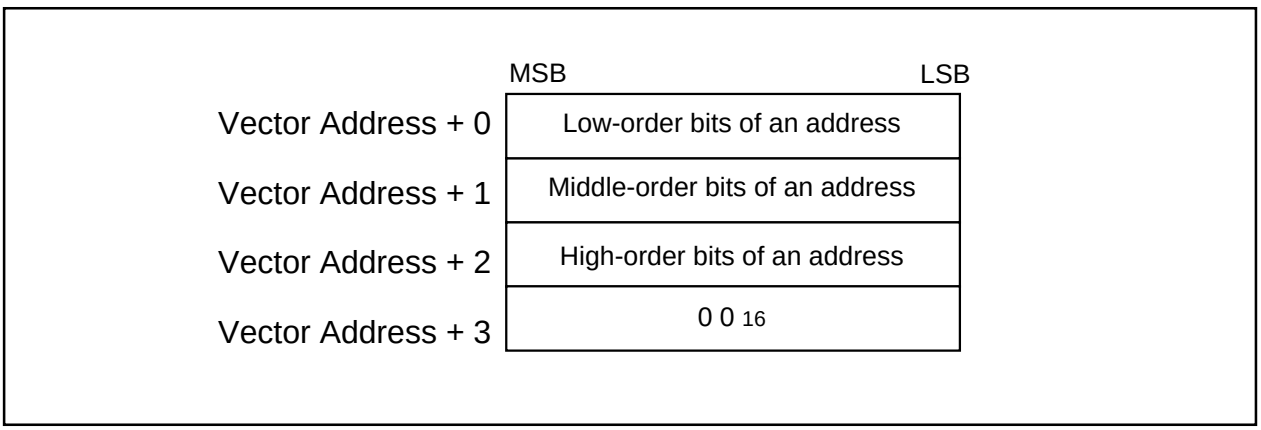


Figure 10.2 Interrupt Vector

10.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses FFFFDC16 to FFFFFF16. Table 10.1 lists the fixed vector tables. Refer to **25.2 Functions to Prevent Flash Memory from Rewriting** for fixed vectors of flash memory.

Table 10.1 Fixed Vector Table

Interrupt Generated by	Vector Addresses Address (L) to Address (H)	Remarks	Reference
Undefined Instruction	FFFFDC16 to FFFFDF16		M32C/80 series software manual
Overflow	FFFFE016 to FFFFE316		
BRK Instruction	FFFFE416 to FFFFE716	If the content of address FFFFE716 is FF16, the program is executed from the address stored into software interrupt number 0 in the relocatable vector table	
Address Match	FFFFE816 to FFFFEB16		
-	FFFFEC16 to FFFFEF16	Reserved space	
Watchdog Timer	FFFFF016 to FFFFF316	These addresses are used for the watchdog timer interrupt and the oscillation stop detect interrupt	Clock oscillation circuit, Watchdog timer
-	FFFFF416 to FFFFF716	Reserved space	
$\overline{\text{NMI}}$	FFFFF816 to FFFFFB16		
Reset	FFFFFC16 to FFFFFF16		Reset

10.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes from the starting address set in the INTB register. Table 10.2 lists the relocatable vector tables.

Set an even address as the starting address of the vector table set in the INTB register to increase interrupt sequence execution rate.

Table 10.2 Relocatable Vector Tables

Interrupt Generated by	Vector Table Address Address(L) to Address(H)(1)	Software Interrupt Number	Reference
BRK Instruction(2)	+0 to +3 (0000_{16} to 0003_{16})	0	M32C/80 Series
Reserved Space	+4 to +27 (0004_{16} to $001B_{16}$)	1 to 6	Software Manual
A/D1	+28 to +31 ($001C_{16}$ to $001F_{16}$)	7	A/D Converter
DMA0	+32 to +35 (0020_{16} to 0023_{16})	8	DMAC
DMA1	+36 to +39 (0024_{16} to 0027_{16})	9	
DMA2	+40 to +43 (0028_{16} to $002B_{16}$)	10	
DMA3	+44 to +47 ($002C_{16}$ to $002F_{16}$)	11	
Timer A0	+48 to +51 (0030_{16} to 0033_{16})	12	Timer A
Timer A1	+52 to +55 (0034_{16} to 0037_{16})	13	
Timer A2	+56 to +59 (0038_{16} to $003B_{16}$)	14	
Timer A3	+60 to +63 ($003C_{16}$ to $003F_{16}$)	15	
Timer A4	+64 to +67 (0040_{16} to 0043_{16})	16	
UART0 Transmission, NACK(3)	+68 to +71 (0044_{16} to 0047_{16})	17	Serial I/O
UART0 Reception, ACK(3)	+72 to +75 (0048_{16} to $004B_{16}$)	18	
UART1 Transmission, NACK(3)	+76 to +79 ($004C_{16}$ to $004F_{16}$)	19	
UART1 Reception, ACK(3)	+80 to +83 (0050_{16} to 0053_{16})	20	
Timer B0	+84 to +87 (0054_{16} to 0057_{16})	21	Timer B
Timer B1	+88 to +91 (0058_{16} to $005B_{16}$)	22	
Timer B2	+92 to +95 ($005C_{16}$ to $005F_{16}$)	23	
Timer B3	+96 to +99 (0060_{16} to 0063_{16})	24	
Timer B4	+100 to +103 (0064_{16} to 0067_{16})	25	
$\overline{\text{INT5}}$	+104 to +107 (0068_{16} to $006B_{16}$)	26	Interrupt
$\overline{\text{INT4}}$	+108 to +111 ($006C_{16}$ to $006F_{16}$)	27	
$\overline{\text{INT3}}$	+112 to +115 (0070_{16} to 0073_{16})	28	
$\overline{\text{INT2}}$	+116 to +119 (0074_{16} to 0077_{16})	29	
$\overline{\text{INT1}}$	+120 to +123 (0078_{16} to $007B_{16}$)	30	
$\overline{\text{INT0}}$	+124 to +127 ($007C_{16}$ to $007F_{16}$)	31	
Timer B5	+128 to +131 (0080_{16} to 0083_{16})	32	Timer B
UART2 Transmission, NACK(3)	+132 to +135 (0084_{16} to 0087_{16})	33	Serial I/O
UART2 Reception, ACK(3)	+136 to +139 (0088_{16} to $008B_{16}$)	34	
UART3 Transmission, NACK(3)	+140 to +143 ($008C_{16}$ to $008F_{16}$)	35	
UART3 Reception, ACK(3)	+144 to +147 (0090_{16} to 0093_{16})	36	
UART4 Transmission, NACK(3)	+148 to +151 (0094_{16} to 0097_{16})	37	
UART4 Reception, ACK(3)	+152 to +155 (0098_{16} to $009B_{16}$)	38	

Table 10.2 Relocatable Vector Tables (Continued)

Interrupt Generated by	Vector Table Address Address(L)to Address(H)(1)	Software Interrupt Number	Reference
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, (UART2)(3), Fault Error(4)	+156 to +159 (009C16 to 009F16)	39	Serial I/O
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, (UART3/UART0)(5), Fault Error(4)	+160 to +163 (00A016 to 00A316)	40	
Bus Conflict Detect, Start Condition Select, Stop Condition Detect, (UART4/UART1)(5), Fault Error(4)	+164 to +167 (00A416 to 00A716)	41	
A/D0	+168 to +171 (00A816 to 00AB16)	42	A/D Converter
Key Input	+172 to +175 (00AC16 to 00AF16)	43	Interrupts
Intelligent I/O Interrupt 0	+176 to +179 (00B016 to 00B316)	44	Intelligent I/O CAN
Intelligent I/O Interrupt 1	+180 to +183 (00B416 to 00B716)	45	
Intelligent I/O Interrupt 2	+184 to +187 (00B816 to 00BB16)	46	
Intelligent I/O Interrupt 3	+188 to +191 (00BC16 to 00BF16)	47	
Intelligent I/O Interrupt 4	+192 to +195 (00C016 to 00C316)	48	
Intelligent I/O Interrupt 5	+196 to +199 (00C416 to 00C716)	49	
Intelligent I/O Interrupt 6	+200 to +203(00C816 to 00CB16)	50	
Intelligent I/O Interrupt 7	+204 to +207(00CC16 to 00CF16)	51	
Intelligent I/O Interrupt 8	+208 to +211(00D016 to 00D316)	52	
Intelligent I/O Interrupt 9, CAN 0	+212 to +215 (00D416 to 00D716)	53	
Intelligent I/O Interrupt 10, CAN 1	+216 to +219 (00D816 to 00DB16)	54	
Reserved Space	+220 to +227 (00DC16 to 00E316)	55 to 56	—
Intelligent I/O Interrupt 11, CAN 2	+228 to +231 (00E416 to 00E716)	57	Intelligent I/O CAN
Reserved Space	+232 to +255 (00E816 to 00FF16)	58 to 62	—
INT Instruction(2)	+0 to +3 (000016 to 000316) to +252 to +255 (00FC16 to 00FF16)	0 to 63	Interrupts

NOTES:

1. These addresses are relative to those in the INTB register.
2. The I flag does not disable interrupts.
3. In I^2C mode, NACK, ACK or start/stop condition detection causes interrupts to be generated.
4. When the $\overline{SS}$ pin is selected, fault error causes an interrupt to be generated.
5. The IFSR6 bit in the IFSR register determines whether these addresses are used for an interrupt in UART0 or in UART3.
   The IFSR7 bit in the IFSR register determines whether these addresses are used for an interrupt in UART1 or in UART4.

10.6 Interrupt Request Reception

Software interrupts and special interrupts occur when conditions to generate an interrupt are met.

The peripheral function interrupts are acknowledged when all conditions below are met.

- I flag = "1"
- IR bit = "1"
- ILVL2 to ILVL0 bits > IPL

The I flag, IPL, IR bit and ILVL2 to ILVL0 bits are independent of each other. The I flag and IPL are in the FLG register. The IR bit and ILVL2 to ILVL0 bits are in the interrupt control register.

10.6.1 I Flag and IPL

The I flag enables or disables maskable interrupts. When the I flag is set to "1" (enable), all maskable interrupts are enabled; when the I flag is set to "0" (disable), they are disabled. The I flag is automatically set to "0" after reset.

IPL, consisting of three bits, indicates the interrupt priority level from level 0 to level 7.

If a requested interrupt has higher priority than that indicated by IPL, the interrupt is acknowledged.

Table 10.3 lists interrupt priority levels associated with IPL.

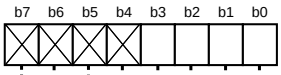
Table 10.3 Interrupt Priority Levels

IPL2	IPL1	IPL0	Interrupt Priority Levels
0	0	0	Level 1 and above
0	0	1	Level 2 and above
0	1	0	Level 3 and above
0	1	1	Level 4 and above
1	0	0	Level 5 and above
1	0	1	Level 6 and above
1	1	0	Level 7 and above
1	1	1	All maskable interrupts are disabled

10.6.2 Interrupt Control Register and RLVL Register

The peripheral function interrupts use interrupt control registers to control each interrupt. Figures 10.3 and 10.4 show the interrupt control register. Figure 10.5 shows the RLVL register.

Interrupt Control Register



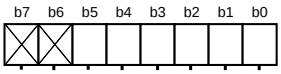
Symbol	Address	After Reset
TA0IC to TA4IC	$006C_{16}$, $008C_{16}$, $006E_{16}$, $008E_{16}$, 0070_{16}	XXXX X000$_2$
TB0IC to TB5IC	0094_{16}, 0076_{16}, 0096_{16}, 0078_{16}, 0098_{16}, 0069_{16}	XXXX X000$_2$
S0TIC to S4TIC	0090_{16}, 0092_{16}, 0089_{16}, $008B_{16}$, $008D_{16}$	XXXX X000$_2$
S0RIC to S4RIC	0072_{16}, 0074_{16}, $006B_{16}$, $006D_{16}$, $006F_{16}$	XXXX X000$_2$
BCN0IC to BCN4IC	0071_{16}, 0091_{16}, $008F_{16}$, 0071_{16}(1), 0091_{16}(2)	XXXX X000$_2$
DM0IC to DM3IC	0068_{16}, 0088_{16}, $006A_{16}$, $008A_{16}$	XXXX X000$_2$
AD0IC, AD1IC	0073_{16}, 0086_{16}	XXXX X000$_2$
KUPIC	0093_{16}	XXXX X000$_2$
IIO0IC to IIO5IC	0075_{16}, 0095_{16}, 0077_{16}, 0097_{16}, 0079_{16}, 0099_{16}	XXXX X000$_2$
IIO6IC to IIO11IC	$007B_{16}$, $009B_{16}$, $007D_{16}$, $009D_{16}$, $007F_{16}$, 0081_{16}	XXXX X000$_2$
CAN0IC0 to CAN2IC	$009D_{16}$, $007F_{16}$, 0081_{16}(3)	XXXX X000$_2$

Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt Priority Level Select Bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt Request Bit	0 : No interrupt requested 1 : Interrupt requested(4)	RW
____ (b7 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. The BCN0IC register shares an address with the BCN3IC register.
2. The BCN1IC register shares an address with the BCN4IC register.
3. The IIO9IC register shares an address with the CAN0IC register.
   The IIO10IC register shares an address with the CAN1IC register.
   The IIO11IC register shares an address with the CAN2IC register.
4. The IR bit can be set to "0" only (do not set to "1").

Figure 10.3 Interrupt Control Register (1)

Interrupt Control Register



Symbol	Address	After Reset
INT0IC to INT2IC	009E16, 007E16, 009C16	XX00 X0002
INT3IC to INT5IC(1)	007C16, 009A16, 007A16	XX00 X0002

Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt Priority Level Select Bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt Request Bit	0 : Requests no interrupt 1 : Requests an interrupt(2)	RW
POL	Polarity Switch Bit	0 : Selects falling edge or "L" 1 : Selects rising edge or "H"(3)	RW
LVS	Level Sense/Edge Sense Switch Bit	0 : Edge sense 1 : Level sense(4)	RW
____ (b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

NOTES:
1. When the 16-bit data bus is used in microprocessor or memory expansion mode, each pin for the INT3 to INT5 bits is used as the data bus. Set the ILVL2 to ILVL0 bits in the INT3IC, INT4IC and INT5IC registers to "0002".
2. The IR bit can be set to "0" only (do not set to "1").
3. Set the POL bit to "0" when the corresponding bit in the IFSR register is set to "1" (both edges).
4. When setting a level sense, set a bit corresponding to the IFSR register to "0" (one edge).

Figure 10.4 Interrupt Control Register (2)

10.6.2.1 ILVL2 to ILVL0 Bits

The ILVL2 to ILVL0 bits determines the interrupt priority level. The higher the interrupt priority level, the higher interrupt priority is.

When an interrupt request is generated, its interrupt priority level is compared to IPL. This interrupt is acknowledged only when its interrupt priority level is higher than IPL. When the ILVL2 to ILVL0 bits are set to "0002" (level 0), this interrupt is ignored.

10.6.2.2 IR Bit

The IR bit is set to "1" (interrupt requested) by hardware when an interrupt request is generated. The IR bit is set to "0" (no interrupt requested) by hardware after an interrupt request is acknowledged and the program in the corresponding interrupt vector is executed.

The IR bit can be set to "0" by program. Do not set to "1".

Exit Priority Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
X	X		X					RLVL	009F16	XXXX 00002

Bit Symbol	Bit Name	Function	RW
RLVL0	Stop/Wait Mode Exit Minimum Interrupt Priority Level Control Bit(1)	b2 b1 b0 0 0 0 : Level 0 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
RLVL1			RW
RLVL2			RW
FSIT	High-Speed Interrupt Set Bit(2)	0: Interrupt priority level 7 is used for normal interrupt 1: Interrupt priority level 7 is used for high-speed interrupt	RW
____ (b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
DMA II	DMAC II Select Bit(3,4)	0: Interrupt priority level 7 is used for interrupt 1: Interrupt priority level 7 is used for DMAC II transfer	RW
____ (b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. The microcomputer exits stop or wait mode when the requested interrupt priority level is higher than the level set in the RLVL2 to RLVL0 bits. Set the RLVL2 to RLVL0 bits to the same value as IPL in the FLG register.
2. When the FSIT bit is set to "1" (high-speed interrupt), interrupt priority level 7 becomes the high-speed interrupt. In this case, set only one interrupt to interrupt priority level 7 and the DMA II bit to "0" (normal interrupt).
3. After reset, set the DMA II bit only once. Set the ILVl1 to ILVL0 bits after setting the DMA II bit following reset. When setting the DMA II bit to "1", set the FSIT bit to "0" (normal interrupt). The DMAC II cannot be used simultaneously with the high-speed interrupt . I flag and IPL settings do not affect DMAC II transfer.
4. After reset, the DMA II bit is indeterminate. When using an interrupt, set the interrupt control register after setting the DMA II bit to "0".

Figure 10.5 RLVL Register

10.6.2.3 RLVL2 to RLVL0 Bits

When using an interrupt to exit stop or wait mode, refer to **8.5.2 Wait Mode** and **8.5.3 Stop Mode** for details.

10.6.3 Interrupt Sequence

The interrupt sequence is performed between an interrupt request acknowledgment and interrupt routine execution.

When an interrupt request is generated while an instruction is executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, in regards to the SCMPU, SIN, SMOVB, SMOVF, SMOVU, SSTR, SOUT or RMPA instruction, if an interrupt request is generated while executing the instruction, the microcomputer suspends the instruction to start the interrupt sequence.

The interrupt sequence is performed as follows:

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 000000_{16} (address 000002_{16} for the high-speed interrupt). Then, the IR bit applicable to the interrupt information is set to "0" (interrupt requested).
(2) The FLG register, prior to an interrupt sequence, is saved to a temporary register(1) within the CPU.
(3) Each bit in the FLG register is set as follows:
- The I flag is set to "0" (interrupt disabled)
- The D flag is set to "0" (single-step disabled)
- The U flag is set to "0" (ISP selected)

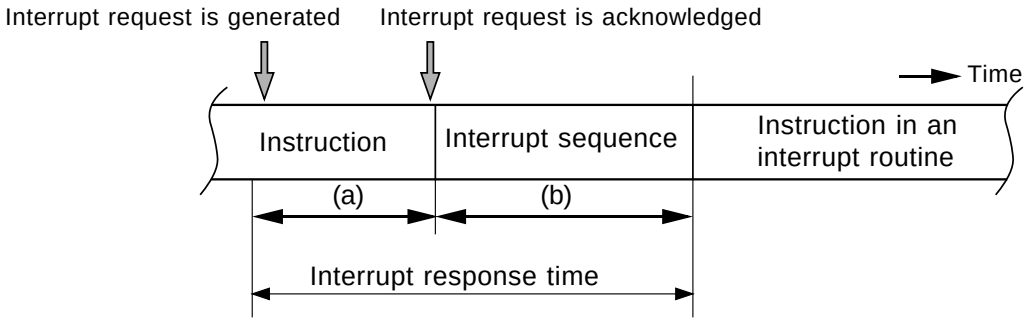
(4) A temporary register within the CPU is saved to the stack; or to the SVF register for the high-speed interrupt.
(5) PC is saved to the stack; or to the SVP register for the high-speed interrupt.
(6) The interrupt priority level of the acknowledged interrupt is set in IPL .
(7) A relocatable vector corresponding to the acknowledged interrupt is stored into PC.

After the interrupt sequence is completed, an instruction is executed from the starting address of the interrupt routine.

NOTES:
1. Temporary register cannot be modified by users.

10.6.4 Interrupt Response Time

Figure 10.6 shows an interrupt response time. Interrupt response time is the period between an interrupt generation and the execution of the first instruction in an interrupt routine. An interrupt response time includes the period between an interrupt request generation and the completed execution of an instruction ((a) in Figure 10.6) and the period required to perform an interrupt sequence ((b) in Figure 10.6).



(a) Period between an interrupt request generation and the completed execution of an instruction.
(b) Period required to perform an interrupt sequence.

Figure 10.6 Interrupt Response Time

Time (a) varies depending on the instruction being executed. The DIV instruction requires the longest time (a); 40 cycles when an immediate value or register is set as the divisor .
When the divisor is a value in the memory, the following value is added.

- Normal addressing : 2 + X
- Index addressing : 3 + X
- Indirect addressing : 5 + X + 2Y
- Indirect index addressing : 6 + X + 2Y

X is the number of wait states for a divisor space. Y is the number of wait states for the space that stores indirect addresses. If X and Y are in an odd address or in 8-bit bus space, the X and Y value must be doubled.
Table 10.4 lists time (b).

Table 10.4 Interrupt Sequence Execution Time

Interrupt	Interrupt Vector Address	16-Bit Bus	8-Bit Bus
Peripheral Function	Even address	14 cycles	16 cycles
	Odd address(1)	16 cycles	16 cycles
INT Instruction	Even address	12 cycles	14 cycles
	Odd address(1)	14 cycles	14 cycles
$\overline{\text{NMI}}$ Watchdog Timer Undefined Instruction Address Match	Even address(2)	13 cycles	15 cycles
Overflow	Even address(2)	14 cycles	16 cycles
BRK Instruction (relocatable vector table)	Even address	17 cycles	19 cycles
	Odd address(1)	19 cycles	19 cycles
BRK Instruction (fixed vector table)	Even address(2)	19 cycles	21 cycles
High-Speed Interrupt	Vector table is internal register	5 cycles	

NOTES:
1. Allocate interrupt vectors to even addresses.
2. Vectors are fixed to even addresses.

10.6.5 IPL Change when Interrupt Request is Acknowledged

When a peripheral function request is acknowledged, IPL sets the priority level for the acknowledged interrupt.

Software interrupts and special interrupts have no interrupt priority level. If an interrupt request that has no interrupt priority level is acknowledged, the value shown in Table 10.5 is set in IPL as the interrupt priority level.

Table 10.5 Interrupts without Interrupt Priority Levels and IPL

Interrupt Sources	Level that is Set to IPL
Watchdog Timer, $\overline{\text{NMI}}$, Oscillation Stop Detect	7
Reset	0
Software, Address Match	Not changed

10.6.6 Saving a Register

In the interrupt sequence, the FLG register and PC are saved to the stack.

After the FLG register is saved to the stack, 16 high-order bits and 16 low-order bits of PC, extended to 32 bits, are saved to the stack. Figure 10.7 shows the stack state before and after an interrupt request is acknowledged.

Other important registers are saved by program at the beginning of an interrupt routine. The PUSHM instruction can save all registers except SP.

Refer to **10.4 High-Speed Interrupt** for the high-speed interrupt.

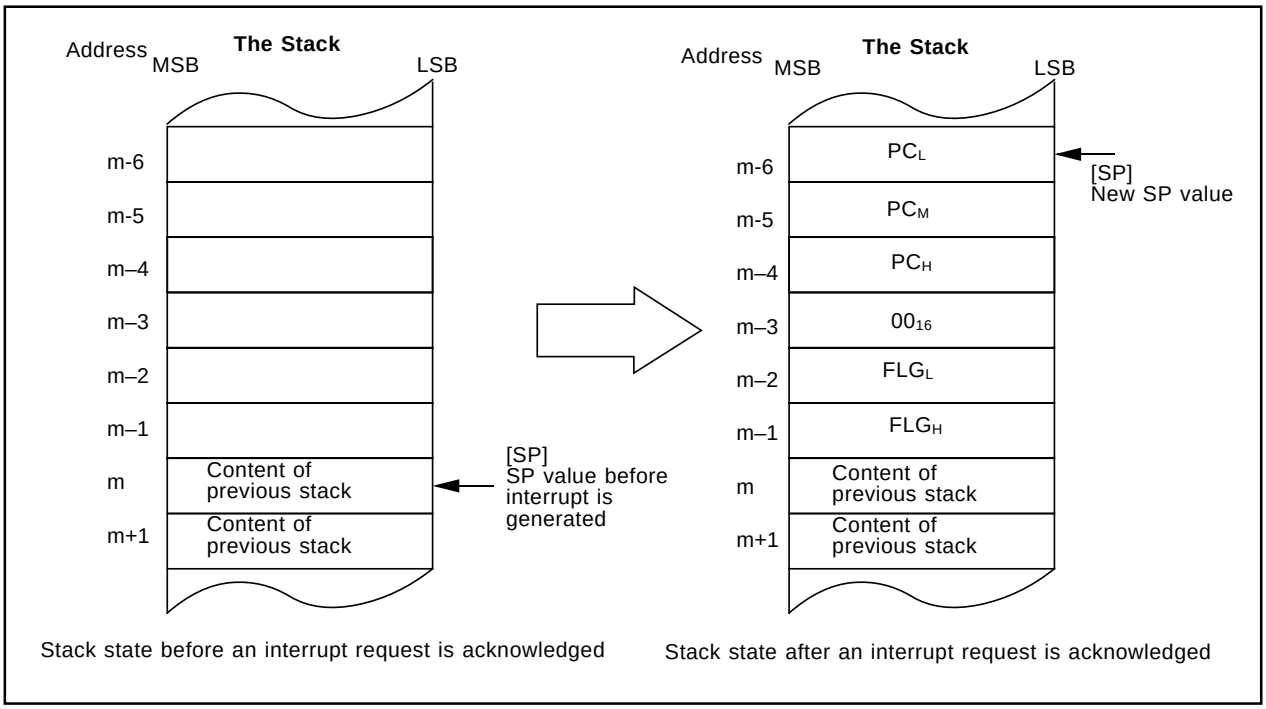


Figure 10.7 Stack States

10.6.7 Restoration from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved to the stack, are automatically restored. The program, executed before the interrupt request has been acknowledged, starts running again. Refer to **10.4 High-Speed Interrupt** for the high-speed interrupt.

Restore registers saved by program in an interrupt routine by the POPM instruction or others before the REIT and FREIT instructions. Register bank is switched back to the bank used prior to the interrupt sequence by the REIT or FREIT instruction.

10.6.8 Interrupt Priority

If two or more interrupt requests are sampled at the same sampling points (a timing to detect whether an interrupt request is generated or not), the interrupt with the highest priority is acknowledged.

Set the ILVL2 to ILVL0 bits to select the desired priority level for maskable interrupts (peripheral function interrupt).

Priority levels of special interrupts such as reset (reset has the highest priority) and watchdog timer are set by hardware. Figure 10.8 shows priority levels of hardware interrupts.

The interrupt priority does not affect software interrupts. The microcomputer jumps to the interrupt routine when the instruction is executed.

Reset > $\overline{\text{NMI}}$ > Oscillation Stop Detect / Watchdog > Peripheral Function > Address Match

Figure 10.8 Interrupt Priority

10.6.9 Interrupt Priority Level Select Circuit

The interrupt priority level select circuit selects the highest priority interrupt when two or more interrupt requests are sampled at the same sampling point.

Figure 10.9 shows the interrupt priority level select circuit.

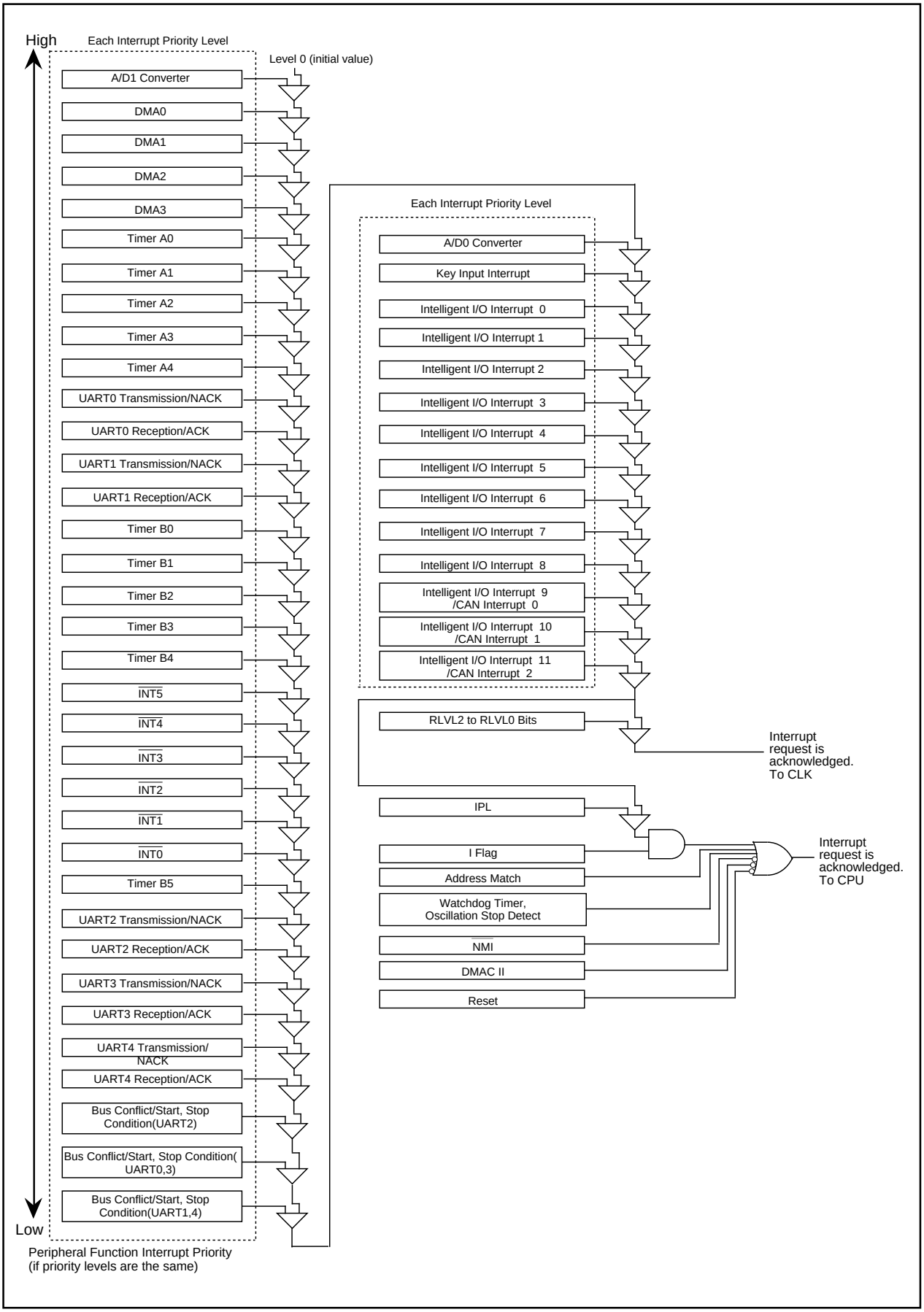


Figure 10.9 Interrupt Priority Level Select Circuit

10.7 $\overline{\text{INT}}$ Interrupt

The $\overline{\text{INTi}}$ interrupt (i = 0 to 5) is generated by an external input. The LVS bit in the INTiIC register selects either an edge sense to generate an interrupt by an edge or a level sense to generate an interrupt by an applied signal level. The POL bit in the INTiIC register determines the polarity.

With an edge sense, when the IFSRi bit in the IFSR register is set to "1" (both edges), an interrupt occurs on both rising and falling edges of the external input. If the IFSRi bit is set to "1", set the POL bit in the corresponding register to "0" (falling edge).

With a level sense, set the IFSRi bit to "0" (single edge). When the $\overline{\text{INTi}}$ pin input level reaches the level set in the POL bit, the IR bit in the INTiIC register is set to "1". The IR bit remains set to "1" even if the $\overline{\text{INTi}}$ pin level is changed. The IR bit is set to "0" when the $\overline{\text{INTi}}$ interrupt is acknowledged or when "0" is written by program.

Figure 10.10 shows the IFSR register.

External Interrupt Request Cause Select Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
								IFSR	031F16	0016

Bit Symbol	Bit Name	Function	RW
IFSR0	INT0 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR1	INT1 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR2	INT2 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR3	INT3 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR4	INT4 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR5	INT5 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR6	UART0, 3 Interrupt Cause Select Bit	0 : UART3 bus conflict, start condition detect, stop condition detect, fault error detect 1 : UART0 bus conflict, start condition detect, stop condition detect, fault error detect	RW
IFSR7	UART1, 4 Interrupt Cause Select Bit	0 : UART4 bus conflict, start condition detect, stop condition detect, fault error detect 1 : UART1 bus conflict, start condition detect, stop condition detect, fault error detect	RW

NOTES:
1.When level sense is selected, set this bit to "0".
When both edges are selected, set the POL bit in the INTiIC register (i = 0 to 5) to "0" (falling edge).

Figure 10.10 IFSR Register

10.8 NMI Interrupt

The NMI interrupt occurs when the signal applied to the P85/NMI pin changes from an "H" signal to an "L" signal. The NMI interrupt is a non-maskable interrupt. Although the P85/NMI pin is used as the NMI interrupt input pin, the P8_5 bit in the P85 register indicates input level for this pin.

NOTES:

When the NMI function is not used, connect (pull-up) the NMI pin to Vcc via a resistor. Because the NMI interrupt cannot be ignored, the pin must be connected.

10.9 Key Input Interrupt

The key input interrupt request is generated when one of the signals applied to the P104 to P107 pins in input mode is on the falling edge. The key input interrupt can be also used as key-on wake-up function to exit wait or stop mode. With the key input interrupt, do not use P104 to P107 as A/D input ports. Figure 10.11 shows a block diagram of the key input interrupt. When an "L" signal is applied to any pins in input mode, signals applied to other pins are not detected as a request signal for an interrupt.

When the PSC_7 bit in the PSC register(1) is set to "1" (key input interrupt disabled), no key input interrupt occurs regardless of interrupt control register settings. When the PSC_7 bit is set to "1", no input from a port pin is available even when in input mode.

NOTES:

1. Refer to **24. Programmable I/O Ports** for details on the PSC register.

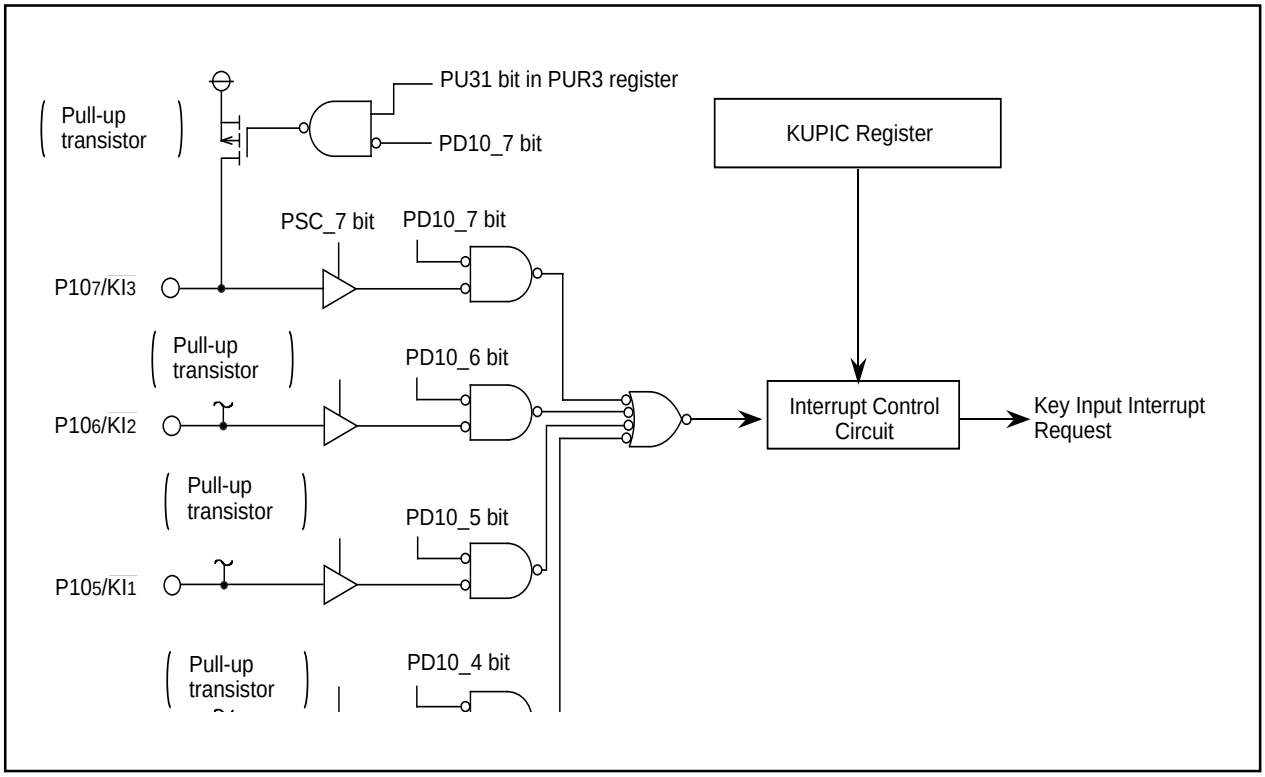


Figure 10.11 Key Input Interrupt

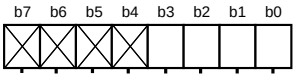
10.10 Address Match Interrupt

The address match interrupt occurs immediately before executing an instruction that is stored into an address indicated by the RMADi register (i=0 to 3). The address match interrupt can be set in four addresses. The AIERi bit in the AIER register determines whether the interrupt is enabled or disabled. The I flag and IPL do not affect the address match interrupt.

Figure 10.12 shows registers associated with the address match interrupt.

Set the starting address of an instruction in the RMADi register. The address match interrupt does not occur when a table data or addresses other than the starting address of the instruction is set.

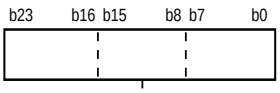
Address Match Interrupt Enable Register



Symbol	Address	After Reset
AIER	0009_{16}	XXXX 0000_2

Bit Symbol	Bit Name	Function	RW
AIER0	Address Match Interrupt 0 Enable Bit	0 : Disables the interrupt 1 : Enables the interrupt	RW
AIER1	Address Match Interrupt 1 Enable Bit	0 : Disables the interrupt 1 : Enables the interrupt	RW
AIER2	Address Match Interrupt 2 Enable Bit	0 : Disables the interrupt 1 : Enables the interrupt	RW
AIER3	Address Match Interrupt 3 Enable Bit	0 : Disables the interrupt 1 : Enables the interrupt	RW
____ (b7 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

Address Match Interrupt Register i



Symbol	Address	After Reset
RMAD0	0012_{16} - 0010_{16}	000000_{16}
RMAD1	0016_{16} - 0014_{16}	000000_{16}
RMAD2	$001A_{16}$ - 0018_{16}	000000_{16}
RMAD3	$001E_{16}$ - $001C_{16}$	000000_{16}

Function	Setting Range	RW
Addressing Register for the Address Match Interrupt	000000_{16} to $FFFFFF_{16}$	RW

Figure 10.12 AIER Register and RMAD0 to RMAD7 Registers

10.11 Intelligent I/O Interrupt and CAN Interrupt

The intelligent I/O interrupt and CAN interrupt are assigned to software interrupt numbers 44 to 54, and 57. Figure 10.13 shows a block diagram of the intelligent I/O interrupt and CAN interrupt. Figure 10.14 shows the IIOiIR register (i = 0 to 11). Figure 10.15 shows the IIOiIE register.

When using the intelligent I/O interrupt or CAN interrupt, set the IRLT bit in the IIOiIE register to "1" (interrupt request for interrupt used).

Various interrupt requests cause the intelligent I/O interrupt to occur. When an interrupt request is generated with intelligent I/O or CAN functions, the corresponding bit in the IIOiIR register is set to "1" (interrupt requested). When the corresponding bit in the IIOiIE register is set to "1" (interrupt enabled), the IR bit in the corresponding IIOiIC register is set to "1" (interrupt requested).

After the IR bit setting changes from "0" to "1", the IR bit remains set to "1" when a bit in the IIOiIR register is set to "1" by another interrupt request and the corresponding bit in the IIOiIE register is set to "1".

Bits in the IIOiIR register are not set to "0" automatically, even if an interrupt is acknowledged. Set each bit to "0" by program. If these bits remain set to "1", all generated interrupt requests are ignored.

CAN interrupt uses bit 7 in the IIO9IR to IIO11IR registers and bit 7 in the IIO9IE to IIO11IE registers. IIO9IR to IIO11IR registers share addresses with the CAN0IC to CAN2IC registers. Refer to **22.3 CAN Interrupt** for details.

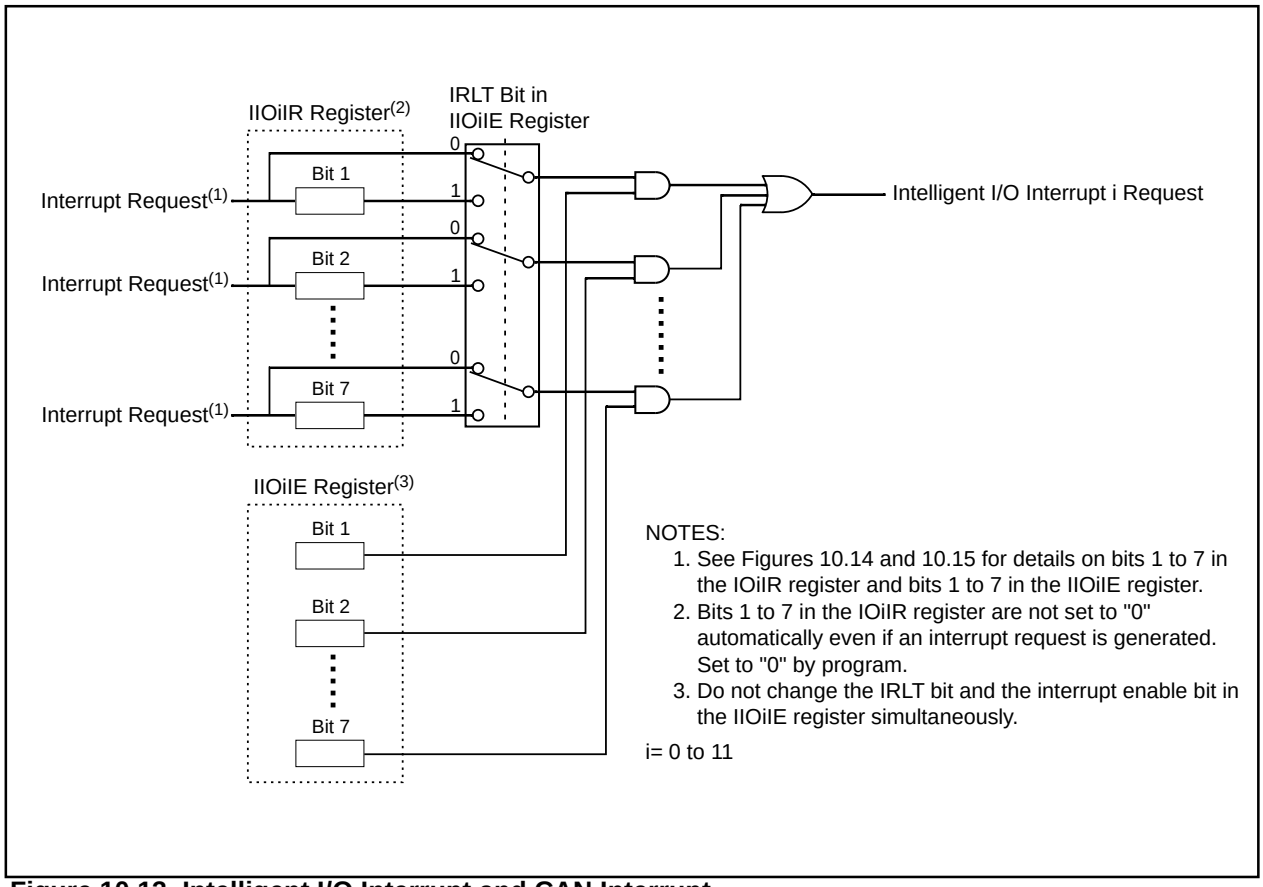
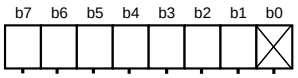


Figure 10.13 Intelligent I/O Interrupt and CAN Interrupt

When using the intelligent I/O interrupt or CAN interrupt to activate DMA II, set the IRLT bit in the IIOiIE register to "0" (an interrupt used for DMAC, DMAC II) to enable the interrupt request that the IIOiIE register requires.

Interrupt Request Register



Symbol	Address	After Reset
IIO0IR to IIO11IR	See below	0000 000X2

Bit Symbol	Function	RW
——— (b0)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.	—
(Note 1)	0 : Requests no interrupt 1 : Requests an interrupt (Note 2)	RW
(Note 1)		RW
(Note 1)		RW
(Note 1)		RW
(Note 1)		RW
(Note 1)		RW
(Note 1)		RW

NOTES:
1. See table below for bit symbols.
2. Only "0" can be set (nothing is changed even if "1" is set).

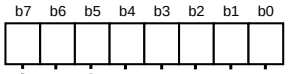
Bit Symbols for the Interrupt Request Register

Symbol	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IIO0IR	00A016	-	-	SIO0RR	G0RIR	-	PO13R	TM02R	-
IIO1IR	00A116	-	-	SIO0TR	G0TOR	-	PO14R	TM00R/PO00R	-
IIO2IR	00A216	-	-	SIO1RR	G1RIR	-	TM12R/PO12R	-	-
IIO3IR	00A316	-	-	SIO1TR	G1TOR	PO27R	PO10R	TM03R	-
IIO4IR	00A416	SRT0R	SRT1R	-	BT1R	PO32R	TM17R/PO17R	TM04R/PO04R	-
IIO5IR	00A516	-	-	-	SIO2RR	PO33R	PO21R	TM05R/PO05R	-
IIO6IR	00A616	-	-	-	SIO2TR	PO34R	PO20R	TM06R	-
IIO7IR	00A716	IE0R	-	-	BT0R	PO35R	PO22R	TM07R	-
IIO8IR	00A816	IE1R	IE2R	-	BT2R	PO36R	PO23R	TM11R/PO11R	-
IIO9IR	00A916	CAN0R	-	-	SIO3RR	PO31R	PO24R	PO15R	-
IIO10IR	00AA16	CAN1R	-	-	SIO3TR	PO30R	PO25R	TM16R/PO16R	-
IIO11IR	00AB16	CAN2R	-	-	BT3R	PO37R	PO26R	TM01R/PO01R	-

BTiR : Intelligent I/O Group i Base Timer Interrupt Request Bit (i=0 to 3)
TMijR : Intelligent I/O Group i Time Measurement j Interrupt Request Bit (j=0 to 7)
POijR : Intelligent I/O Group i Waveform Generation Function j Interrupt Request Bit
SIOiRR/SIOiTR : Intelligent I/O Group i Communication Function Interrupt Request Bit (RR:receive, TR:transmit)
GiRIR/GiTOR : Intelligent I/O Group i HDLC Data Processing Function Interrupt Request Bit (RIR:input to receive, TOR:input to transmit)
SRTiR : Intelligent I/O Group i Special Communication Function Interrupt Request Bit (i=0,1)
IEkR : Intelligent I/O Group 2 IEBus Communication Function Interrupt Request Bit (k = 0 to 2)
CANkR : CAN Communication Function Interrupt Request Bit
- : Reserved bit. Set to "0".

Figure 10.14 IIO0IR to IIO11IR Registers

Interrupt Enable Register



Symbol: IIO0IE to IIO11IE | Address: See below | After Reset: 00_{16}

Bit Symbol	Bit Name	Function	RW
IRLT	Interrupt Request Select Bit(2)	0 : Interrupt request is used for DMAC, DMAC II 1 : Interrupt request is used for interrupt	RW
(Note 1)	———	0 : Disables an interrupt by bit 1 in IIOiIR register 1 : Enables an interrupt by bit 1 in IIOiIR register	RW
(Note 1)	———	0 : Disables an interrupt by bit 2 in IIOiIR register 1 : Enables an interrupt by bit 2 in IIOiIR register	RW
(Note 1)	———	0 : Disables an interrupt by bit 3 in IIOiIR register 1 : Enables an interrupt by bit 3 in IIOiIR register	RW
(Note 1)	———	0 : Disables an interrupt by bit 4 in IIOiIR register 1 : Enables an interrupt by bit 4 in IIOiIR register	RW
(Note 1)	———	0 : Disables an interrupt by bit 5 in IIOiIR register 1 : Enables an interrupt by bit 5 in IIOiIR register	RW
(Note 1)	———	0 : Disables an interrupt by bit 6 in IIOiIR register 1 : Enables an interrupt by bit 6 in IIOiIR register	RW
(Note 1)	———	0 : Disables an interrupt by bit 7 in IIOiIR register 1 : Enables an interrupt by bit 7 in IIOiIR register	RW

NOTES:
1. See table below for bit symbols.
2. If an interrupt request is used for interrupt, set bit 1 to 7 to "1" after the IRLT bit is set to "1".

Bit Symbols for the Interrupt Enable Register

Symbol	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IIO0IE	$00B0_{16}$	-	-	SIO0RE	G0RIE	-	PO13E	TM02E	IRLT
IIO1IE	$00B1_{16}$	-	-	SIO0TE	G0TOE	-	PO14E	TM00E/PO00E	IRLT
IIO2IE	$00B2_{16}$	-	-	SIO1RE	G1RIE	-	TM12E/PO12E	-	IRLT
IIO3IE	$00B3_{16}$	-	-	SIO1TE	G1TOE	PO27E	PO10E	TM03E	IRLT
IIO4IE	$00B4_{16}$	SRT0E	SRT1E	-	BT1E	PO32E	TM17E/PO17E	TM04E/PO04E	IRLT
IIO5IE	$00B5_{16}$	-	-	-	SIO2RE	PO33E	PO21E	TM05E/PO05E	IRLT
IIO6IE	$00B6_{16}$	-	-	-	SIO2TE	PO34E	PO20E	TM06E	IRLT
IIO7IE	$00B7_{16}$	IE0E	-	-	BT0E	PO35E	PO22E	TM07E	IRLT
IIO8IE	$00B8_{16}$	IE1E	IE2E	-	BT2E	PO36E	PO23E	TM11E/PO11E	IRLT
IIO9IE	$00B9_{16}$	CAN0E	-	-	SIO3RE	PO31E	PO24E	PO15E	IRLT
IIO10IE	$00BA_{16}$	CAN1E	-	-	SIO3TE	PO30E	PO25E	TM16E/PO16E	IRLT
IIO11IE	$00BB_{16}$	CAN2E	-	-	BT3E	PO37E	PO26E	TM01E/PO01E	IRLT

BTiE : Intelligent I/O Group i Base Timer Interrupt Enable Bit (i=0 to 3)
TMijE : Intelligent I/O Group i Time Measurement j Interrupt Enable Bit (j=0 to 7)
POijE : Intelligent I/O Group i Waveform Generation Function j Interrupt Enable Bit
SIOiRE/SIOiTE : Intelligent I/O Group i Communication Function Interrupt Enable Bit (RE:receive, TE:transmit)
GiRIE/GiTOE : Intelligent I/O Group i HDLC Data Processing Function Interrupt Enable Bit (RIE:input to receive, TOE:input to transmit)
SRTiE : Intelligent I/O Group i Special Communication Function Interrupt Enable Bit (i=0,1)
IEkE : Intelligent I/O Group 2 IEBus Communication Function Interrupt Enable Bit (k=0 to 2)
CANkE : CAN Communication Function Interrupt Enable Bit
- : Reserved bit. Set to "0".

Figure 10.15 IIO0IE to IIO11IE Registers

11. Watchdog Timer

The watchdog timer detects a program which is out of control. The watchdog timer contains a 15-bit counter which is decremented by the CPU clock that the prescaler divides. The CM06 bit in the CM0 register determines whether the watchdog timer interrupt request or reset is generated when the watchdog timer underflows. The CM06 bit can be set to "1" (reset) only. Once the CM06 bit is set to "1", it cannot be changed to "0" (watchdog timer interrupt) by program. The CM06 bit is set to "0" only after reset.
When the main clock, on-chip oscillator clock, or the PLL clock runs as the CPU clock, the WDC7 bit in the WDC register determines whether the prescaler divides by 16 or by 128. When the sub clock runs as the CPU clock, the prescaler divides by 2 regardless of the WDC7 bit setting. Watchdog timer cycle is calculated as follows. Marginal errors, due to the prescaler, may occur in watchdog timer cycle.

When the main clock, on-chip oscillator clock, or PLL clock is selected as the CPU clock:

$$\text{Watchdog timer cycle} = \frac{\text{Divide by 16 or 128 prescaler x counter value of watchdog timer (32768)}}{\text{CPU clock}}$$

When the sub clock is selected as the CPU clock,

$$\text{Watchdog timer cycle} = \frac{\text{Divided by 2 prescaler x counter value of watchdog timer (32768)}}{\text{CPU clock}}$$

For example, if the CPU clock frequency is 30MHz and the prescaler divides by 16, watchdog timer cycle is approximately 17.5 ms.

The watchdog timer is reset when the WDTS register is set and when a watchdog timer interrupt request is generated. The prescaler is reset only when the microcomputer is reset. Both watchdog timer and prescaler stop after reset. They begin counting when the WDTS register is set.
The watchdog timer and prescaler stop in stop mode, wait mode and hold state. They resume counting from the value held when the mode or state is exited.
Figure 11.1 shows a block diagram of the watchdog timer. Figure 11.2 shows registers associated with the watchdog timer.

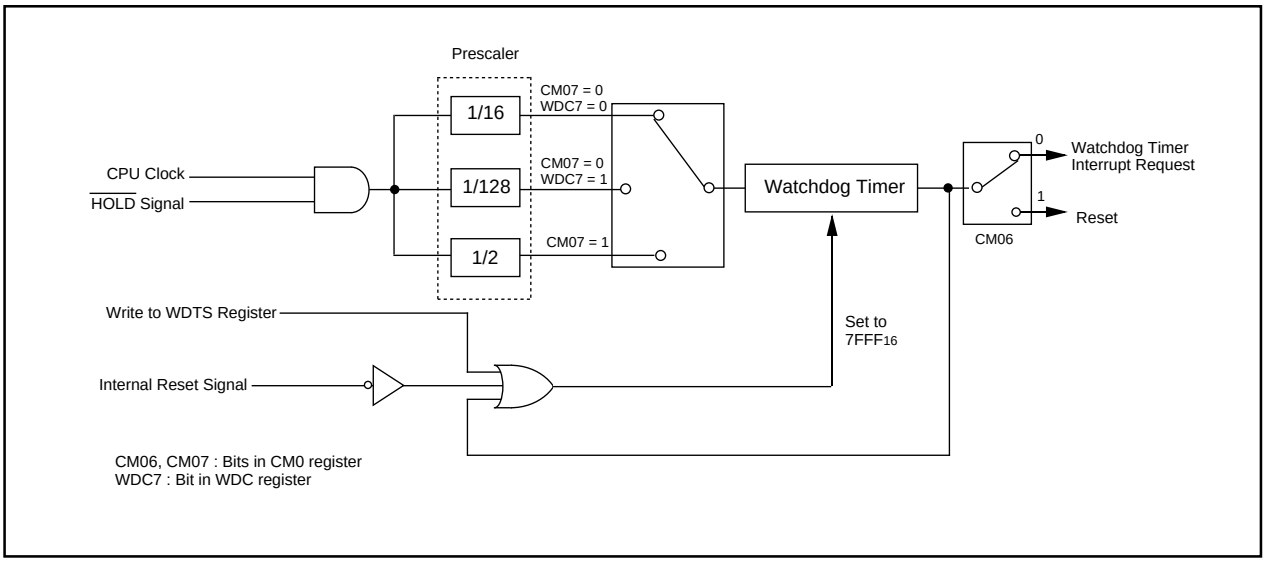


Figure 11.1 Watchdog Timer Block Diagram

Watchdog Timer Control Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0					

Symbol	Address	After Reset
WDC	$000F_{16}$	$000X\ XXXX_2$

Bit Symbol	Bit Name	Function	RW
——— (b4 - b0)	High-Order Bit of Watchdog Timer		RO
——— (b6 - b5)	Reserved Bit	Set to "0"	RW
WDC7	Prescaler Select Bit	0 : Divide-by-16 1 : Divide-by-128	RW

Watchdog Timer Start Register

b7	b0

Symbol	Address	After Reset
WDTS	$000E_{16}$	Indeterminate

Function	RW
The watchdog timer is reset to start counting by a write instruction to the WDTS register. Default value of the watchdog timer is always set to "$7FFF_{16}$" regardless of the value written.	WO

Figure 11.2 WDC Register and WDTS Register

System Clock Control Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
				1			

Symbol	Address	After Reset
CM0	0006_{16}	$0000\ X000_2$

Bit Symbol	Bit Name	Function	RW
CM00	Clock Output Function Select Bit(2)	b1 b0 0 0 : I/O port $P5_3$ 0 1 : Outputs f_C 1 0 : Outputs f_8 1 1 : Outputs f_{32}	RW
CM01			RW
CM02	In Wait Mode, Peripheral Function Clock Stop Bit	0 : Peripheral clock does not stop in wait mode 1 : Peripheral clock stops in wait mode(3)	RW
$\overline{\text{(b3)}}$	Reserved Bit	Set to "1"	RW
CM04	Port X_C Switch Bit	0 : I/O port function 1 : X_{CIN}-X_{COUT} oscillation function(4)	RW
CM05	Main Clock (X_{IN}-X_{OUT}) Stop Bit(5)	0 : Main clock oscillates 1 : Main clock stops(6)	RW
CM06	Watchdog Timer Function Select Bit	0 : Watchdog timer interrupt 1 : Reset(7)	RW
CM07	System Clock Select Bit(8)	0 : Selects X_{IN} - X_{OUT} 1 : Selects X_{CIN} - X_{COUT}	RW

NOTES:
1. Rewrite the CM0 register after the PRC0 bit in the PRCR register is set to "1" (write enable).
2. When the PM07 bit in the PM0 register is set to "0" (BCLK output), set the CM01 to CM00 bits to "00_2". When the PM15 to PM14 bits in the PM1 register is set to "01_2" (ALE output to $P5_3$), set the CM01 to CM00 bits to "00_2". When the PM07 bit is set to "1" (function selected in the CM01 to CM00 bits) in microprocessor or memory expansion mode, and the CM01 to CM00 bits are set to "00_2", an "L" signal is output from port $P5_3$ (port $P5_3$ does not function as an I/O port).
3. f_{C32} does not stop. When the CM02 bit is set to "1", the PLL clock cannot be used in wait mode.
4. When setting the CM04 bit to "1" (X_{CIN}-X_{COUT} oscillation), set the PD8_7 to PD8_6 bits to "00_2" (with port $P8_7$ and $P8_6$ input mode) and the PU25 bit in the PUR2 register to "0" (no pull-up).
5. When entering the low-power consumption mode or on-chip oscillator low-power consumption mode, the CM05 bit stops the main clock. The CM05 bit cannot detect whether the main clock stops or not. To stop the main clock, set the CM05 bit to "1" after the CM07 bit is set to "1" with a stable sub clock oscillation or after the CM21 bit in the CM2 register is set to "1" (on-chip oscillator clock). When the CM05 bit is set to "1", X_{OUT} becomes "H". The internal feedback resistance remains ON. X_{IN} is pulled up to X_{OUT} ("H" level) via the feedback resistance.
6. When the CM05 bit is set to "1", the MCD register is set to "08_{16}" (divide-by-8 mode). In on-chip oscillation mode, the MCD register is not divided by eight even if the CM05 bit terminates X_{IN}-X_{OUT}.
7. Once the CM06 bit is set to "1", it cannot be set "0" by program.
8. After the CM04 bit is set to "1" with a stable sub clock oscillation, set the CM07 bit to "1" from "0". After the CM05 bit is set to "0" with a stable main clock oscillation, set the CM07 bit to "0" from "1". Do not set the CM07 bit and CM04 or CM05 bits simultaneously.

Figure 11.3 CM0 Register

12. DMAC

This microcomputer contains four DMAC (direct memory access controller) channels that allow data to be sent to memory without using the CPU. DMAC transmits a 8- or 16-bit data from a source address to a destination address whenever a transmit request occurs. DMA0 and DMA1 must be prioritized when using DMAC. DMAC2 and DMAC3 share registers required for high-speed interrupts. High-speed interrupts cannot be used when using three or more DMAC channels.

The CPU and DMAC use the same data bus, but DMAC has a higher bus access privilege than the CPU. The cycle-steal method employed by DMAC enables high-speed operation between a transfer request and the complete transmission of 16-bit (word) or 8-bit (byte) data. Figure 12.1 shows a mapping of registers used for DMAC. Table 12.1 lists specifications of DMAC. Figures 12.2 to 12.5 show registers associated with DMAC.

Because the registers shown in Figure 12.1 are allocated to the CPU, use the LDC instruction to write to the registers. To set DCT2, DCT3, DRC2, DRC3, DMA2 and DMA3 registers, set the B flag to "1" (register bank 1) and set R0 to R3, A0, A1 registers with the MOV instruction.

To set DSA2 and DSA3 registers, set the B flag to "1" and set the SB, FB, SVP, VCT registers with the LDC instruction. To set the DRA2 and DRA3 registers, set the SVP, VCT registers with the LDC instruction.

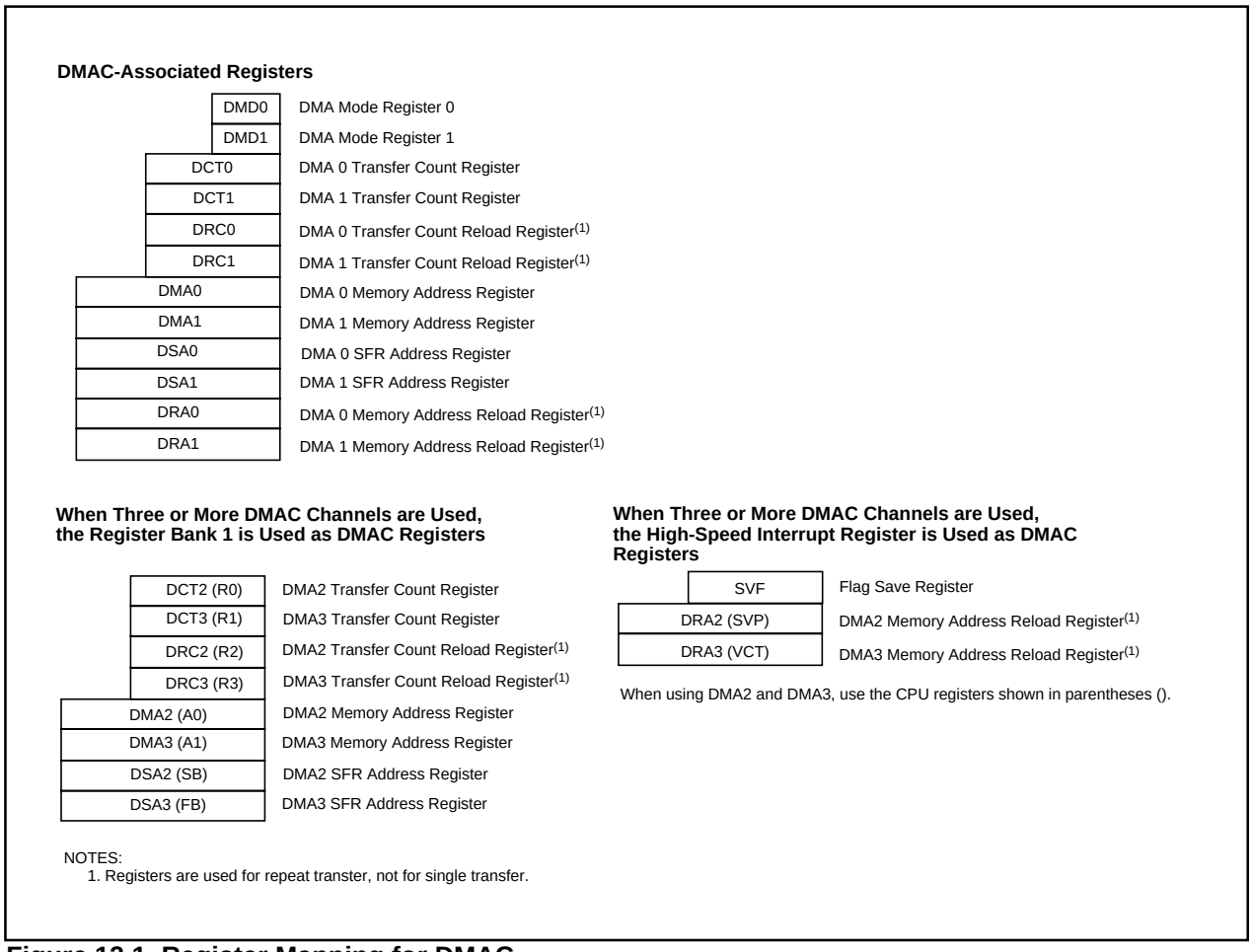


Figure 12.1 Register Mapping for DMAC

DMAC starts a data transfer by setting the DSR bit in the DMiSL register (i=0 to 3) or by using an interrupt request, generated by the functions determined by the DSEL 4 to DSEL0 bits in the DMiSL register, as a DMA request. Unlike interrupt requests, the I flag and interrupt control register do not affect DMA. Therefore, a DMA request can be acknowledged even if interrupt is disabled and cannot be acknowledged. In addition, the IR bit in the interrupt control register does not changed when a DMA request is acknowledged.

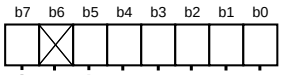
Table 12.1 DMAC Specifications

Item		Specification
Channels		4 channels (cycle-steal method)
Transfer Memory Space		• From a desired address in a 16M-byte space to a fixed address in a 16M-byte space • From a fixed address in a 16M-byte space to a desired address in a 16M-byte space
Maximum Bytes Transferred		128K bytes (when a 16-bit data is transferred) or 64K bytes (when an 8-bit data is transferred)
DMA Request Factors(1)		Falling edge or both edges of input signals to the $\overline{INT0}$ to $\overline{INT3}$ pins Timer A0 to timer A4 interrupt requests Timer B0 to timer B5 interrupt requests UART0 to UART4 transmit and receive interrupt requests A/D conversion interrupt request Intelligent I/O interrupt request CAN interrupt request Software trigger
Channel Priority		DMA0 > DMA1 > DMA2 > DMA3 (DMA0 has highest priority)
Transfer Unit		8 bits, 16 bits
Destination Address		Forward/fixed (forward and fixed directions cannot be specified when specifying source and destination addresses simultaneously)
Transfer Mode	Single Transfer	Transfer is completed when the DCTi register (i = 0 to 3) is set to "0000_{16}"
	Repeat Transfer	When the DCTi register is set to "0000_{16}", the value of the DRCi register is reloaded into the DCTi register and the DMA transfer is continued
DMA Interrupt Request Generation Timing		When the DCTi register changes "0001_{16}" to "0000_{16}"
DMA Startup	Single Transfer	DMA starts when a DMA request is generated after the DCTi register is set to "0001_{16}" or more and the MDi1 to MD0 bits in the DMDj register (j = 0 to 1) are set to "01_2" (single transfer)
	Repeat Transfer	DMA starts when a DMA request is generated after the DCTi register is set to "0001_{16}" or more and the MDi1 to MDi0 bits are set to "11_2" (repeat transfer)
DMA Stop	Single Transfer	DMA stops when the MDi1 to MDi0 bits are set to "00_2" (DMA disabled) or when the DCTi register is set to "0000_{16}" (0 DMA transfer) by DMA transfer or write
	Repeat Transfer	DMA stops when the MDi1 to MDi0 bits are set to "00_2" or when the DCTi register is set to "0000_{16}" and the DRCi register set to "0000_{16}"
Reload Timing to the DCTi or DMAi Register		When the DCTi register is set to "0000_{16}" from "0001_{16}" in repeat transfer mode
DMA Transfer Cycles		Minimum 3 cycles

NOTES:

1. The IR bit in the interrupt control register does not changed when a DMA request is acknowledged.

DMAi Request Factor Select Register (i=0 to 3)



Symbol	Address	After Reset
DM0SL to DM3SL	0378_{16}, 0379_{16}, $037A_{16}$, $037B_{16}$	$0X00\ 0000_2$

Bit Symbol	Bit Name	Function	RW
DSEL0	DMA Request Cause Select Bit(1)	See Table 12.2 about DMiSL register (i = 0 to 3) function	RW
DSEL1			RW
DSEL2			RW
DSEL3			RW
DSEL4			RW
DSR	Software DMA Request Bit(2)	When a software trigger is selected, a DMA request is generated by setting this bit to "1" (When read, its content is always "0")	RW
____ (b6)	Nothing is assigned. When write, set "0". When read, its content is indeterminate.		—
DRQ	DMA Request Bit(2, 3)	0 : Not requested 1 : Requested	RW

NOTES:
1. Change the DSEL4 to DSEL0 bits while the MDi1 to MDi0 bits in the DMA0 or DMD1 register are set to "00_2" (DMA disabled). Also, set the DRQ bit to "1" simultaneously when the DSEL4 to DSEL0 bits are changed.
   e.g MOV.B #083h, DMiSL ; Set timer A0
2. When the DSR bit is set to "1", set the DRQ bit to "1" simultaneously.
   e.g OR.B #0A0h, DMiSL
3. Do not write "0" to this bit.

Figure 12.2 DM0SL to DM3SL Registers

Table 12.2 DMiSL Register (i = 0 to 3) Function

Setting Value	DMA Request Cause				
b4 b3 b2 b1 b0	DMA0	DMA1	DMA2	DMA3	
0 0 0 0 0	Software Trigger				
0 0 0 0 1	Falling edge of INT0	Falling edge of INT1	Falling edge of INT2	Falling edge of INT3(1)	(Note 2)
0 0 0 1 0	Both edges of INT0	Both edges of INT1	Both edges of INT2	Both edges of INT3(1)	(Note 2)
0 0 0 1 1	Timer A0 Interrupt Request				
0 0 1 0 0	Timer A1 Interrupt Request				
0 0 1 0 1	Timer A2 Interrupt Request				
0 0 1 1 0	Timer A3 Interrupt Request				
0 0 1 1 1	Timer A4 Interrupt Request				
0 1 0 0 0	Timer B0 Interrupt Request				
0 1 0 0 1	Timer B1 Interrupt Request				
0 1 0 1 0	Timer B2 Interrupt Request				
0 1 0 1 1	Timer B3 Interrupt Request				
0 1 1 0 0	Timer B4 Interrupt Request				
0 1 1 0 1	Timer B5 Interrupt Request				
0 1 1 1 0	UART0 Transmit Interrupt Request				
0 1 1 1 1	UART0 Receive or ACK Interrupt Request(3)				
1 0 0 0 0	UART1 Transmit Interrupt Request				
1 0 0 0 1	UART1 Receive or ACK Interrupt Request(3)				
1 0 0 1 0	UART2 Transmit Interrupt Request				
1 0 0 1 1	UART2 Receive or ACK Interrupt Request(3)				
1 0 1 0 0	UART3 Transmit Interrupt Request				
1 0 1 0 1	UART3 Receive or ACK Interrupt Request(3)				
1 0 1 1 0	UART4 Transmit Interrupt Request				
1 0 1 1 1	UART4 Receive or ACK Interrupt Request(3)				
1 1 0 0 0	A/D0 Interrupt Request	A/D1 Interrupt Request	A/D0 Interrupt request	A/D1 Interrupt Request	
1 1 0 0 1	Intelligent I/O Interrupt 0 Request	Intelligent I/O Interrupt 7 Request	Intelligent I/O Interrupt 2 Request	Intelligent I/O Interrupt 9 Request(4)	
1 1 0 1 0	Intelligent I/O Interrupt 1 Request	Intelligent I/O Interrupt 8 Request	Intelligent I/O Interrupt 3 Request	Intelligent I/O Interrupt 10 Request(5)	
1 1 0 1 1	Intelligent I/O Interrupt 2 Request	Intelligent I/O Interrupt 9 Request(4)	Intelligent I/O Interrupt 4 Request	Intelligent I/O Interrupt 11 Request(6)	
1 1 1 0 0	Intelligent I/O Interrupt 3 Request	Intelligent I/O Interrupt 10 Request(5)	Intelligent I/O Interrupt 5 Request	Intelligent I/O Interrupt 0 Request	
1 1 1 0 1	Intelligent I/O Interrupt 4 Request	Intelligent I/O Interrupt 11 Request(6)	Intelligent I/O Interrupt 6 Request	Intelligent I/O Interrupt 1 Request	
1 1 1 1 0	Intelligent I/O Interrupt 5 Request	Intelligent I/O Interrupt 0 Request	Intelligent I/O Interrupt 7 Request	Intelligent I/O Interrupt 2 Request	
1 1 1 1 1	Intelligent I/O Interrupt 6 Request	Intelligent I/O Interrupt 1 Request	Intelligent I/O Interrupt 8 Request	Intelligent I/O Interrupt 3 Request	

NOTES:
1. If the $\overline{\text{INT3}}$ pin is used as data bus in the memory expansion mode or microprocessor mode, a DMA3 interrupt request cannot be generated by an input signal to the $\overline{\text{INT3}}$ pin.
2. The falling edge and both edges of input signal into the $\overline{\text{INTj}}$ pin (j = 0 to 3) cause a DMA request. The $\overline{\text{INT}}$ interrupt (the POL bit in the INTjIC register, the LVS bit, the IFSR register) is not affected and vice versa.
3. The UkSMR register and UkSMR2 register (k = 0 to 4) switch the UARTj receive to ACK or ACK to UARTk receive.
4. The same setting is used to generate an intelligent I/O interrupt 9 request and a CAN interrupt 0 request.
5. The same setting is used to generate an intelligent I/O interrupt 10 request and a CAN interrupt 1 request.
6. The same setting is used to generate an intelligent I/O interrupt 11 request and a CAN interrupt 2 request.

DMA Mode Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
DMD0	CPU Internal Register	00₁₆

Bit Symbol	Bit Name	Function	RW
MD00	Channel 0 Transfer Mode Select Bit	b1 b0 0 0 : DMA disabled 0 1 : Single transfer 1 0 : Do not set to this value 1 1 : Repeat transfer	RW
MD01			RW
BW0	Channel 0 Transfer Unit Select Bit	0 : 8 bits 1 : 16 bits	RW
RW0	Channel 0 Transfer Direction Select Bit	0 : Fixed address to memory (forward direction) 1 : Memory (forward direction) to fixed address	RW
MD10	Channel 1 Transfer Mode Select Bit	b5 b4 0 0 : DMA disabled 0 1 : Single transfer 1 0 : Do not set to this value 1 1 : Repeat transfer	RW
MD11			RW
BW1	Channel 1 Transfer Unit Select Bit	0 : 8 bits 1 : 16 bits	RW
RW1	Channel 1 Transfer Direction Select Bit	0 : Fixed address to memory (forward direction) 1 : Memory (forward direction) to fixed address	RW

NOTES:
1. Use the LDC instruction to set the DMD0 register.

DMA Mode Register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0

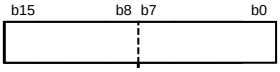
Symbol	Address	After Reset
DMD1	CPU Internal Register	00₁₆

Bit Symbol	Bit Name	Function	RW
MD20	Channel 2 Transfer Mode Select Bit	b1 b0 0 0 : DMA disabled 0 1 : Single transfer 1 0 : Do not set to this value 1 1 : Repeat transfer	RW
MD21			RW
BW2	Channel 2 Transfer Unit Select Bit	0 : 8 bits 1 : 16 bits	RW
RW2	Channel 2 Transfer Direction Select Bit	0 : Fixed address to memory (forward direction) 1 : Memory (forward direction) to fixed address	RW
MD30	Channel 3 Transfer Mode Select Bit	b5 b4 0 0 : DMA disabled 0 1 : Single transfer 1 0 : Do not set to this value 1 1 : Repeat transfer	RW
MD31			RW
BW3	Channel 3 Transfer Unit Select Bit	0 : 8 bits 1 : 16 bits	RW
RW3	Channel 3 Transfer Direction Select Bit	0 : Fixed address to memory (forward direction) 1 : Memory (forward direction) to fixed address	RW

NOTES:
1. Use the LDC instruction to set the DMD1 register.

Figure 12.3 DMD0 Register, DMD1 Register

DMAi Transfer Count Register (i=0 to 3)

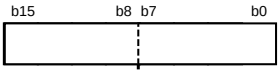


Symbol	Address	After Reset
DCT0(2)	(CPU Internal Register)	XXXX16
DCT1(2)	(CPU Internal Register)	XXXX16
DCT2(bank1;R0)(3)	(CPU Internal Register)	000016
DCT3(bank1;R1)(4)	(CPU Internal Register)	000016

Function	Setting Range	RW
Set the number of transfers	0000$_{16}$ to FFFF$_{16}$(1)	RW

NOTES:
1. When the DCTi register to "0000$_{16}$", no data transfer occurs regardless of a DMA request.
2. Use the LDC instruction to set the DCT0 and DCT1 registers.
3. To set the DCT2 register, set the B flag in the FLG register to "1" (register bank 1) and set R0 register. Use the MOV instruction to set the DCT2 register.
4. To set the DCT3 register, set the B flag to "1" and set R1 register. Use the MOV instruction to set the DCT3 register.

DMAi Transfer Count Reload Register (i=0 to 3)



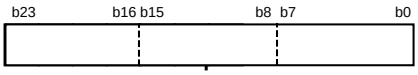
Symbol	Address	After Reset
DRC0(1)	(CPU Internal Register)	XXXX16
DRC1(1)	(CPU Internal Register)	XXXX16
DRC2(bank1;R2)(2)	(CPU Internal Register)	0000$_{16}$
DRC3(bank1;R3)(3)	(CPU Internal Register)	0000$_{16}$

Function	Setting Range	RW
Set the number of transfers	0000$_{16}$ to FFFF$_{16}$	RW

NOTES:
1. Use the LDC instruction to set the DRC0 and DRC1 registers.
2. To set the DRC2 register, set the B flag in the FLG register to "1" (register bank 1) and set R2 register. Use the MOV instruction to set the DRC2 register.
3. To set the DRC3 register, set the B flag to "1" and set R3 register. Use the MOV instruction to set the DRC3 register.

Figure 12.4 DCT0 to DCT3 Registers and DRC0 to DRC3 Registers

DMAi Memory Address Register (i=0 to 3)

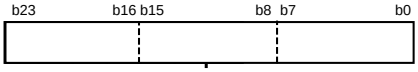


Symbol	Address	After Reset
DMA0(2)	(CPU Internal Register)	XXXXXX16
DMA1(2)	(CPU Internal Register)	XXXXXX16
DMA2(bank1;A0)(3)	(CPU Internal Register)	000000₁₆
DMA3(bank1;A1)(4)	(CPU Internal Register)	000000₁₆

Function	Setting Range	RW
Set a source memory address or destination memory address(1)	000000₁₆ to FFFFFF₁₆ (16M-byte space)	RW

NOTES:
1. When the RWk bit (k=0 to 3) in the DMDj register (j=0, 1)is set to "0" (fixed address to memory), a destination address is selected. When the RWk bit is set to "1" (memory to fixed address), a source address is selected.
2. Use the LDC instruction to set the DMA0 and DMA1 registers.
3. To set the DMA2 register, set the B flag in the FLG register to "1" (register bank 1) and set A0 register. Use the MOV instruction to set the DMA2 register.
4. To set the DMA3 register, set the B flag to "1" and set A1 register. Use the MOV instruction to set the DMA3 register.

DMAi SFR Address Register (i=0 to 3)

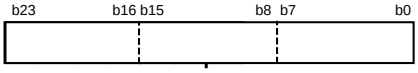


Symbol	Address	After Reset
DSA0(2)	(CPU Internal Register)	XXXXXX16
DSA1(2)	(CPU Internal Register)	XXXXXX16
DSA2(bank1;SB)(3)	(CPU Internal Register)	000000₁₆
DSA3(bank1;FB)(4)	(CPU Internal Register)	000000₁₆

Function	Setting Range	RW
Set a source fixed address or destination fixed address(1)	000000₁₆ to FFFFFF₁₆ (16M-byte space)	RW

NOTES:
1. When the RWk bit (k=0 to 3) in the DMDj register (j=0, 1) is set to "0" (fixed address to memory), a source address is selected. When the RWk bit is set to "1" (memory to fixed address), a destination address is selected.
2. Use the LDC instruction to set the DSA0 and DSA1 registers.
3. To set the DSA2 register, set the B flag in the FLG register to "1" (register bank 1) and the set the SB register. Use the LDC instruction to set the DSA2 register.
4. To set the DSA3 register, set the B flag to "1" and set the FB register. Use the LDC instruction to set the DSA3 register.

DMAi Memory Address Reload Register(1) (i=0 to 3)



Symbol	Address	After Reset
DRA0	(CPU Internal Register)	XXXXXX16
DRA1	(CPU Internal Register)	XXXXXX16
DRA2(SVP)(2)	(CPU Internal Register)	XXXXXX16
DRA3(VCT)(3)	(CPU Internal Register)	XXXXXX16

Function	Setting Range	RW
Set a source memory address or destination memory address	000000₁₆ to FFFFFF₁₆ (16M-byte space)	RW

NOTES:
1. Use the LDC instruction to set the these registers.
2. To set the DRA2 register, set the SVP register.
3. To set the DRA3 register, set the VCT register.

Figure 12.5 DMA0 to DMA3 Registers, DSA0 to DSA3 Registers and DRA0 to DRA3 Registers

12.1 Transfer Cycles

Transfer cycle contains a bus cycle to read data from a memory or the SFR area (source read) and a bus cycle to write data to a memory space or the SFR area (destination write). The number of read and write bus cycles depends on source and destination addresses. In memory expansion mode and microprocessor mode, the number of read and write bus cycles also depends on the DS register. Software wait state insertion and the $\overline{\text{RDY}}$ signal make a bus cycle longer.

12.1.1 Effect of Source and Destination Addresses

When a 16-bit data is transferred with a 16-bit data bus, and the source address starts with an odd address, source read cycle has one more bus cycle compared to a source address starting with an even address.

When a 16-bit data is transferred with a 16-bit data bus and the destination address starts with an odd address, destination write cycle has one more bus cycle compared to a destination address starting with an even address.

12.1.2 Effect of the DS Register

In an external space in memory expansion or microprocessor mode, transfer cycle varies depending on the data bus used at the source and destination addresses. See **Figure 7.1** for details about the DS register.

(1) When an 8-bit data bus (the DSi bit in the DS register is set to "0" (i=0 to 3)), accessing both source address and destination address, is used to transfer a 16-bit data, 8-bit data is transferred twice. Therefore, two bus cycles are required to read the data and another two bus cycles to write the data.

(2) When an 8-bit data bus (the DSi bit in the DS register is set to "0" (i=0 to 3)), accessing source address, and a 16-bit data bus, accessing destination address, are used to transfer a 16-bit data, 8-bit data is read twice but is written once as 16-bit data. Therefore, two bus cycles are required for reading and one bus cycle is for writing.

(3) When a 16-bit data bus, accessing source address, and an 8-bit data bus, accessing destination address, are used to transfer a 16-bit data, 16-bit data is read once and 8-bit data is written twice. Therefore, one bus cycle is required for reading and two bus cycles is for writing.

12.1.3 Effect of Software Wait State

When the SFR area or memory space with software wait states is accessed, the number of cycles is incremented by software wait states.

Figure 12.6 shows an example of a transfer cycle for the source-read bus cycle. In Figure 12.6, the number of source-read bus cycles is illustrated under different conditions, provided that the destination address is an address of an external space with two destination-write bus cycles (one bus cycle). In effect, the destination-write bus cycle is also affected by each condition and the transfer cycles change accordingly. To calculate a transfer cycle, apply respective conditions to both destination-write bus cycle and source-read bus cycle. As shown in example (2) of Figure 12.6, when an 8-bit data bus, accessing both source and destination addresses, is used to transfer a 16-bit data, two bus cycles each are required for the source-read bus cycle and destination-write bus cycle.

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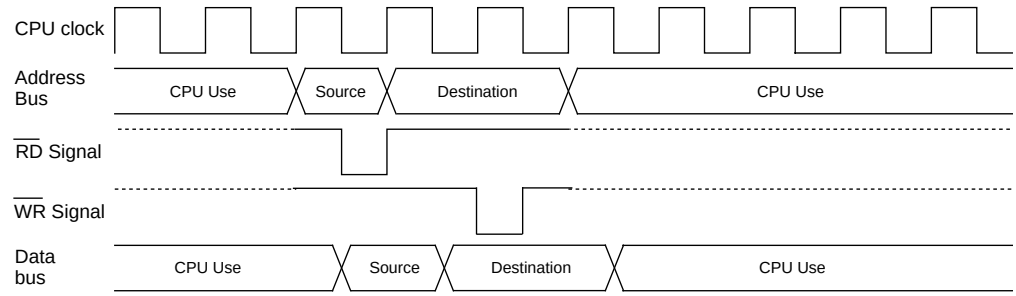
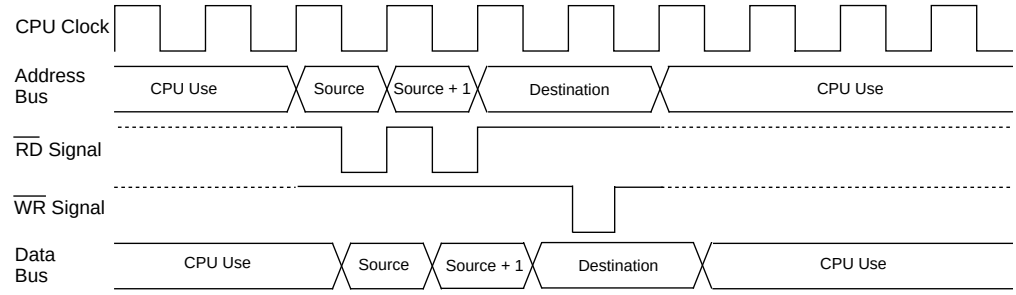
12.1.4 Effect of $\overline{\text{RDY}}$ Signal

In memory expansion or microprocessor mode, the $\overline{\text{RDY}}$ signal affects external space. Refer to **7.2.6 $\overline{\text{RDY}}$ Signal** for details.

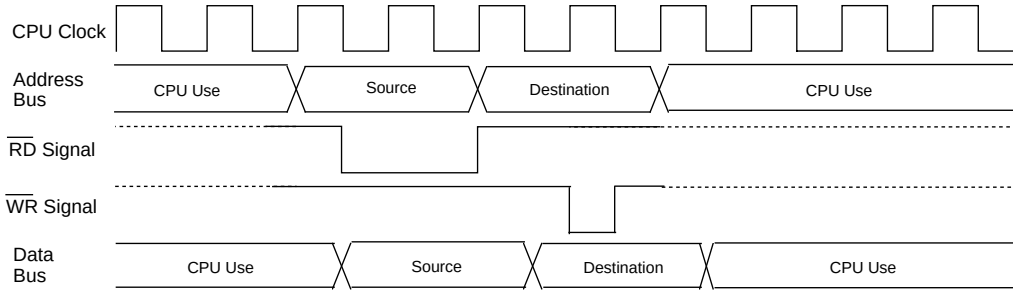
(1) When 8-bit data is transferred
or when 16-bit data is transferred from an even source address by a 16-bit data bus



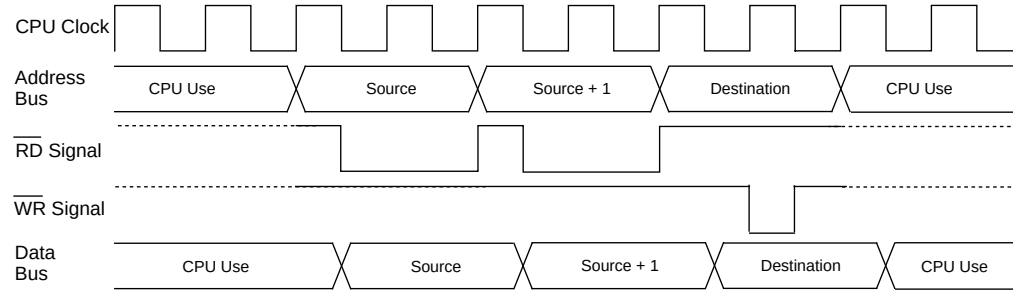
(2) When 16-bit data is transferred from an odd source address
or when 16-bit data is transferred from source by an 8-bit data bus



(3) When one wait state is inserted into the source-read bus cycle under the conditions in (1)



(4) When one wait state is inserted into the source-read bus cycle under the conditions in (2)



NOTES:
1. The above applies when the destination write cycle is 2 cycles (1 bus cycle).
However, if the destination write cycle is placed under these conditions , it will change to the sa
timing as the source-read bus cycle illustrated above.

Figure 12.6 Transfer Cycle Examples with the Source-Read Bus Cycle

12.2 DMAC Transfer Cycles

The number of DMAC transfer cycle can be calculated as follows.

Any combination of even or odd transfer read and write addresses are possible. Table 12.3 lists the number of DMAC transfer cycles. Table 12.4 lists coefficient j, k.

Transfer cycles per transfer = Number of read cycle x j + Number of write cycle x k

Table 12.3 DMAC Transfer Cycles

Transfer Unit	Bus Width	Access Address	Single-Chip Mode		Memory Expansion Mode Microprocessor Mode	
			Read Cycle	Write Cycle	Read Cycle	Write Cycle
8-bit transfers (BWi bit in the DMDp register = 0)	16-bit	Even	1	1	1	1
		Odd	1	1	1	1
	8-bit	Even	—	—	1	1
		Odd	—	—	1	1
16-bit transfers (BWi bit = 1)	16-bit	Even	1	1	1	1
		Odd	2	2	2	2
	8-bit	Even	—	—	2	2
		Odd	—	—	2	2

i= 0 to 3, p = 0 to 1

Table 12.4 Coefficient j, k

Internal Space			External Space					
Internal ROM or Internal RAM with no wait state	Internal ROM or Internal RAM with a wait state	SFR Area	Separate Bus with no wait state	Separate Bus with 1 wait state	Separate Bus with 2 wait states	Separate Bus with 3 wait states	Multiplexed Bus with 2 wait states	Multiplexed Bus with 3 wait states
j = 1 k = 1	j = 2 k = 2	j = 2 k = 2	j = 1 k = 2	j = 2 k = 2	j = 3 k = 3	j = 4 k = 4	j = 3 k = 3	j = 4 k = 4

12.3 Channel Priority and DMA Transfer Timing

When multiple DMA requests are generated in the same sampling period, between the falling edge of the CPU clock and the next falling edge, the DRQ bit in the DMiSL register (i = 0 to 3) is set to "1" (a request) simultaneously. Channel priority in this case is : DMA0 > DMA1 > DMA2 > DMA3.

Figure 12.7 shows an example of the DMA transfer by external factors.

In Figure 12.7, the DMA0 request which has the highest priority is received first to start a transfer when a DMA0 request and DMA1 request are generated simultaneously. After one DMA0 transfer is completed, the bus privilege is returned to the CPU. When the CPU has completed one bus access, the DMA1 transfer starts. After one DMA1 transfer is completed, the privilege is again returned to the CPU.

In addition, DMA requests cannot be counted up since each channel has one DRQ bit. Therefore, when DMA requests, as DMA1 in Figure 12.7, occur more than once before receiving bus privilege, the DRQ bit is set to "0" as soon as privilege is acquired. The bus privilege is returned to the CPU when one transfer is completed.

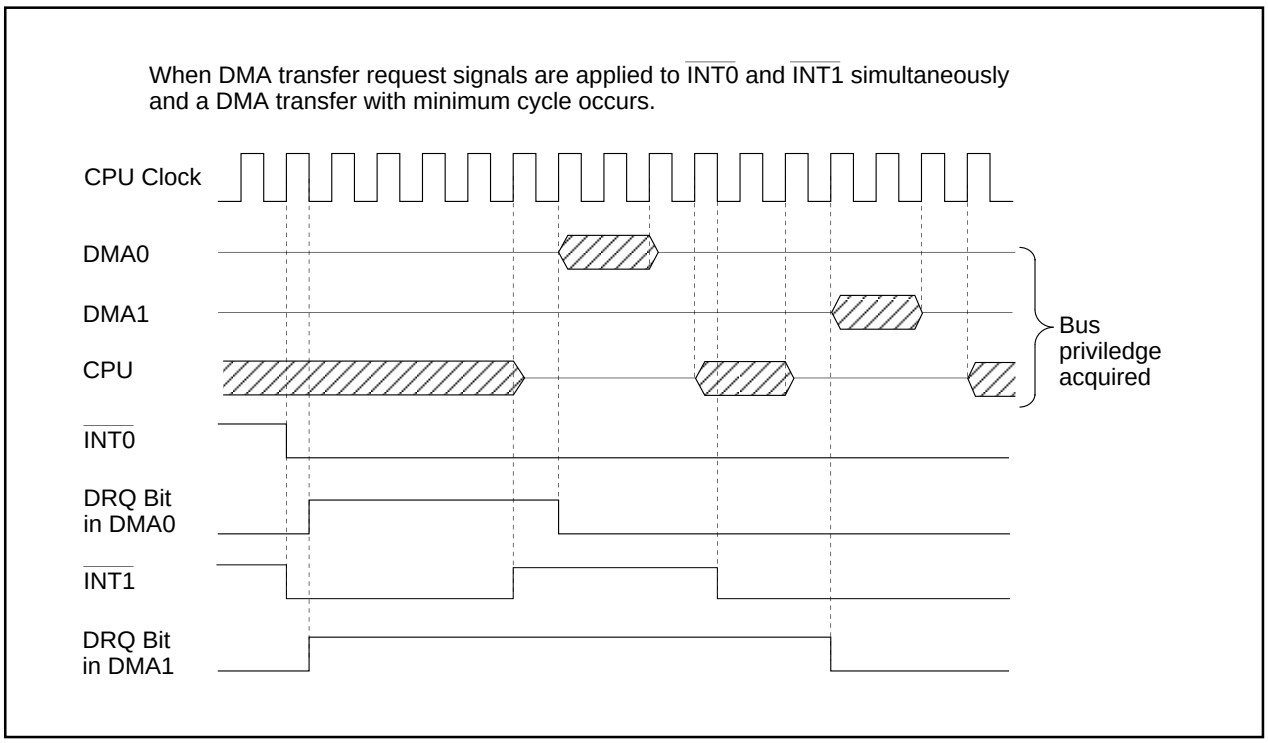


Figure 12.7 DMA Transfer by External Factors

13. DMAC II

The DMAC II performs memory-to-memory transfer, immediate data transfer and calculation transfer, which transfers the sum of two data added by an interrupt request from any peripheral functions.
Table 13.1 lists specifications of the DMAC II.

Table 13.1 DMAC II Specifications

Item	Specification
DMAC II Request Factor	Interrupt requests generated by all peripheral functions when the ILVL2 to ILVL0 bits is set to "111_2"
Transfer Data	• Data in memory is transferred to memory (memory-to-memory transfer) • Immediate data is transferred to memory (immediate data transfer) • Data in memory (or immediate data) + data in memory is transferred to memory (calculation transfer)
Transfer Block	8 bits or 16 bits
Transfer Space	64K-byte space in addresses 0000_{16} to $0FFFF_{16}$ (1, 2)
Transfer Direction	Fixed or forward address Selected separately for each source address and destination address
Transfer Mode	Single transfer, burst transfer
Chained Transfer Function	Parameters (transfer count, transfer address and other information) are switched when transfer counter reaches zero
End-of-Transfer Interrupt	Interrupt occurs when a transfer counter reaches zero
Multiple Transfer Function	Multiple data can be transferred by a generated request for one DMA II transfer

NOTES:
1. When transferring a 16-bit data to destination address $0FFFF_{16}$, it is transferred to $0FFFF_{16}$ and 10000_{16}. The same transfer occurs when the source address is $0FFFF_{16}$.
2. The actual space where transfer can occur is limited due to internal RAM capacity.

13.1 DMAC II Settings

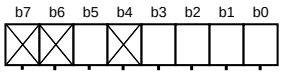
DMAC II can be made available by setting up the following registers and tables.
- RLVL register
- DMAC II Index
- Interrupt control register of the peripheral function causing a DMAC II request
- The relocatable vector table of the peripheral function causing a DMAC II request
- IRLT bit in the IIOiIE register (i = 0 to 11) when using the intelligent I/O or CAN interrupt

Refer to **10. Interrupts** for details on the IIOiIE register

13.1.1 RLVL Register

When the DMAII bit is set to "1" (DMAC II transfer) and the FSIT bit to "0" (normal interrupt), the DMAC II is activated by an interrupt request from any peripheral function with the ILVL2 to ILVL0 bits in the interrupt control register set to "111_2" (level 7).
Figure 13.1 shows the RLVL register.

Exit Priority Register



Symbol	Address	After Reset
RLVL	009F16	XXXX 00002

Bit Symbol	Bit Name	Function	RW
RLVL0	Stop/Wait Mode Exit Minimum Interrupt Priority Level Control Bit(1)	b2 b1 b0 0 0 0 : Level 0 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
RLVL1			RW
RLVL2			RW
FSIT	High-Speed Interrupt Set Bit(2)	0: Interrupt priority level 7 is used for normal interrupt 1: Interrupt priority level 7 is used for high-speed interrupt	RW
____ (b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_
DMA II	DMAC II Select Bit(3,4)	0: Interrupt priority level 7 is used for interrupt 1: Interrupt priority level 7 is used for DMAC II transfer	RW
____ (b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

NOTES:
1. The microcomputer exits stop or wait mode when the requested interrupt priority level is higher than the level set in the RLVL2 to RLVL0 bits. Set the RLVL2 to RLVL0 bits to the same value as IPL in the FLG register.
2. When the FSIT bit is set to "1" (high-speed interrupt), interrupt priority level 7 becomes the high-speed interrupt. In this case, set only one interrupt to interrupt priority level 7 and the DMA II bit to "0" (normal interrupt).
3. After reset, set the DMA II bit only once. Set the ILVl1 to ILVL0 bits after setting the DMA II bit following reset. When setting the DMA II bit to "1", set the FSIT bit to "0" (normal interrupt). The DMAC II cannot be used simultaneously with the high-speed interrupt . I flag and IPL settings do not affect DMAC II transfer.
4. After reset, the DMA II bit is indeterminate. When using an interrupt, set the interrupt control register after setting the DMA II bit to "0".

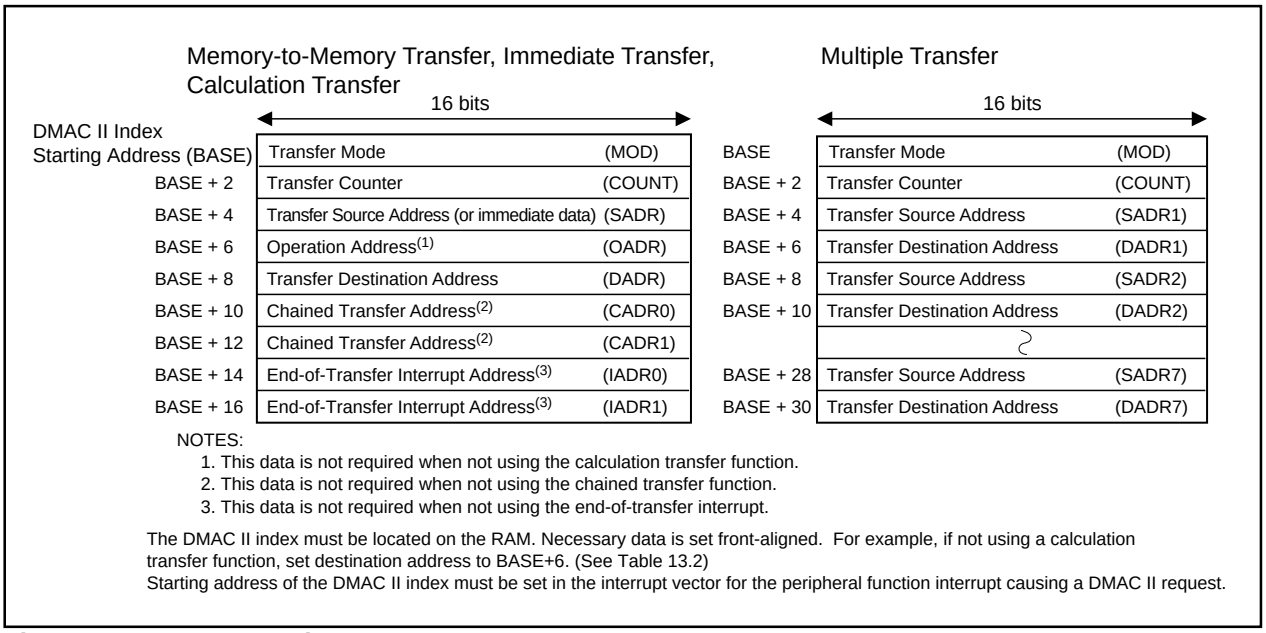
Figure 13.1 RLVL Register

13.1.2 DMAC II Index

The DMAC II index is a data table which comprises 8 to 18 bytes (maximum 32 bytes when the multiple transfer function is selected). The DMAC II index stores parameters for transfer mode, transfer counter, source address (or immediate data), operation address as an address to be calculated, destination address, chained transfer address, and end-of-transfer interrupt address.

This DMAC II index must be located on the RAM area.

Figure 13.2 shows a configuration of the DMAC II index. Table 13.2 lists a configuration of the DMAC II index in transfer mode.



NOTES:
1. This data is not required when not using the calculation transfer function.
2. This data is not required when not using the chained transfer function.
3. This data is not required when not using the end-of-transfer interrupt.

The DMAC II index must be located on the RAM. Necessary data is set front-aligned. For example, if not using a calculation transfer function, set destination address to BASE+6. (See Table 13.2)
Starting address of the DMAC II index must be set in the interrupt vector for the peripheral function interrupt causing a DMAC II request.

Figure 13.2 DMAC II Index

The followings are details of the DMAC II index. Set these parameters in the specified order listed in Table 13.2, according to DMAC II transfer mode.

- **Transfer mode (MOD)**
  Two-byte data is required to set transfer mode. Figure 13.3 shows a configuration for transfer mode.
- **Transfer counter (COUNT)**
  Two-byte data is required to set the number of transfer.
- **Transfer source address (SADR)**
  Two-byte data is required to set the source memory address or immediate data.
- **Operation address (OADR)**
  Two-byte data is required to set a memory address to be calculated. Set this data only when using the calculation transfer function.
- **Transfer destination address (DADR)**
  Two-byte data is required to set the destination memory address.
- **Chained transfer address (CADR)**
  Four-byte data is required to set the starting address of the DMAC II index for the next transfer. Set this data only when using the chained transfer function.
- **End-of-transfer interrupt address (IADR)**
  Four-byte data is required to set a jump address for end-of-transfer interrupt processing. Set this data only when using the end-of-transfer interrupt.

Table 13.2 DMAC II Index Configuration in Transfer Mode

	Memory-to-Memory Transfer /Immediate Data Transfer				Calculation Transfer				Multiple Transfer
Chained Transfer	Not Used	Used	Not Used	Used	Not Used	Used	Not Used	Used	Not Available
End-of-Transfer Interrupt	Not Used	Not Used	Used	Used	Not Used	Not Used	Used	Used	Not Available
DMAC II Index	MOD COUNT SADR DADR 8 bytes	MOD COUNT SADR DADR CADR0 CADR1 12 bytes	MOD COUNT SADR DADR IADR0 IADR1 12 bytes	MOD COUNT SADR DADR CADR0 CADR1 IADR0 IADR1 16 bytes	MOD COUNT SADR OADR DADR 10 bytes	MOD COUNT SADR OADR DADR CADR0 CADR1 14 bytes	MOD COUNT SADR OADR DADR IADR0 IADR1 14 bytes	MOD COUNT SADR OADR DADR CADR0 CADR1 IADR0 IADR1 18 bytes	MOD COUNT SADR1 DADR1 SADRi DADRi i=1 to 7 Max 32 bytes (when i=7)

Transfer Mode (MOD)(1)

b15 b8 b7 b0

Bit Symbol	Bit Name	Function (MULT=0)	Function (MULT=1)	RW
SIZE	Transfer Unit Select Bit	0: 8 bits 1: 16 bits		RW
IMM	Transfer Data Select Bit	0: Immediate data 1: Memory	Set to "1"	RW
UPDS	Transfer Source Direction Select Bit	0: Fixed address 1: Forward address		RW
UPDD	Transfer Destination Direction Select Bit	0: Fixed address 1: Forward address		RW
OPER/ CNT0(2)	Calculation Transfer Function Select Bit	0: Not used 1: Used	b6 b5 b4 0 0 0: Do not set to this value 0 0 1: Once 0 1 0: Twice : 1 1 0: 6 times 1 1 1: 7 times	RW
BRST/ CNT1(2)	Burst Transfer Select Bit	0: Single transfer 1: Burst transfer		RW
INTE/ CNT2(2)	End-of-Transfer Interrupt Select Bit	0: Interrupt not used 1: Use interrupt		RW
CHAIN	Chained Transfer Select Bit	0: Chained transfer not used 1: Use chained transfer	Set to "0"	RW
____ (b14 - b8)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.			—
MULT	Multiple Transfer Select Bit	0: Multiple transfer not used	1: Use multiple transfer	RW

NOTES:
1. The MOD register must be located on the RAM.
2. When the MULT bit is set to "0" (no multiple transfer), bits 4 to 6 becomes the OPER, BRST, INTE bits. When the MULT bit is set to "1" (multiple transfer), bits 4 to 6 becomes the CNT0 to CNT2 bits.

Figure 13.3 MOD

13.1.3 Interrupt Control Register for the Peripheral Function

For the peripheral function interrupt activating a DMAC II request, set the ILVL2 to ILVL0 bits to "111_2" (level 7).

13.1.4 Relocatable Vector Table for the Peripheral Function

Set the starting address of the DMAC II index in the interrupt vector for the peripheral function interrupt activating a DMAC II request.
When using the chained transfer, the relocatable vector table must be located in the RAM.

13.1.5 IRLT Bit in the IIOiIE Register (i=0 to 11)

When the intelligent I/O interrupt or CAN interrupt is used to activate DMAC II, set the IRLT bit in the IIOiIE register of the interrupt to "0".

13.2 DMAC II Performance

The DMAC II function is selected by setting the DMA II bit to "1" (DMAC II transfer). DMAC II request is activated by all peripheral function interrupts with the ILVL2 to ILVL0 bits set to "1112" (level 7). These peripheral function interrupt request signals become DMAC II transfer request signals and the peripheral function interrupt cannot be used.
When an interrupt request is generated by setting the ILVL2 to ILVL0 bits to "111_2" (level 7), the DMAC II is activated regardless of what state the I flag and IPL is in.

13.3 Transfer Data

The DMAC II transfers 8-bit or 16-bit data.

- Memory-to-memory transfer : Data is transferred from a desired memory location in a 64K-byte space (Addresses 00000_{16} to $0FFFF_{16}$) to another desired memory location in the same space.
- Immediate data transfer : Immediate data is transferred to a desired memory location in a 64K-byte space.
- Calculation transfer : Two 8-bit or16-bit data are added together and the result is transferred to a desired memory location in a 64K-byte space.

When a 16-bit data is transferred to the destination address $0FFFF_{16}$, it is transferred to $0FFFF_{16}$ and 10000_{16}. The same transfer occurs when the source address is $0FFFF_{16}$.

13.3.1 Memory-to-Memory Transfer

Data transfer between any two memory locations can be:

- a transfer from a fixed address to another fixed address
- a transfer from a fixed address to a relocatable address
- a transfer from a relocatable address to a fixed address
- a transfer from a relocatable address to another relocatable address

When a relocatable address is selected, the address is incremented, after a transfer, for the next transfer. In a 8-bit transfer, the transfer address is incremented by one. In a 16-bit transfer, the transfer address is incremented by two.
When a source or destination address exceeds address $0FFFF_{16}$ as a result of address incrementation, the source or destination address returns to address 000000_{16} and continues incrementation. Maintain source and destination address at address $0FFFF_{16}$ or below.

13.3.2 Immediate Data Transfer

Immediate data is transferred to a desired memory location. A fixed or relocatable address can be selected as the destination address. Store the immediate data into SADR. To transfer an 8-bit immediate data, write the data in the low-order byte of SADR (high-order byte is ignored).

13.3.3 Calculation Transfer

After two memory data, or an immediate data and memory data are added together, the calculated result is transferred to a desired memory location. One memory location address to be calculated or immediate data must be set in SADR and the other memory location address to be calculated in OADR. Fixed or relocatable address can be selected as source and destination addresses when using a memory + memory calculation transfer. If the transfer source address is relocatable, the operation address also becomes relocatable. Fixed or relocatable address can be selected as the transfer destination address when using an immediate data + memory calculation transfer.

13.4 Transfer Modes

In DMAC II, single and burst transfers are available. The BRST bit in MOD selects transfer method, either the single transfer or burst transfer. COUNT determines how many transfers occur. No transfer occurs when COUNT is set to "0000_{16}". All interrupts are ignored while transfer is in progress.

13.4.1 Single Transfer

For every transfer request factor, one transfer unit of 8-bit or 16-bit data is transferred once. When the source or destination address is relocatable, the address is incremented, after a transfer, for the next transfer.

COUNT is decremented every time a transfer occurs. When using the end-of-transfer interrupt, the interrupt is acknowledged when COUNT reaches "0".

13.4.2 Burst Transfer

For every transfer request factor, data is continuously transferred the number of times determined by COUNT. COUNT is decremented every time a transfer occurs. The burst transfer ends when COUNT reaches "0". The end-of-transfer interrupt is acknowledged when the burst transfer ends if using the end-of-transfer interrupt.

13.4.3 Multiple Transfer

The MULT bit in MOD selects the multiple transfer. When using the multiple transfer, select the memory-to-memory transfer. One transfer request factor initiates multiple transfers. The CNT2 to CNT0 bits in MOD selects the number of transfers from "001_2" (once) to "111_2" (7 times). Do not set the CNT2 to CNT0 bits to "000_2".

The transfer source and destination addresses for each transfer must be allocated alternately to addresses following MOD and COUNT. When the multiple transfer is selected, the calculation transfer, burst transfer, end-of-transfer interrupt and chained transfer cannot be used.

13.4.4 Chained Transfer

The CHAIN bit in MOD selects the chained transfer.

The following process initiates the chained transfer.

(1) Transfer, caused by a transfer request factor, occurs according to the content of the DMAC II index. The vectors of the request factor indicates where the DMAC II index is allocated. For each request, the BRST bit selects either single or burst transfer.

(2) When COUNT reaches "0", the contents of CADR1 to CADR0 are written to the vector of the request factor. When the INTE bit in the MOD is set to "1," the end-of-transfer interrupt is generated simultaneously.

(3) When the next DMAC II transfer request is generated, transfer occurs according to the contents of the DMAC II index indicated by the vector rewritten in (2).

Figure 13.4 shows the relocatable vector and DMACII index of when the chained transfer is in progress. When performing the chained transfer, the relocatable vector table must be located in the RAM.

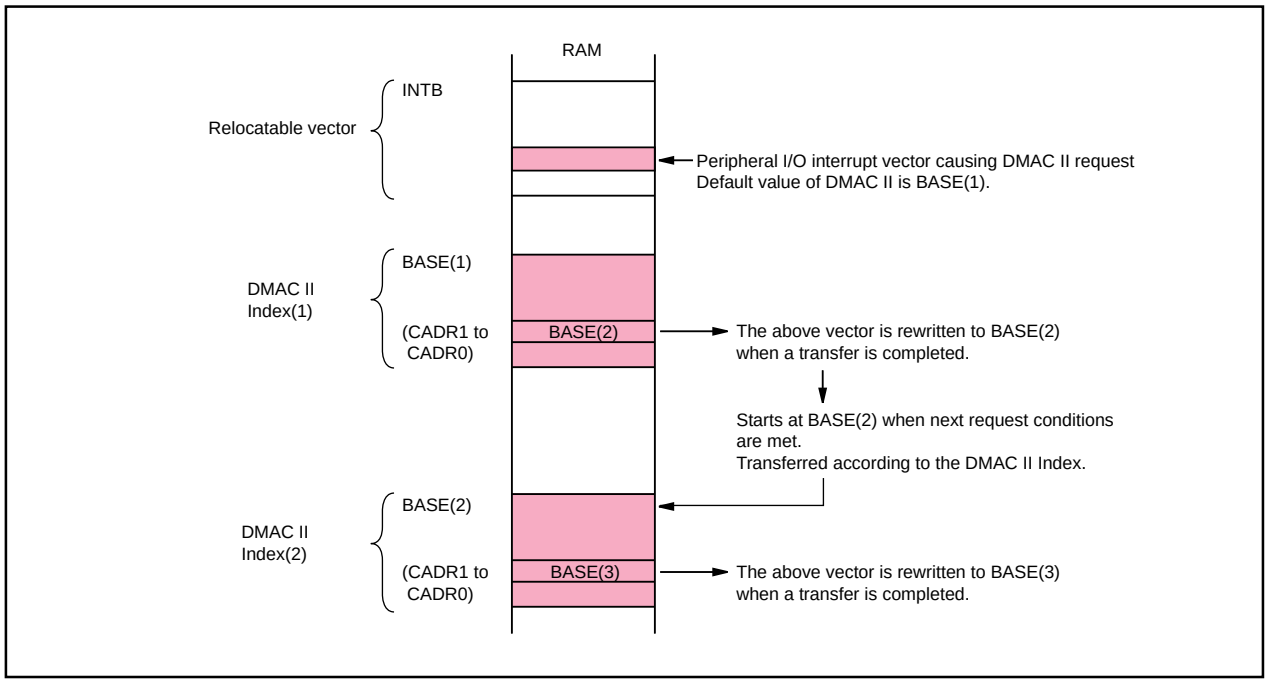


Figure 13.4 Relocatable Vector and DMAC II Index

13.4.5 End-of-Transfer Interrupt

The INTE bit in MOD selects the end-of-transfer interrupt. Set the starting address of the end-of-transfer interrupt routine in the IADR1 to IADR0 bits. The end-of-transfer interrupt is generated when COUNT reaches "0."

13.5 Execution Time

DMAC II execution cycle is calculated by the following equations:

Multiple transfer: t = 21 + (11 + b + c) x k cycles
Other than multiple transfers: t = 6 + (26 + a + b + c + d) x m + (4 + e) x n cycles

a: If IMM = 0 (source of transfer is immediate data), a = 0;
if IMM = 1 (source of transfer is memory), a = –1
b: If UPDS = 1 (source transfer address is a relocatable address), b = 0;
if UPDS = 0 (source transfer address is a fixed address), b = 1
c: If UPDD = 1 (destination transfer address is a relocatable address), c = 0;
if UPDD = 0 (destination transfer address is a fixed address), c = 1
d: If OPER = 0 (calculation function is not selected), d = 0;
if OPER = 1 (calculation function is selected) and UPDS = 0 (source of transfer is immediate data or fixed address memory), d = 7;
if OPER = 1 (calculation function is selected) and UPDS = 1 (source of transfer is relocatable address memory), d = 8
e: If CHAIN = 0 (chained transfer is not selected), e = 0; if CHAIN = 1 (chained transfer is selected), e = 4
m: BRST = 0 (single transfer), m = 1; BRST = 1 (burst transfer), m = the value set in COUNT
n: If COUNT = 1, n = 0; if COUNT = 2 or more, n = 1
k: Number of transfers set in the CNT2 to CNT0 bits

The equations above are approximations. The number of cycles may change with CPU state, bus wait state, and DMAC II index allocation.

The first instruction from the end-of-transfer interrupt routine is executed in the 8th cycle after the DMAC II transfer is completed.

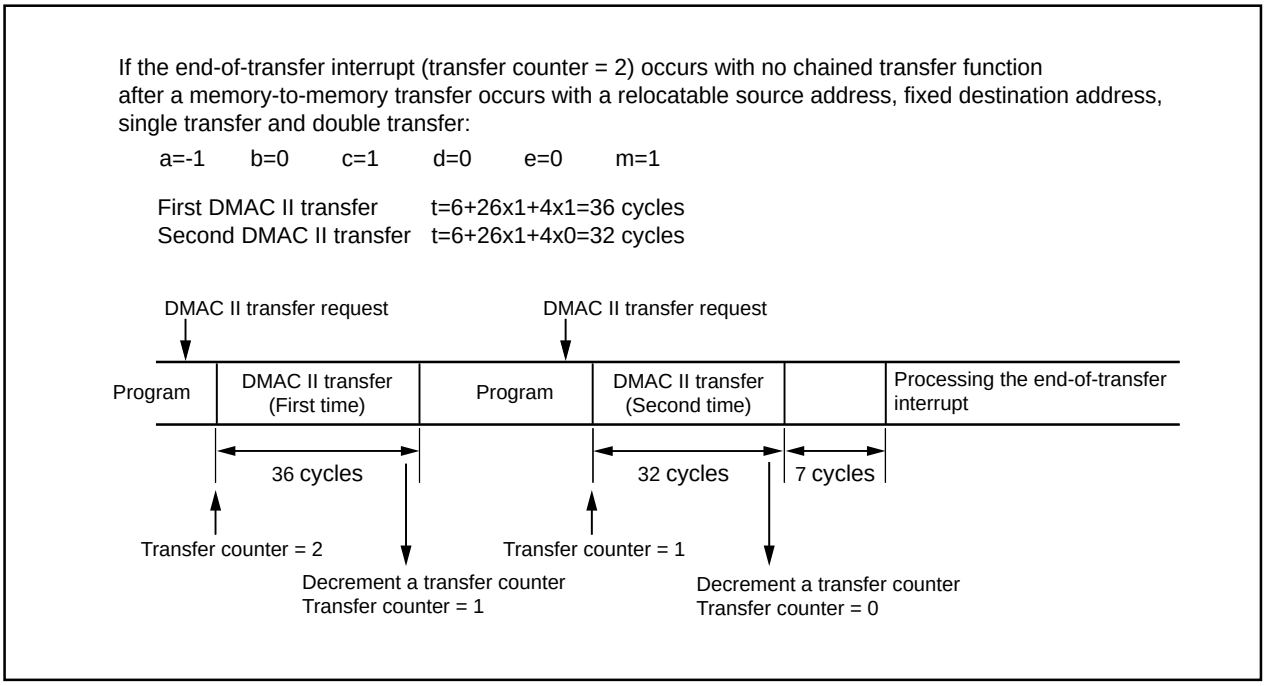
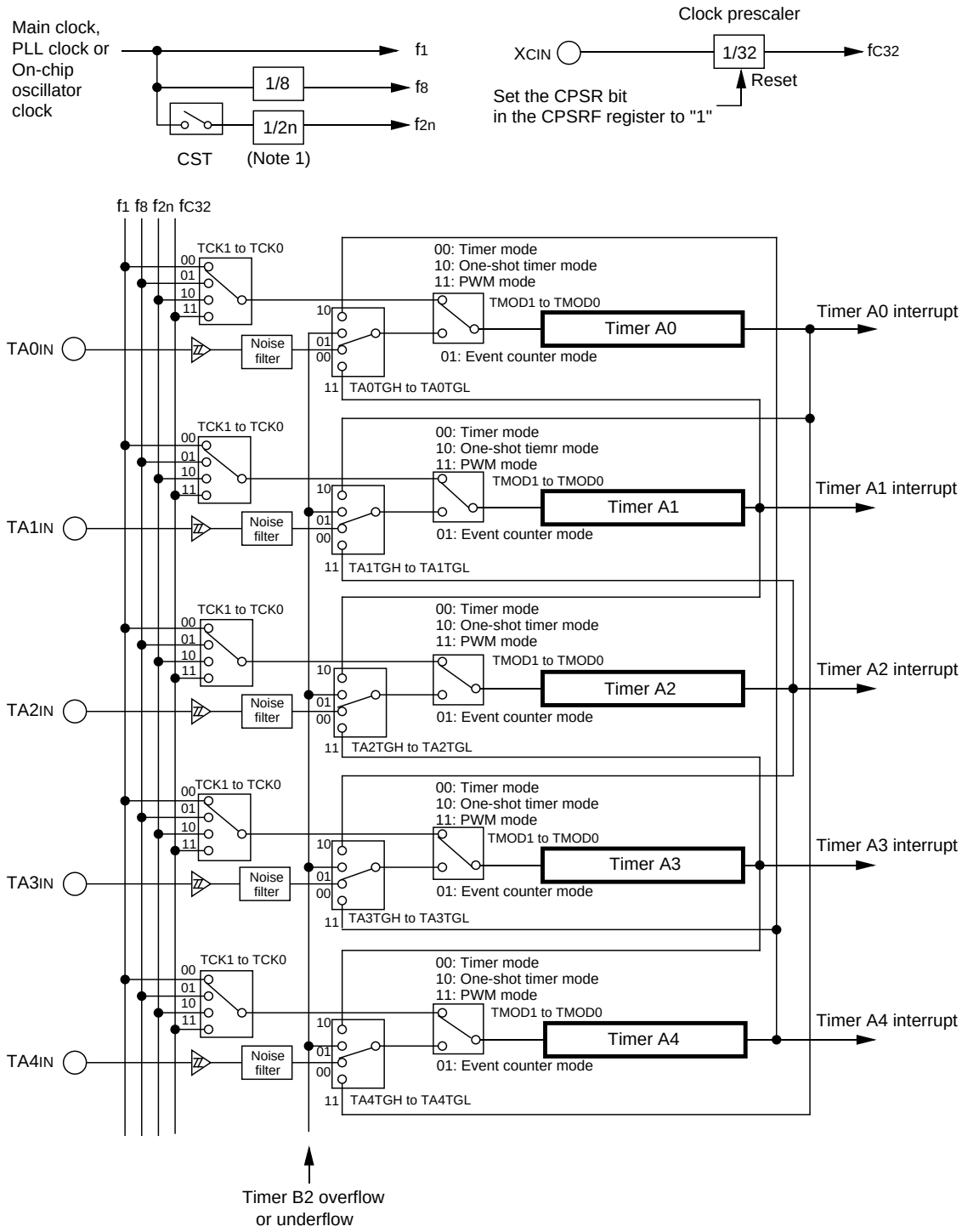


Figure 13.5 Transfer Cycle

When an interrupt request which acts as a DMAC II transfer request factor and another interrupt request with higher priority (e.g., $\overline{\text{NMI}}$ or watchdog timer) are generated simultaneously, the interrupt with higher priority takes precedence over the DMAC II transfer. The pending DMAC II transfer starts after the interrupt processing sequence has been completed.

14. Timers

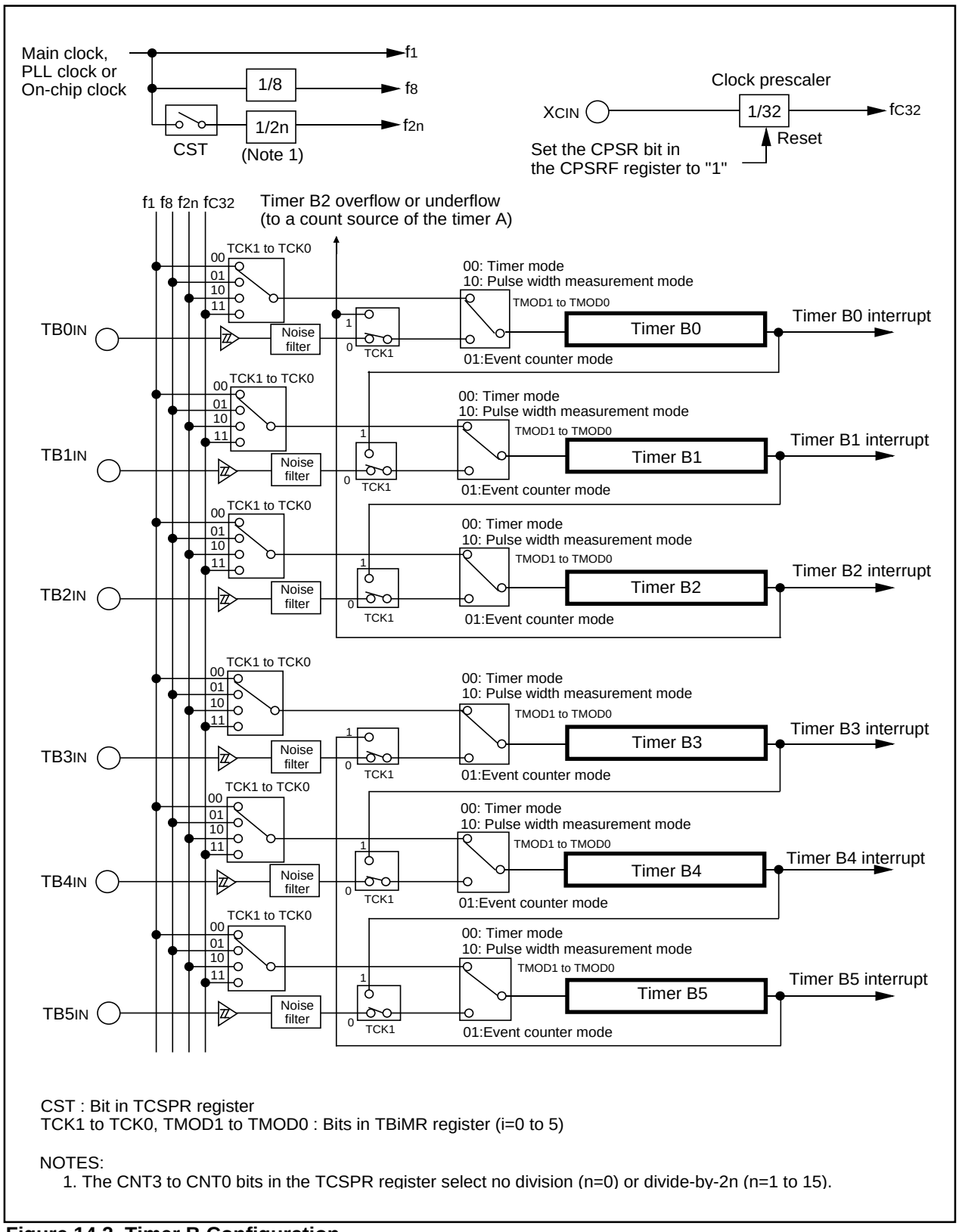
The microcomputer has eleven 16-bit timers. Five timers A and six timers B have different functions. Each timer operates independently. The count source for each timer is the clock for timer operations including counting and reloading, etc. Figures 14.1 and 14.2 show block diagrams of timer A and timer B configuration.



CST: Bit in TCSPR register
TCK1 to TCK0, TMOD1 to TMOD0 : Bits in TAiMR register
TAiGH to TAiGL: Bits in ONSF register or TRGSR register (i=1 to 4)

NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Figure 14.1 Timer A Configuration



CST : Bit in TCSPR register
TCK1 to TCK0, TMOD1 to TMOD0 : Bits in TBiMR register (i=0 to 5)

NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Figure 14.2 Timer B Configuration

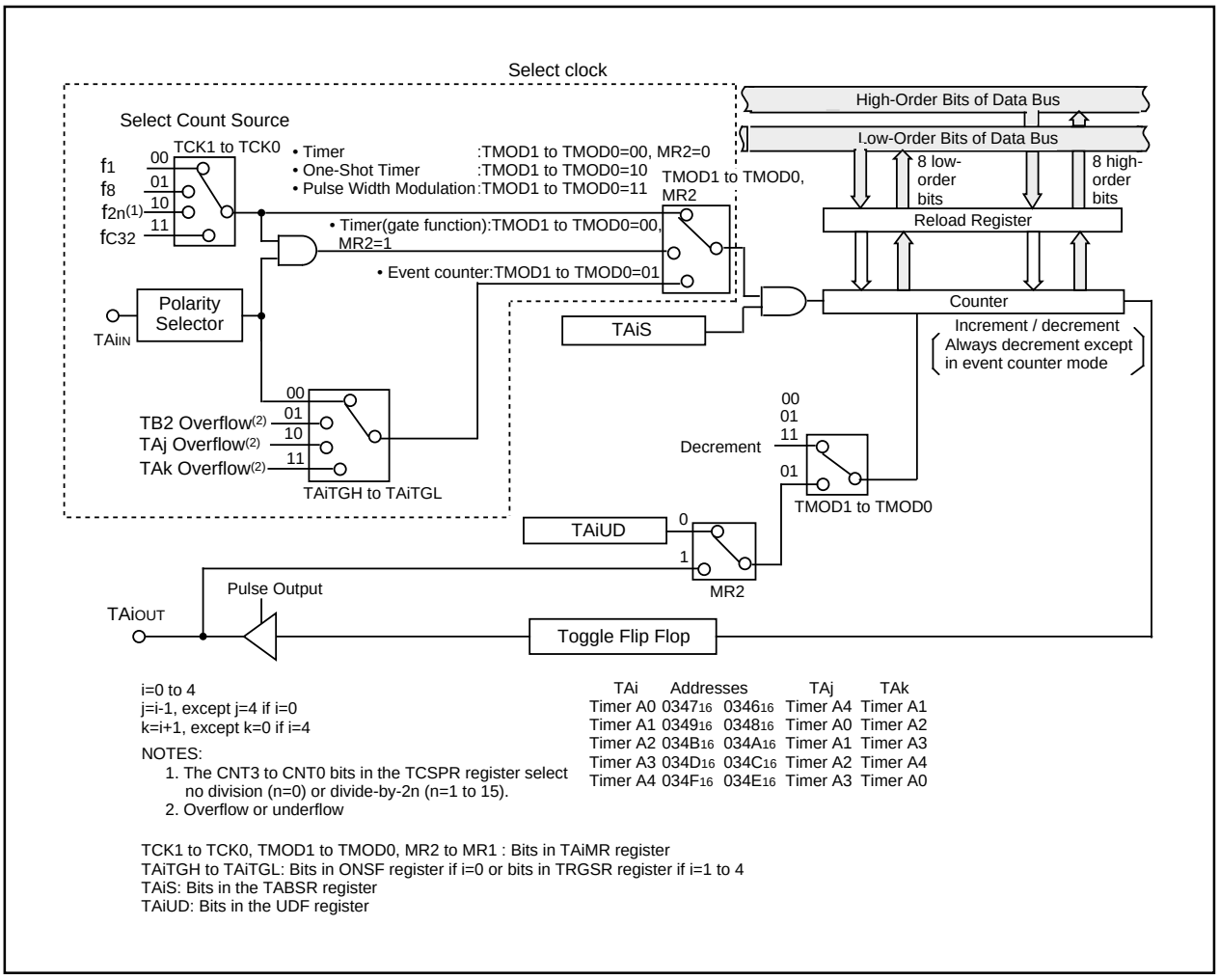
14.1 Timer A

Figure 14.3 shows a block diagram of the timer A. Figures 14.4 to 14.7 show registers associated with the timer A.

The timer A supports the following four modes. Except in event counter mode, all timers A0 to A4 have the same function. The TMOD1 to TMOD0 bits in the TAiMR register (i=0 to 4) determine which mode is used.

- Timer mode: The timer counts an internal count source.
- Event counter mode: The timer counts an external pulse or an overflow and underflow of other timers.
- One-shot timer mode: The timer outputs one valid pulse until the counter reaches "0000$_{16}$".
- Pulse width modulation mode: The timer continuously outputs desired pulse widths.

Table 14.1 lists TAiOUT pin settings when used as an output. Table 14.2 lists TAiIN and TAiOUT pin settings when used as an input.



i=0 to 4
j=i-1, except j=4 if i=0
k=i+1, except k=0 if i=4

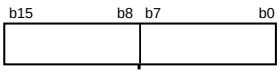
NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).
2. Overflow or underflow

TAi	Addresses		TAj	TAk
Timer A0	0347$_{16}$	0346$_{16}$	Timer A4	Timer A1
Timer A1	0349$_{16}$	0348$_{16}$	Timer A0	Timer A2
Timer A2	034B$_{16}$	034A$_{16}$	Timer A1	Timer A3
Timer A3	034D$_{16}$	034C$_{16}$	Timer A2	Timer A4
Timer A4	034F$_{16}$	034E$_{16}$	Timer A3	Timer A0

TCK1 to TCK0, TMOD1 to TMOD0, MR2 to MR1 : Bits in TAiMR register
TAiTGH to TAiTGL: Bits in ONSF register if i=0 or bits in TRGSR register if i=1 to 4
TAiS: Bits in the TABSR register
TAiUD: Bits in the UDF register

Figure 14.3 Timer A Block Diagram

Timer Ai Register (i=0 to 4)(1)



Symbol	Address	After Reset
TA0 to TA2	0347$_{16}$-0346$_{16}$, 0349$_{16}$-0348$_{16}$, 034B$_{16}$-034A$_{16}$	Indeterminate
TA3, TA4	034D$_{16}$-034C$_{16}$, 034F$_{16}$-034E$_{16}$	Indeterminate

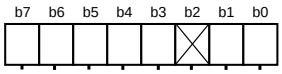
Mode	Function	Setting Range	RW
Timer Mode	If setting value is *n*, count source is divided by *n+1*.	0000$_{16}$ to FFFF$_{16}$	RW
Event Counter Mode(2)	If setting value is *n*, count source is divided by *FFFF$_{16}$ - n+1* when the counter is incremented and by *n+1* when the counter is decremented.	0000$_{16}$ to FFFF$_{16}$	RW
One-Shot Timer Mode(4)	If setting value is *n*, count source is divided by *n*, then stops.	0000$_{16}$ to FFFF$_{16}$(3)	WO
Pulse Width Modulation Mode(5) (16-Bit PWM)	If count source frequency is *fj* and setting value of the TAi register is *n*, PWM cycle: *(2^{16}-1) / fj* "H" width of PWM pulse: *n / fj*	0000$_{16}$ to FFFE$_{16}$(3)	WO
Pulse Width Modulation Mode(5) (8-Bit PWM)	If count source frequency is *fj*, setting value of high-order bits in the TAi register is *n* and setting value of low-order bits in the TAi register is *m*, PWM cycle: *(2^{8}-1)x(m+1) / fj* "H" width of PWM pulse: *(m+1)n / fj*	00$_{16}$ to FE$_{16}$(3) (High-order address bits) 00$_{16}$ to FF$_{16}$(3) (Low-order address bits)	WO

fj : f_1, f_8, f_{2n}, f_{C32}

NOTES:
1. Use 16-bit data for reading and writing.
2. The TAi register counts how many pulses are input externally or how many times another timer overflows and underflows.
3. Use the MOV instruction to set the TAi register.
4. When the TAi register is set to "0000$_{16}$", the counter does not start and the timer Ai interrupt request is not generated.
5. When the TAi register is set to "0000$_{16}$", the pulse width modulator does not operate and the TAi$_{OUT}$ pin is held "L". The TAi interrupt request is also not generated. The same situation occurs in 8-bit pulse width modulator mode if the 8 high-order bits in the TAi register are set to "00$_{16}$".

Figure 14.4 TA0 to TA4 Registers

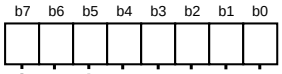
Timer Ai Mode Register (i=0 to 4)



Symbol	Address	After Reset
TA0MR0 to TA4MR	0356_{16}, 0357_{16}, 0358_{16}, 0359_{16}, $035A_{16}$	0000 0X00$_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation Mode Select Bit	b1b0 0 0 : Timer mode 0 1 : Event counter mode 1 0 : One-shot timer mode 1 1 : Pulse width modulation (PWM) mode	RW
TMOD1			RW
$\overline{\text{(b2)}}$	Nothing is assigned. When write, set to "0".		—
MR1	————	Function varies depending on operation mode	RW
MR2			RW
MR3			RW
TCK0	Count Source Select Bit	Function varies depending on operation mode	RW
TCK1			RW

Count Start Flag



Symbol	Address	After Reset
TABSR	0340_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA1S	Timer A1 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA2S	Timer A2 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA3S	Timer A3 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA4S	Timer A4 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB0S	Timer B0 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB1S	Timer B1 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB2S	Timer B2 Count Start Flag	0 : Stops counting 1 : Starts counting	RW

Figure 14.5 TA0MR to TA4MR Registers and TABSR Register

Up/Down Flag(1)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
UDF	0344₁₆	00₁₆

Bit Symbol	Bit Name	Function	RW
TA0UD	Timer A0 Up/Down Flag	0 : Decrement 1 : Increment (Note 2)	RW
TA1UD	Timer A1 Up/Down Flag	0 : Decrement 1 : Increment (Note 2)	RW
TA2UD	Timer A2 Up/Down Flag	0 : Decrement 1 : Increment (Note 2)	RW
TA3UD	Timer A3 Up/Down Flag	0 : Decrement 1 : Increment (Note 2)	RW
TA4UD	Timer A4 Up/Down Flag	0 : Decrement 1 : Increment (Note 2)	RW
TA2P	Timer A2 Two-Phase Pulse Signal Processing Function Select Bit	0 : Disables two-phase pulse signal processing function 1 : Enables two-phase pulse signal processing function (Note 3)	WO
TA3P	Timer A3 Two-Phase Pulse Signal Processing Function Select Bit	0 : Disables two-phase pulse signal processing function 1 : Enables two-phase pulse signal processing function (Note 3)	WO
TA4P	Timer A4 Two-Phase Pulse Signal Processing Function Select Bit	0 : Disables two-phase pulse signal processing function 1 : Enables two-phase pulse signal processing function (Note 3)	WO

NOTES:
1. Use the MOV instruction to set the UDF register.
2. This bit is enabled when the MR2 bit in the TAiMR register (i=0 to 4) is set to "0" (the UDF register causes increment/decrement switching) in event counter mode.
3. Set this bit to "0" when not using the two-phase pulse signal processing function.

One-Shot Start Flag

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
ONSF	0342₁₆	00₁₆

Bit Symbol	Bit Name	Function	RW
TA0OS	Timer A0 One-Shot Start Flag	0 : In an idle state 1 : Starts the timer (Note 1)	RW
TA1OS	Timer A1 One-Shot Start Flag	0 : In an idle state 1 : Starts the timer (Note 1)	RW
TA2OS	Timer A2 One-Shot Start Flag	0 : In an idle state 1 : Starts the timer (Note 1)	RW
TA3OS	Timer A3 One-Shot Start Flag	0 : In an idle state 1 : Starts the timer (Note 1)	RW
TA4OS	Timer A4 One-Shot Start Flag	0 : In an idle state 1 : Starts the timer (Note 1)	RW
TAZIE	Z-Phase Input Enable Bit	0 : Disables Z-phase input 1 : Enables Z-phase input	RW
TA0TGL	Timer A0 Event/Trigger Select Bit	b7 b6 0 0 : Selects an input to the TA0IN pin 0 1 : Selects the TB2 overflows(2) 1 0 : Selects the TA4 overflows(2) 1 1 : Selects the TA1 overflows(2)	RW
TA0TGH			RW

NOTES:
1. When read, the bit is set to "0".
2. Overflow or underflow.

Figure 14.6 UDF Register and ONSF Register

Trigger Select Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRGSR	034316	0016

Bit Symbol	Bit Name	Function	RW
TA1TGL	Timer A1 Event/Trigger Select Bit	b0 b1 0 0 : Selects an input to the TA1IN pin 0 1 : Selects the TB2 overflows(1) 1 0 : Selects the TA0 overflows(1) 1 1 : Selects the TA2 overflows(1)	RW
TA1TGH			RW
TA2TGL	Timer A2 Event/Trigger Select Bit	b3 b2 0 0 : Selects an input to the TA2IN pin 0 1 : Selects the TB2 overflows(1) 1 0 : Selects the TA1 overflows(1) 1 1 : Selects the TA3 overflows(1)	RW
TA2TGH			RW
TA3TGL	Timer A3 Event/Trigger Select Bit	b5 b4 0 0 : Selects an input to the TA3IN pin 0 1 : Selects the TB2 overflows(1) 1 0 : Selects the TA2 overflows(1) 1 1 : Selects the TA4 overflows(1)	RW
TA3TGH			RW
TA4TGL	Timer A4 Event/Trigger Select Bit	b7 b6 0 0 : Selects an input to the TA4IN pin 0 1 : Selects the TB2 overflows(1) 1 0 : Selects the TA3 overflows(1) 1 1 : Selects the TA0 overflows(1)	RW
TA4TGH			RW

NOTES:
1. Overflow or underflow.

Count Source Prescaler Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TCSPR	$035F16$	$0XXX\ 0000_2$

Bit Symbol	Bit Name	Function	RW
CNT0	Divide Ratio Select Bit	If setting value is *n*, f_{2n} is the main clock, PLL clock or on-chip oscillator clock divided by *2n*. Not divided if *n=0*. (Note 1)	RW
CNT1			RW
CNT2			RW
CNT3			RW
____ (b6 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		–
CST	Operation Enable Bit	0 : Stops divider 1 : Starts divider	RW

NOTES:
1. Set the CST bit to "0" before the CNT3 to CNT0 bits are rewritten.

Figure 14.7 TRGSR Register and TCSPR Register

Table 14.1 Pin Settings for Output from TAiOUT Pin (i=0 to 4)

Pin	Setting		
	PS1, PS2 Registers	PSL1, PSL2 Registers	PSC Register
P70/TA0OUT(1)	PS1_0= 1	PSL1_0=1	PSC_0= 0
P72/TA1OUT	PS1_2= 1	PSL1_2=1	PSC_2= 0
P74/TA2OUT	PS1_4= 1	PSL1_4=0	PSC_4= 0
P76/TA3OUT	PS1_6= 1	PSL1_6=1	PSC_6= 0
P80/TA4OUT	PS2_0= 1	PSL2_0=0	–

NOTES:

1. P70/TA0OUT is a port for the N-channel open drain output.

Table 14.2 Pin Settings for Input to TAiIN and TAiOUT Pins (i=0 to 4)

Pin	Setting	
	PS1, PS2 Registers	PD7, PD8 Registers
P70/TA0OUT	PS1_0=0	PD7_0=0
P71/TA0IN	PS1_1=0	PD7_1=0
P72/TA1OUT	PS1_2=0	PD7_2=0
P73/TA1IN	PS1_3=0	PD7_3=0
P74TA2OUT	PS1_4=0	PD7_4=0
P75/TA2IN	PS1_5=0	PD7_5=0
P76TA3OUT	PS1_6=0	PD7_6=0
P77/TA3IN	PS1_7=0	PD7_7=0
P80/TA4OUT	PS2_0=0	PD8_0=0
P81/TA4IN	PS2_1=0	PD8_1=0

14.1.1 Timer Mode

In timer mode, the timer counts an internally generated count source (see Table 14.3). Figure 14.8 shows the TAiMR register (i=0 to 4) in timer mode.

Table 14.3 Specifications in Timer Mode

Item	Specification
Count Source	f_1, f_8, f_{2n}(1), f_{C32}
Count Operation	• The timer decrements the counter When the timer underflows, the content of the reload register is reloaded into the count register and counting resumes.
Divide Ratio	1/(n+1) n: setting value of the TAi register (i=0 to 4) 0000_{16} to $FFFF_{16}$
Count Start Condition	The TAiS bit in the TABSR register is set to "1" (starts counting)
Count Stop Condition	The TAiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer underflows
TAiIN Pin Function	Programmable I/O port or gate input
TAiOUT Pin Function	Programmable I/O port or pulse output
Read from Timer	The TAi register indicates value of the counter
Write to Timer	• When the counter stops or before the first count source after counter start, the value written to the TAi register is also written to both reload register and counter • While counting, the value written to the TAi register is written to the reload register (It is transferred to the counter at the next reload timing)
Selectable Function	• Gate function Input signal to the TAiIN pin determines whether the timer starts or stops counting • Pulse output function The polarity of the TAiOUT pin is inversed whenever the timer underflows

NOTES:

1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Timer Ai Mode Register (i=0 to 4) (Timer Mode)

b7	b6	b5	b4	b3	b2	b1	b0
					X	0	0

Symbol	Address	After Reset
TA0MR to TA4MR	0356_{16}, 0357_{16}, 0358_{16}, 0359_{16}, $035A_{16}$	0000 0X00$_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation Mode Select Bit	b1 b0 0 0 : Timer mode	RW
TMOD1			RW
——— (b2)	Nothing is assigned. When write, set to "0".		—
MR1	Gate Function Select Bit	b4 b3 0 X : Gate function disabled(1) (TAiIN pin is a programmable I/O pin) 1 0 : Timer counts only while the TAiIN pin is held "L" 1 1 : Timer counts only while the TAiIN pin is held "H"	RW
MR2			RW
MR3	Set to "0" in timer mode		RW
TCK0	Count Source Select Bit	b7 b6 0 0 : f_1 0 1 : f_8 1 0 : f_{2n}(2) 1 1 : f_{C32}	RW
TCK1			RW

NOTES:
1. X can be set to either "0" or "1".
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Figure 14.8 TA0MR to TA4MR Registers

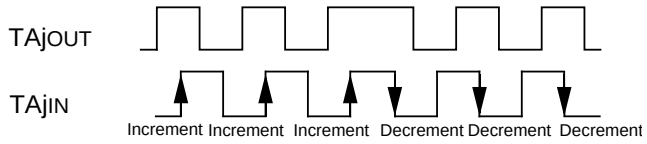
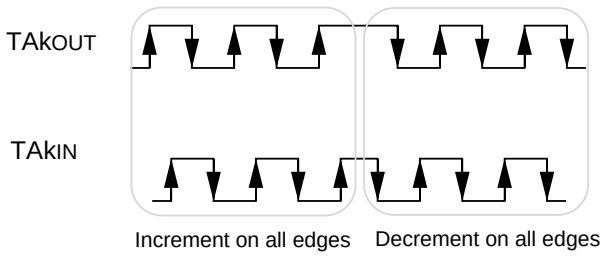
14.1.2 Event Counter Mode

In event counter mode, the timer counts how many external signals are applied or how many times another timer overflows and underflows. The timers A2, A3 and A4 can count externally generated two-phase signals. Table 14.4 lists specifications in event counter mode (when not handling a two-phase pulse signal). Table 14.5 lists specifications in event counter mode (when handling a two-phase pulse signal with the timer A2, A3 and A4). Figure 14.9 shows the TAiMR (i=0 to 4) register in event counter mode.

Table 14.4 Specifications in Event Counter Mode (when not processing two-phase pulse signal)

Item	Specification
Count Source	• External signal applied to the TAiIN pin (i = 0 to 4) (valid edge can be selected by program) • The timer B2 overflows or underflows, timer Aj overflows or underflows (j=i-1, except j=4 if i=0) and timer Ak overflows or underflows (k=i+1, except k=0 if i=4)
Count Operation	• External signal and program can determine whether the timer increments or decrements the counter • When the timer underflows or overflows, the content of the reload register is reloaded into the count register and counting resumes. When the free-running count function is selected, the timer continues counting without reloading.
Divide Ratio	• 1/($FFFF_{16}$ - n + 1) for counter increment • 1/(n + 1) for counter decrement n : setting value of the TAi register 0000_{16} to $FFFF_{16}$
Count Start Condition	The TAiS bit in the TABSR register is set to "1" (starts counting)
Count Stop Condition	The TAiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer overflows or underflows
TAiIN Pin Function	Programmable I/O port or count source input
TAiOUT Pin Function	Programmable I/O port, pulse output or input selecting a counter increment or decrement
Read from Timer	The TAi register indicates counter value
Write to Timer	• When the counter stops or before the first count source after counter start, the value written to the TAi register is also written to both reload register and counter • While counting, the value written to the TAi register is written to the reload register (It is transferred to the counter at the next reload timing)
Selectable Function	• Free-running count function Content of the reload register is not reloaded even if the timer overflows or underflows • Pulse output function The polarity of the TAiOUT pin is inversed whenever the timer overflows or underflows

Table 14.5 Specifications in Event Counter Mode (when processing two-phase pulse signal on timer A2, A3 and A4)

Item	Specification
Count Source	Two-phase pulse signal applied to the TAiIN pin, or TAiIN and TAiOUT pin (i = 2 to 4)
Count Operation	• Two-phase pulse signal determines whether the timer increments or decrements the counter • When the timer overflows or underflows, the content of the reload register is reloaded into the count register and counting resumes. With the free-running count function, the timer continues counting without reloading.
Divide Ratio	• 1/ (FFFF16 - n + 1) for counter increment • 1/ (n + 1) for counter decrement n : setting value of the TAi register 000016 to FFFF16
Count Start Condition	The TAiS bit in the TABSR register is set to "1" (starts counting)
Count Stop Condition	The TAiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer overflows or underflows
TAiIN Pin Function	Two-phase pulse signal is applied
TAiOUT Pin Function	Two-phase pulse signal is applied
Read from Timer	The TAi register indicates counter value
Write to Timer	• When the counter stops or before the first count source after counter start, the value written to the TAi register is also written to both reload register and counter • While counting, the value written to the TAi register is written to the reload register (It is transferred to the counter at the next reload timing)
Selectable Function(1)	• Normal processing operation (the timer A2 and timer A3) While a high-level signal ("H") is applied to the TAjOUT pin (j = 2 or 3), the timer increments the counter on the rising edge of the TAjIN pin or decrements the counter on the falling edge.  • Multiply-by-4 processing operation (the timer A3 and timer A4) While a high-level signal ("H") is applied to the TAkOUT pin (k = 3 or 4) with the rising edge of the TAkIN pin, the timer increments the counter on the rising and falling edges of the TAkOUT and TAkIN pins. While "H" is applied to the TAkOUT pin with the falling edge of the TAkIN pin, the timer decrements the counter on the rising and falling edges of the TAkOUT and TAkIN pins. 

NOTES:

1. Only timer A3 operation can be selected. The timer A2 is for the normal processing operation. The timer A4 is for the multiply-by-4 operation.

Timer Ai Mode Register (i=0 to 4) (Event Counter Mode)

b7	b6	b5	b4	b3	b2	b1	b0
		0			X	0	1

Symbol	Address	After Reset
TA0MR to TA4MR	0356_{16}, 0357_{16}, 0358_{16}, 0359_{16}, $035A_{16}$	0000 0X00$_{16}$

Bit Symbol	Bit Name	Function (When not using two-phase pulse signal processing)	Function (When using two-phase pulse signal processing)	RW
TMOD0	Operation Mode Select Bit	b1 b0 0 1 : Event counter mode(1)		RW
TMOD1				RW
——— (b2)	Nothing is assigned. When write, set to "0".			RW
MR1	Count Polarity Select Bit(2)	0 : Counts falling edges of an external signal 1 : Counts rising edges of an external signal	Set to "0"	RW
MR2	Increment/Decrement Switching Cause Select Bit	0 : Setting of the UDF register 1 : Input signal to TAiOUT pin(3)	Set to "1"	RW
MR3	Set to "0" in event counter mode			RW
TCK0	Count Operation Type Select Bit	0 : Reloading 1 : Free running		RW
TCK1	Two-Phase Pulse Signal Processing Operation Select Bit(4,5)	Set to "0"	0 : Normal processing operation 1 : Multiplied-by-4 processing operation	RW

NOTES:
1. The TAiTGH to TAiTGL bits in the ONSF or TRGSR register determine the count source in the event counter mode.
2. The MR1 bit is enabled only when counting how many times external signals are applied.
3. The timer decrements the counter when "L" is applied to the TAiOUT pin and the timer increments the counter when "H" is applied to the TAiOUT pin.
4. The TCK1 bit is enabled only in the TA3MR register.
5. For two-phase pulse signal processing, set the TAjP bit in the UDF register (j=2 to 4) to "1" (two-phase pulse signal processing function enabled) and the TAiTGH and TAiTGL bits to "00$_2$" (input to the TAjIN pin).

Figure 14.9 TA0MR to TA4MR Registers

14.1.2.1 Counter Reset by Two-Phase Pulse Signal Processing

The timer counter is reset to "0" by a Z-phase input when processing a two-phase pulse signal.

This function can be used in timer A3 event counter mode, two-phase pulse signal processing, free-run type or multiply-by-4 processing. The Z-phase signal is applied to the $\overline{INT2}$ pin.

When the TAZIE bit in the ONSF register is set to "1" (Z-phase input enabled), the counter can be reset by a Z-phase input. To reset the counter by a Z-phase input, set the TA3 register to "0000$_{16}$" beforehand.

Z-phase input is enabled when the edge of the signal applied to the $\overline{INT2}$ pin is detected. The POL bit in the INT2IC register can determine edge polarity. The Z-phase must have a pulse width of one timer A3 count source cycle or more. Figure 14.10 shows two-phase pulses (A-phase and B-phase) and the Z-phase.

Z-phase input resets the counter in the next count source following Z-phase input. Figure 14.11 shows the counter reset timing.

The timer A3 interrupt request is generated twice when a timer A3 overflow or an underflow, and a counter reset by $\overline{INT2}$ input occur at the same time. Do not use the timer A3 interrupt request when this function is used.

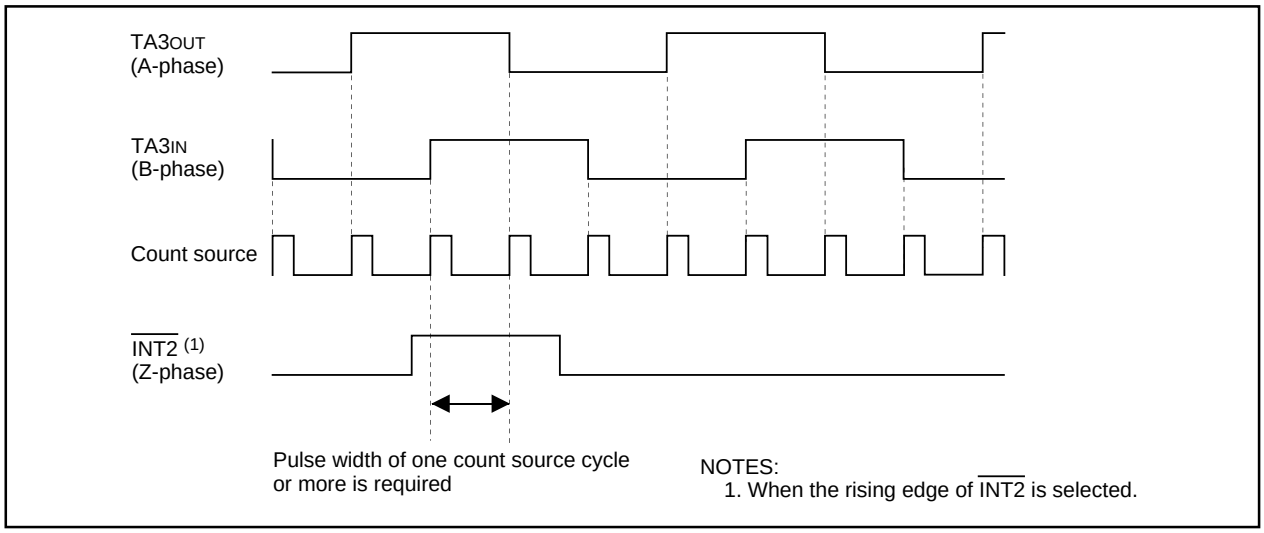


Figure 14.10 Two-phase Pulse (A-phase and B-phase) and Z-phase

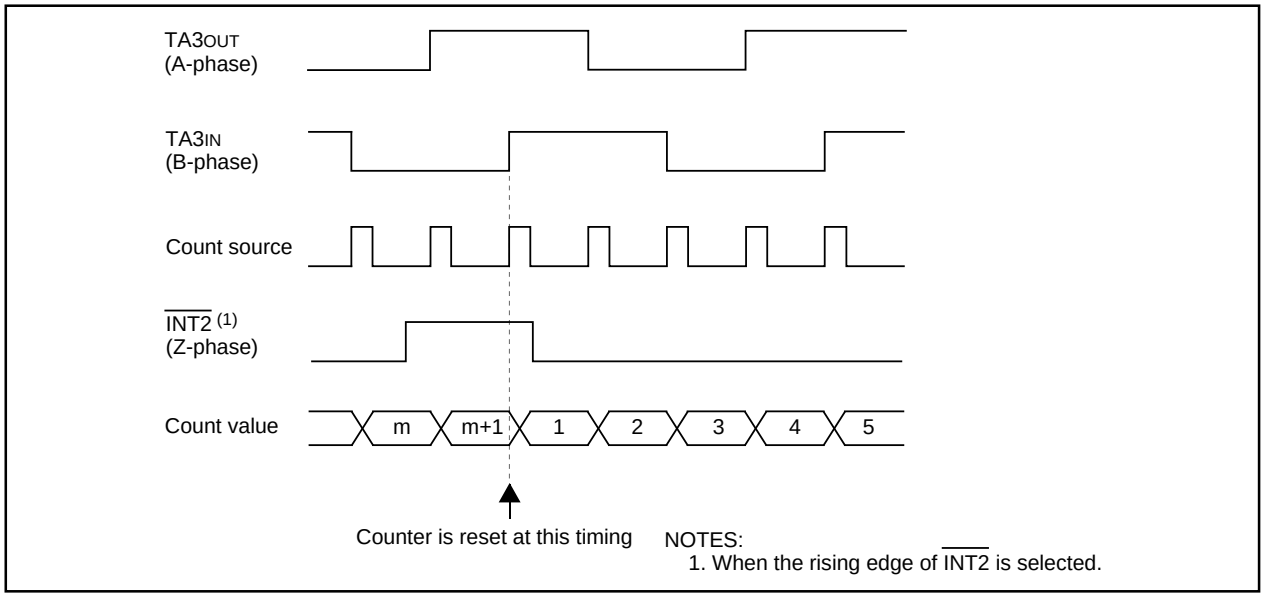


Figure 14.11 Counter Reset Timing

14.1.3 One-shot Timer Mode

In one-shot timer mode, the timer operates only once for each trigger (see **Table 14.6**). Once a trigger occurs, the timer starts and continues operating for a desired period. Figure 14.12 shows the TAiMR register (i=0 to 4) in one-shot timer mode.

Table 14.6 Specifications in One-shot Timer Mode

Item	Specification
Count Source	f_1, f_8, f_{2n}(1), f_{C32}
Count Operation	The timer decrements the counter • When the counter reaches "0000_{16}", the timer stops counting after reloading. • If a trigger occurs while counting, content of the reload register is reloaded into the count register and counting resumes.
Divide Ratio	1/n n : setting value of the TAi register (i=0 to 4) 0000_{16} to $FFFF_{16}$, but the counter does not run if n=0000_{16}
Count Start Condition	The TAiS bit in the TABSR register is set to "1" (starts counting) and following triggers occur: • External trigger is input • The timer overflows and underflows • The TAiOS bit in the ONSF register is set to "1" (timer starts)
Count Stop Condition	• After the counter has reached "0000_{16}" and is reloaded • When the TAiS bit is set to "0" (timer stops)
Interrupt Request Generation Timing	The counter reaches "0000_{16}"
TAiIN Pin Function	Programmable I/O port or trigger input
TAiOUT Pin Function	Programmable I/O port or pulse output
Read from Timer	The value in the TAi register is indeterminate when read
Write to Timer	• When the counter stops or before the first count source after counter star, the value written to the TAi register is also written to both reload register and counter • While counting, the value written to the TAi register is written to the reload register (It is transferred to the counter at the next reload timing)

NOTES:

1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Timer Ai Mode Register (i=0 to 4) (One-Shot Timer Mode)

b7	b6	b5	b4	b3	b2	b1	b0
		0			X	1	0

Symbol	Address	After Reset
TA0MR to TA4MR	0356_{16}, 0357_{16}, 0358_{16}, 0359_{16}, $035A_{16}$	$0000\ 0X00_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation Mode Select Bit	b1b0 1 0 : One-shot timer mode	RW
TMOD1			RW
____ (b2)	Nothing is assigned. When write, set to "0".		—
MR1	External Trigger Select Bit(1)	0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin	RW
MR2	Trigger Select Bit	0 : The TAiOS bit is enabled 1 : Selected by the TAiTGH and TAiTGL bits	RW
MR3	Set to "0" in the one-shot timer mode		RW
TCK0	Count Source Select Bit	b7b6 0 0 : f_1 0 1 : f_8 1 0 : f_{2n}(2) 1 1 : f_{C32}	RW
TCK1			RW

NOTES:
1. The MR1 bit setting is enabled only when the TAiTGH to TAiTGL bits in the TRGSR register are set to "00_2" (input to the TAiIN pin). The MR1 bit can be set to either "0" or "1" when the TAiTGH and TAiTGL bits are set to "01_2" (TB2 overflow and underflow), "10_2" (TAi overflow and underflow) or "11_2" (TAi overflow and underflow).
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Figure 14.12 TA0MR to TA4MR Registers

14.1.4 Pulse Width Modulation Mode

In pulse width modulation mode, the timer outputs pulse of desired width continuously (see **Table 14.7**). The counter functions as either 16-bit pulse width modulator or 8-bit pulse width modulator. Figure 14.13 shows the TAiMR register (i=0 to 4) in pulse width modulation mode. Figures 14.14 and 14.15 show examples of how a 16-bit pulse width modulator operates and of how an 8-bit pulse width modulator operates.

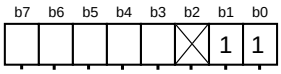
Table 14.7 Specifications in Pulse Width Modulation Mode

Item	Specification
Count Source	f_1, f_8, f_{2n}(1), f_{C32}
Count Operation	The timer decrements the counter (The counter functions as an 8-bit or a 16-bit pulse width modulator) • The timer reloads on the rising edge of PWM pulse and continues counting. • The timer is not affected by the trigger that is generated during counting.
16-Bit PWM	• "H" width = n / f_j n : setting value of the TAi register 0000_{16} to $FFFE_{16}$ f_j : Count source frequency • Cycle = (2^{16}-1) / f_j fixed
8-Bit PWM	• "H" width = n x (m+1) / f_j n : setting value of high-order bit address of the TAi register 00_{16} to FE_{16} • Cycles = (2^8-1) x (m+1) / f_j m : setting value of low-order bit address of the TAi register 00_{16} to FF_{16}
Count Start Condition	• External trigger is input • The timer overflows and underflows • The TAiS bit in the TABSR register is set to "1" (start counting)
Count Stop Condition	The TAiS bit is set to "0" (stop counting)
Interrupt Request Generation Timing	On the falling edge of the PWM pulse
TAiIN Pin Function	Programmable I/O port or trigger input
TAiOUT Pin Function	Pulse output
Read from Timer	The value in the TAi register is indeterminate when read
Write to Timer	• When the counter stops or before the first count source after counter start, the value written to the TAi register is also written to both reload register and counter • While counting, the value written to the TAi register is written to the reload register (It is transferred to the counter at the next reload timing)

NOTES:

1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Timer Ai Mode Register (i=0 to 4) (Pulse Width Modulator Mode)



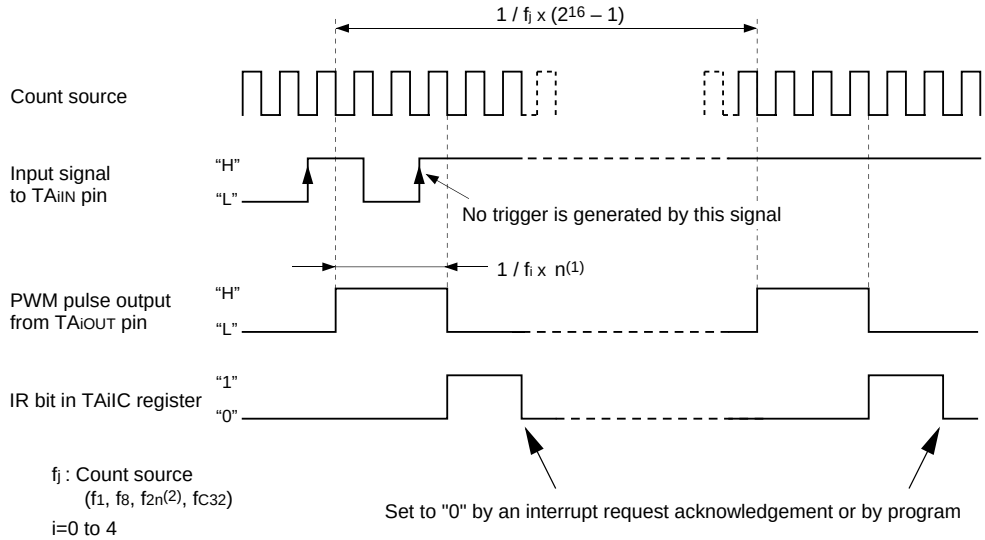
Symbol	Address	After Reset
TA0MR to TA4MR	0356_{16}, 0357_{16}, 0358_{16}, 0359_{16}, $035A_{16}$	$0000\ 0X00_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation Mode Select Bit	b1b0 1 1 : Pulse width modulation (PWM) mode	RW
TMOD1			RW
____ (b2)	Nothing is assigned. When write, set to "0".		—
MR1	External Trigger Select Bit(1)	0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin	RW
MR2	Trigger Select Bit —	0 : The TAiS bit is enabled 1 : Selected by the TAiTGH and TAiTGL bits	RW
MR3	16/8-Bit PWM Mode Select Bit	0: Functions as a 16-bit pulse width modulator 1: Functions as an 8-bit pulse width modulator	RW
TCK0	Count Source Select Bit	b7 b6 0 0 : f_1 0 1 : f_8 1 0 : f_{2n}(2) 1 1 : f_{C32}	RW
TCK1			RW

NOTES:
1. The MR1 bit setting is enabled only when the TAiTGH to TAiTGL bits in the TRGSR register are set to "00_2" (input to the TAiIN pin). The MR1 bit can be set to either "0" or "1" when the TAiTGH and TAiTGL bits are set to "01_2" (TB2 overflow and underflow), "10_2" (TAi overflow and underflow) or "11_2" (TAi overflow and underflow).
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Figure 14.13 TA0MR to TA4MR Registers

When the reload register is set to "0003$_{16}$" and an external trigger (rising edge of input signal to the TAiIN pin) is selected



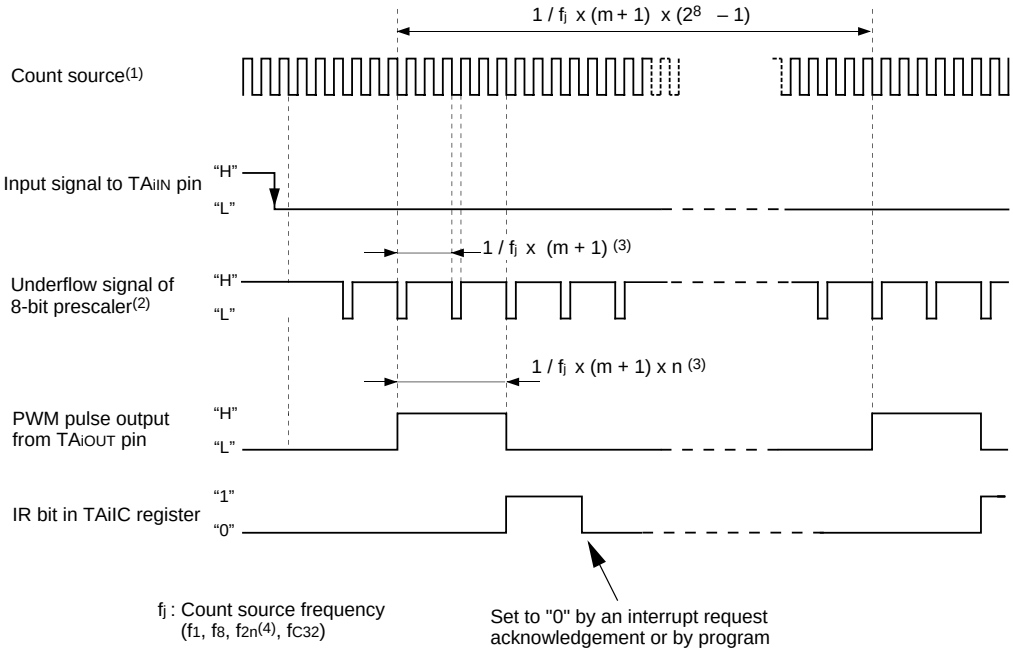
fj : Count source
(f1, f8, f2n(2), fC32)

i=0 to 4

NOTES:
1. n = 0000$_{16}$ to FFFE$_{16}$.
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Figure 14.14 16-bit Pulse Width Modulator Operation

When 8 high-order bits of the reload register are set to "02$_{16}$", 8 low-order bits of the reload register are set to "02$_{16}$" and an external trigger (falling edge of input signal to the TAiIN pin) is selected



fj : Count source frequency
(f1, f8, f2n(4), fC32)

i=0 to 4

NOTES:
1. 8-bit prescaler counts a count source.
2. 8-bit pulse width modulator counts underflow signals of the 8-bit prescaler.
3. m = 00$_{16}$ to FF$_{16}$, n = 00$_{16}$ to FE$_{16}$
4. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

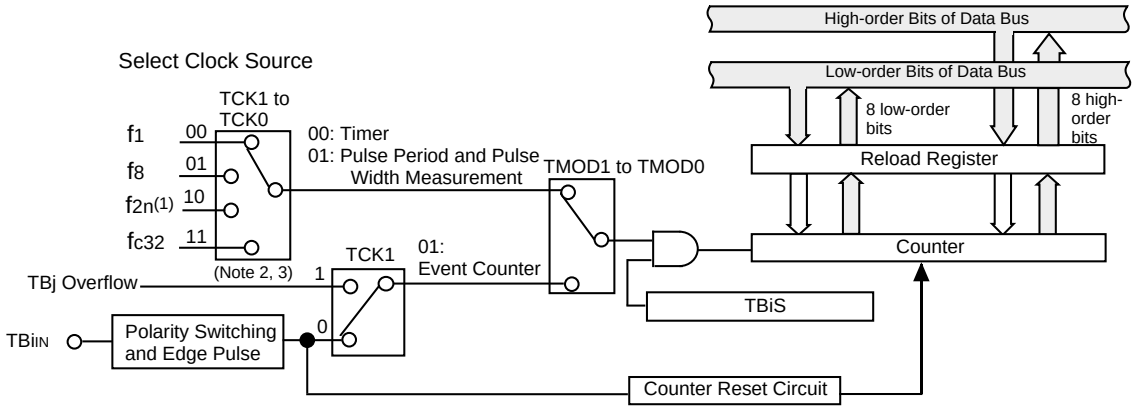
Figure 14.15 8-bit Pulse Width Modulator Operation

14.2 Timer B

Figure 14.16 shows a block diagram of the timer B. Figures 14.17 to 14.19 show registers associated with the timer B. The timer B supports the following three modes. The TMOD1 to TMOD0 bits in the TBiMR register (i=0 to 5) determine which mode is used.

- Timer mode : The timer counts an internal count source.
- Event counter mode : The timer counts pulses from an external source or overflow and underflow of another timer.
- Pulse period/pulse width measurement mode : The timer measures pulse period or pulse width of an external signal.

Table 14.18 lists TBiIN pin settings.



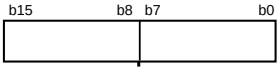
i=0 to 5
NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).
2. Overflows or underflows.
3. j=i-1, except j=2 when i=0 j=5 when i=3

TCK1 to TCK0, TMOD1 to TMOD0 : Bits in TAiMR register
TBiS : Bits in the TABSR and the TBSR register

TBi	Address		TBj
Timer B0	035116	035016	Timer B2
Timer B1	035316	035216	Timer B0
Timer B2	035516	035416	Timer B1
Timer B3	031116	031016	Timer B5
Timer B4	031316	031216	Timer B3
Timer B5	031516	031416	Timer B4

Figure 14.16 Timer B Block Diagram

Timer Bi Register(1) (i=0 to 5)



Symbol	Address	After Reset
TB0 to TB2	035116 - 035016, 035316 - 035216, 035516 - 035416	Indeterminate
TB3 to TB5	031116 - 031016, 031316 - 031216, 031516 - 031416	Indeterminate

Mode	Function	Setting Range	RW
Timer Mode	If setting value is *n*, a count source is divided by *n+1*	000016 to FFFF16	RW
Event Counter Mode	If setting value is *n*, a count source is divided by *n+1*(2)	000016 to FFFF16	RW
Pulse Period/Pulse Width Measurement Mode	A count source is incremented between one valid edge and another valid edge of TBiIN pulse	————	RO

NOTES:
1. Use 16-bit data for read and write operations.
2. The TBi register counts the number of external input pulses or the number of times another timer overflows and underflows.

Figure 14.17 TB0 to TB5 Registers

Timer Bi Mode Register (i=0 to 5)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
TB0MR0 to TB5MR	$035B_{16}$, $035C_{16}$, $035D_{16}$, $031B_{16}$, $031C_{16}$, $031D_{16}$	$00XX\ 0000_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation Mode Select Bit	b1b0 0 0 : Timer mode 0 1 : Event counter mode 1 0 : Pulse period measurement mode, pulse width measurement mode 1 1 : Do not set to this value	RW
TMOD1			RW
MR0	———	Function varies depending on operation mode (1, 2)	RW
MR1			RW
MR2			RW
MR3			RW
TCK0	Count Source Select Bit	Function varies depending on operation mode	RW
TCK1			RW

NOTES:
1. Only MR2 bits in the TB0MR and TB3MR registers are enabled.
2. Nothing is assigned in the MR2 bit in the TB1MR, TB2MR, TB4MR and TB5MR registers. When write, set to "0". When read, its content is indeterminate.

Count Start Flag

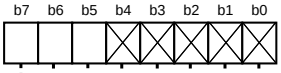
b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
TABSR	0340_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA1S	Timer A1 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA2S	Timer A2 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA3S	Timer A3 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA4S	Timer A4 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB0S	Timer B0 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB1S	Timer B1 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB2S	Timer B2 Count Start Flag	0 : Stops counting 1 : Starts counting	RW

Figure 14.18 TB0MR to TB5MR Registers, TABSR Register

Timer B3, B4,B5 Count Start Flag



Symbol	Address	After Reset
TBSR	0300_{16}	$000X\ XXXX_2$

Bit Symbol	Bit Name	Function	RW
____ (b4 - b0)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
TB3S	Timer B3 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB4S	Timer B4 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB5S	Timer B5 Count Start Flag	0 : Stops counting 1 : Starts counting	RW

Figure 14.19 TBSR Register

Table 14.8 Settings for the TBiIN Pins (i=0 to 5)

Port Name	Function	Setting	
		PS1, PS3(1) Registers	PD7, PD9(1) Registers
$P9_0$	$TB0_{IN}$	PS3_0=0	PD9_0=0
$P9_1$	$TB1_{IN}$	PS3_1=0	PD9_1=0
$P9_2$	$TB2_{IN}$	PS3_2=0	PD9_2=0
$P9_3$	$TB3_{IN}$	PS3_3=0	PD9_3=0
$P9_4$	$TB4_{IN}$	PS3_4=0	PD9_4=0
$P7_1$	$TB5_{IN}$	PS1_1=0	PD7_1=0

NOTES:
1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

14.2.1 Timer Mode

In timer mode, the timer counts an internally generated count source (see Table 14.9). Figure 14.20 shows the TBiMR register (i=0 to 5) in timer mode.

Table 14.9 Specifications in Timer Mode

Item	Specification
Count Source	f_1, f_8, f_{2n}(1), f_{C32}
Count Operation	The timer decrements the counter • When the timer underflows, the content of the reload register is reloaded into the count register and counting resumes
Divide Ratio	1/(n+1) n: setting value of the TBi register (i=0 to 5) 0000_{16} to $FFFF_{16}$
Count Start Condition	The TBiS bits in the TABSR or TBSR registers are set to "1" (starts counting)
Count Stop Condition	The TBiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer underflows
TBi_{IN} Pin Function	Programmable I/O port
Read from Timer	The TBi register indicates counter value
Write to Timer	• When the counter stops or before the first count source after counter start, the value written to the TBi register is also written to both reload register and counter • While counting, the value written to the TBi register is written to the reload register (It is transferred to the counter at the next reload timing)

NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Timer Bi Mode Register (i=0 to 5) (Timer Mode)

b7	b6	b5	b4	b3	b2	b1	b0
		0				0	0

Symbol	Address	After reset
TB0MR to TB5MR	$035B_{16}$, $035C_{16}$, $035D_{16}$, $031B_{16}$, $031C_{16}$, $031D_{16}$	$00XX\ 0000_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation Mode Select Bit	b1b0 0 0 : Timer mode	RW
TMOD1			RW
MR0	Disabled in timer mode. Can be set to "0" or "1".		RW
MR1			RW
MR2	TB0MR, TB3MR registers: Set to "0" in timer mode		RW
	TB1MR, TB2MR TB4MR, TB5MR registers: Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
MR3	Set to "0" in timer mode		RW
TCK0	Count Source Select Bit	b7 b6 0 0 : f_1 0 1 : f_8 1 0 : f_{2n}(1) 1 1 : f_{C32}	RW
TCK1			RW

NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Figure 14.20 TB0MR to TB5MR Registers

14.2.2 Event Counter Mode

In event counter mode, the timer counts how many external signals are applied or how many times another timer overflows and underflows. (See Table 14.10) Figure 14.21 shows the TBiMR register (i=0 to 5) in event counter mode.

Table 14.10 Specifications in Event Counter Mode

Item	Specification
Count Source	• External signal applied to the TBiIN pin (i = 0 to 5) (valid edge can be selected by program) • TBj overflows or underflows (j=i-1, except j=2 when i=0, j=5 when i=3)
Count Operation	• The timer decrements the counter When the timer underflows, the content of the reload register is reloaded into the count register to continue counting
Divide Ratio	1/(n+1) n : setting value of the TBi register 0000$_{16}$ to FFFF$_{16}$
Count Start Condition	The TBiS bit in the TABSR or TBSR register is set to "1" (starts counting)
Count Stop Condition	The TBiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer underflows
TBiIN Pin Function	Programmable I/O port or count source input
Read from Timer	The TBi register indicates the value of the counter
Write to Timer	• When the counter stops or before the first count source after counter start, the value written to the TBi register is also written to both reload register and counter • While counting, the value written to the TBi register is written to the reload register (It is transferred to the counter at the next reload timing)

Timer Bi Mode Register (i=0 to 5) (Event Counter Mode)

b7	b6	b5	b4	b3	b2	b1	b0
		0				0	1

Symbol	Address	After reset
TB0MR to TB5MR	035B16, 035C16, 035D16, 031B16, 031C16, 031D16	00XX 00002

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation Mode Select Bit	b1 b0 0 1 : Event counter mode	RW
TMOD1			RW
MR0	Count Polarity Select Bit(1)	b3 b2 0 0 : Counts falling edges of external signal 0 1 : Counts rising edges of external signal 1 0 : Counts falling and rising edges of external signal 1 1 : Do not set to this value	RW
MR1			RW
MR2	TB0MR and TB3MR registers: Set to "0" in event counter mode		RW
	TB1MR, TB2MR, TB4MR and TB5MR registers: Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
MR3	Disabled in event counter mode. When write, set to "0". When read, its content is indeterminate.		—
TCK0	Disabled in event counter mode. Can be set to "0" or "1".		RW
TCK1	Count Source Select Bit	0 : Input signal from the TBiIN pin 1 : TBj overflows or underflows(2)	RW

NOTES:
1. The MR0 and MR1 bits are enabled when the TCK1 bit is set to "0" (input signal from the TBiIN pin). The MR1 bit can be set to either "0" or "1", when the TCK1 bit is set to "1" (timer overflow or underflow).
2. j=i – 1, except j=2 when i=0 and j=5 when i=3.

Figure 14.21 TB0MR to TB5MR Registers

14.2.3 Pulse Period/Pulse Width Measurement Mode

In pulse period/pulse width measurement mode, the timer measures pulse period or pulse width of an external signal. (See Table 14.11) Figure 14.22 shows the TBiMR register (i=0 to 5) in pulse period/pulse width measurement mode. Figure 14.23 shows an example of an operation timing when measuring a pulse period. Figure 14.24 shows an example of the pulse width measurement.

Table 14.11 Specifications in Pulse Period/Pulse Width Measurement Mode

Item	Specification
Count Source	f_1, f_8, f_{2n}(3), f_{C32}
Count Operation	• The timer increments the counter Counter value is transferred to the reload register on the valid edge of a pulse to be measured. It is set to "0000_{16}" and the timer continues counting
Count Start Condition	The TBiS bit (i=0 to 5) in the TABSR or TBSR register is set to "1" (starts counting)
Count Stop Condition	The TBiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	• On the valid edge of a pulse to be measured(1) • The timer overflows The MR3 bit in the TBiMR register is set to "1" (overflow) simultaneously. When the TBiS bit is set to "1" (start counting) and the next count source is counted after setting the MR3 bit to "1" (overflow), the MR3 bit can be set to "0" (no overflow) by writing to the TBiMR register.
TBi_{IN} Pin Function	Input for a pulse to be measured
Read from Timer	The TBi register indicates reload register values (measurement results)(2)
Write to Timer	Value written to the TBi register can be written to neither reload register nor counter

NOTES:

1. No interrupt request is generated when the pulse to be measured is on the first valid edge after the timer has started counting.
2. The TBi register is in an indeterminate state until the pulse to be measured is on the second valid edge after the timer has started counting.
3. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Timer Bi Mode Register (i=0 to 5)
(Pulse Period / Pulse Width Measurement Mode)

b7	b6	b5	b4	b3	b2	b1	b0
						1	0

Symbol	Address	After reset
TB0MR to TB5MR	$035B_{16}$, $035C_{16}$, $035D_{16}$, $031B_{16}$, $031C_{16}$, $031D_{16}$	$00XX\ 0000_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation Mode Select Bit	b1 b0 1 0 : Pulse period measurement mode, pulse width measurement mode	RW
TMOD1			RW
MR0	Measurement Mode Select Bit	b3 b2 0 0 : Pulse period measurement 1 0 1 : Pulse period measurement 2 1 0 : Pulse width measurement 1 1 : Do not set to this value (Note 1)	RW
MR1			RW
MR2	TB0MR, TB3MR registers: Set to "0" in pulse period/pulse width measurement mode		RW
	TB1MR, TB2MR TB4MR, TB5MR registers: Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
MR3	Timer Bi Overflow Flag(2)	0 : No overflow 1 : Overflow	RO
TCK0	Count Source Select Bit	b7 b6 0 0 : f_1 0 1 : f_8 1 0 : f_{2n}(3) 1 1 : f_{C32}	RW
TCK1			RW

NOTES:
1. The MR1 to MR0 bits selects the following measurements.
   Pulse period measurement 1 (MR1 to MR0 bits = 00_2) :
   Measures between the falling edge and the next falling edge of a pulse to be measured
   Pulse period measurement 2 (MR1 to MR0 bits = 01_2) :
   Measures between the rising edge and the next rising edge of a pulse to be measured
   Pulse width measurement (MR1 to MR0 bits = 10_2) :
   Measures between a falling edge and the next rising edge of a pulse to be measured and between the rising edge and the next falling edge of a pulse to be measured
2. The MR3 bit is indeterminate when reset.
   When the timer overflows, the MR3 bit is set to "1" (overflow) simultaneously. When the TBiS bit is set to "1" (start counting) and the next count source is counted after the MR3 bit is set to "1", the MR3 bit is set to "0" (no overflow) by writing again.
   The MR3 bit cannot be set to "1" by program.
3. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Figure 14.22 TB0MR to TB5MR Registers

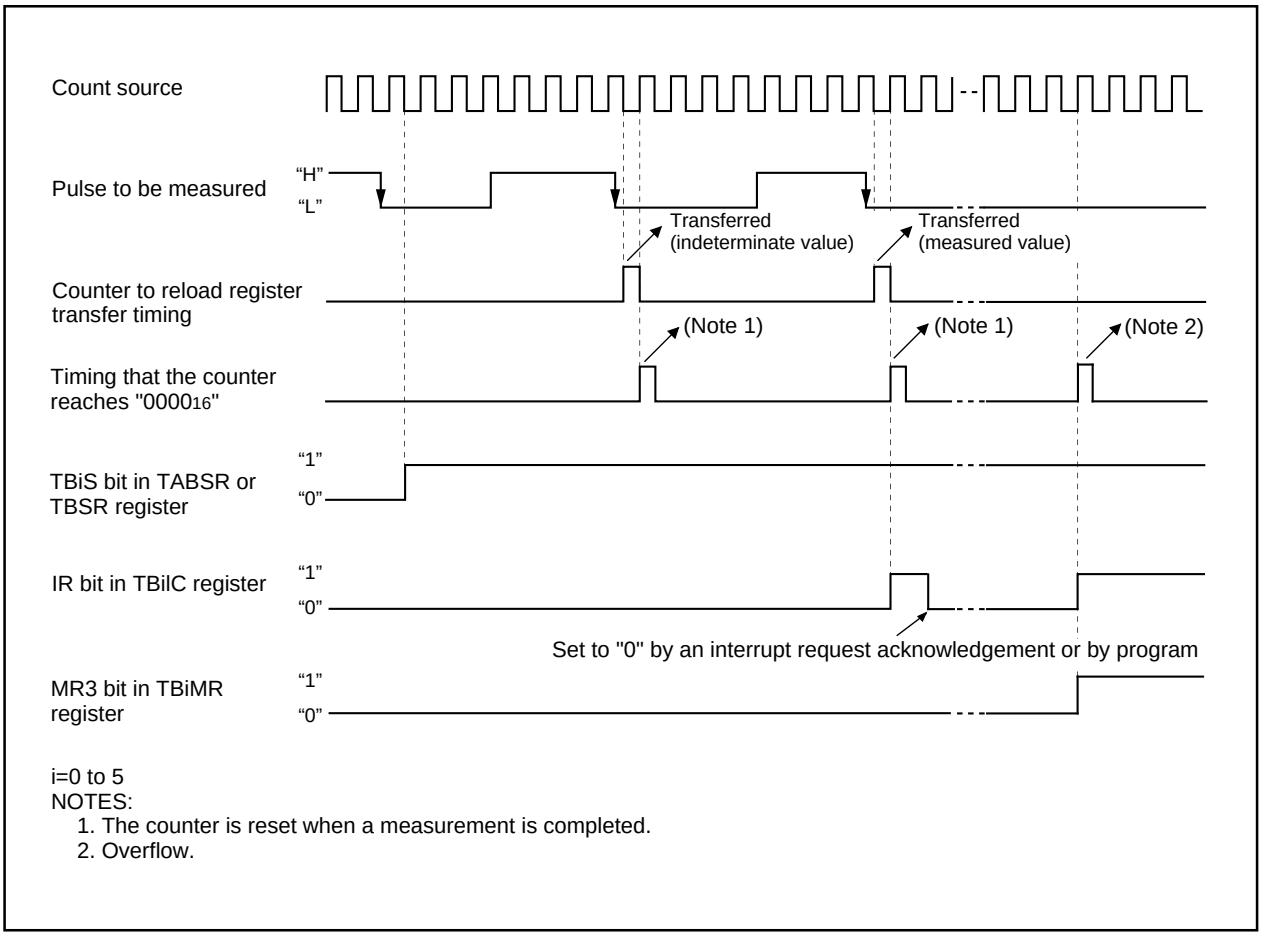


Figure 14.23 Pulse Period 1 Measurement

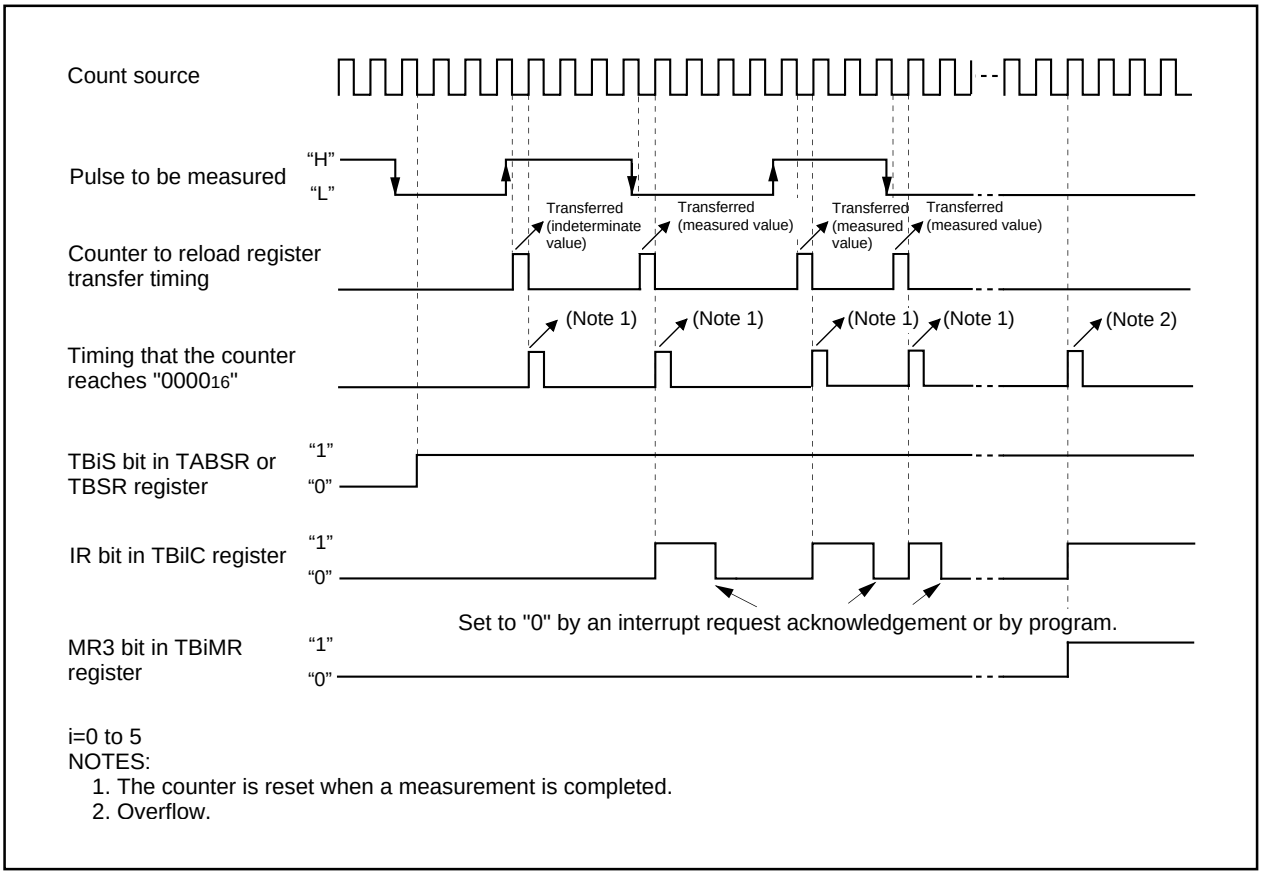


Figure 14.24 Pulse Width Measurement

15. Three-Phase Motor Control Timer Functions

Three-phase motor driving waveform can be output by using the timers A1, A2, A4 and B2. Table 15.1 lists specifications of the three-phase motor control timer functions. Table 15.2 lists pin settings. Figure 15.1 shows a block diagram. Figures 15.2 to 15.7 show registers associated with the three-phase control timer functions.

Table 15.1 Three-Phase Motor Control Timer Functions Specification

Item	Specification
Three-Phase Waveform Output Pin	Six pins (U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$)
Forced Cutoff(1)	Apply a low-level signal ("L") to the $\overline{NMI}$ pin
Timers to be Used	Timer A4, A1, A2 (used in one-shot timer mode) Timer A4: U- and $\overline{U}$-phase waveform control Timer A1: V- and $\overline{V}$-phase waveform control Timer A2: W- and $\overline{W}$-phase waveform control Timer B2 (used in timer mode) Carrier wave cycle control Dead time timer (three 8-bit timers share reload register) Dead time control
Output Waveform	Triangular wave modulation, Sawtooth wave modification Can output a high-level waveform or a low-level waveform for one cycle Can set positive-phase level and negative-phase level separately
Carrier Wave Cycle	Triangular wave modulation: *count source* x *(m+1)* x *2* Sawtooth wave modulation: *count source* x *(m+1)* m: setting value of the TB2 register, 0000_{16} to $FFFF_{16}$ Count source: f_1, f_8, f_{2n}(2), f_{c32}
Three-Phase PWM Output Width	Triangular wave modulation: *count source* x *n* x *2* Sawtooth wave modulation: *count source* x *n* n : setting value of the TA4, TA1 and TA2 register (of the TA4, TA41, TA1, TA11, TA2 and TA21 registers when setting the INV11 bit to "1"), 0001_{16} to $FFFF_{16}$ Count source: f_1, f_8, f_{2n}(2), f_{c32}
Dead Time	*Count source* x *p*, or no dead time p: setting value of the DTT register, 01_{16} to FF_{16} Count source: f_1, or f_1 divided by 2
Active Level	Selected from a high level ("H") or low level ("L")
Positive and Negative-Phase Concurrent Active Disable Function	Positive and negative-phases concurrent active disable function Positive and negative-phases concurrent active detect function
Interrupt Frequency	For the timer B2 interrupt, one carrier wave cycle-to-cycle basis through 15 time- carrier wave cycle-to-cycle basis can be selected

NOTES:

1. Forced cutoff by the signal applied to the $\overline{NMI}$ pin is available when the INV02 bit is set to "1" (three-phase motor control timer functions) and the INV03 bit is set to "1" (three-phase motor control timer output enabled).
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Table 15.2 Pin Settings

Pin	Setting		
	PS1, PS2 Registers(1)	PSL1, PSL2 Registers	PSC Register
P72/V	PS1_2 =1	PSL1_2 =0	PSC_2 =1
P73/$\overline{V}$	PS1_3 =1	PSL1_3 =1	PSC_3 =0
P74/W	PS1_4 =1	PSL1_4 =1	PSC_4 =0
P75/$\overline{W}$	PS1_5 =1	PSL1_5 =0	——
P80/U	PS2_0 =1	PSL2_0 =1	——
P81/$\overline{U}$	PS2_1 =1	PSL2_1 =0	——

NOTES:
1. Set the PS1_2 to PS1_5 and PS2_0 to PS2_1 bits in the PS1 and PS2 registers to "1" after the INV02 bit is set to "1".

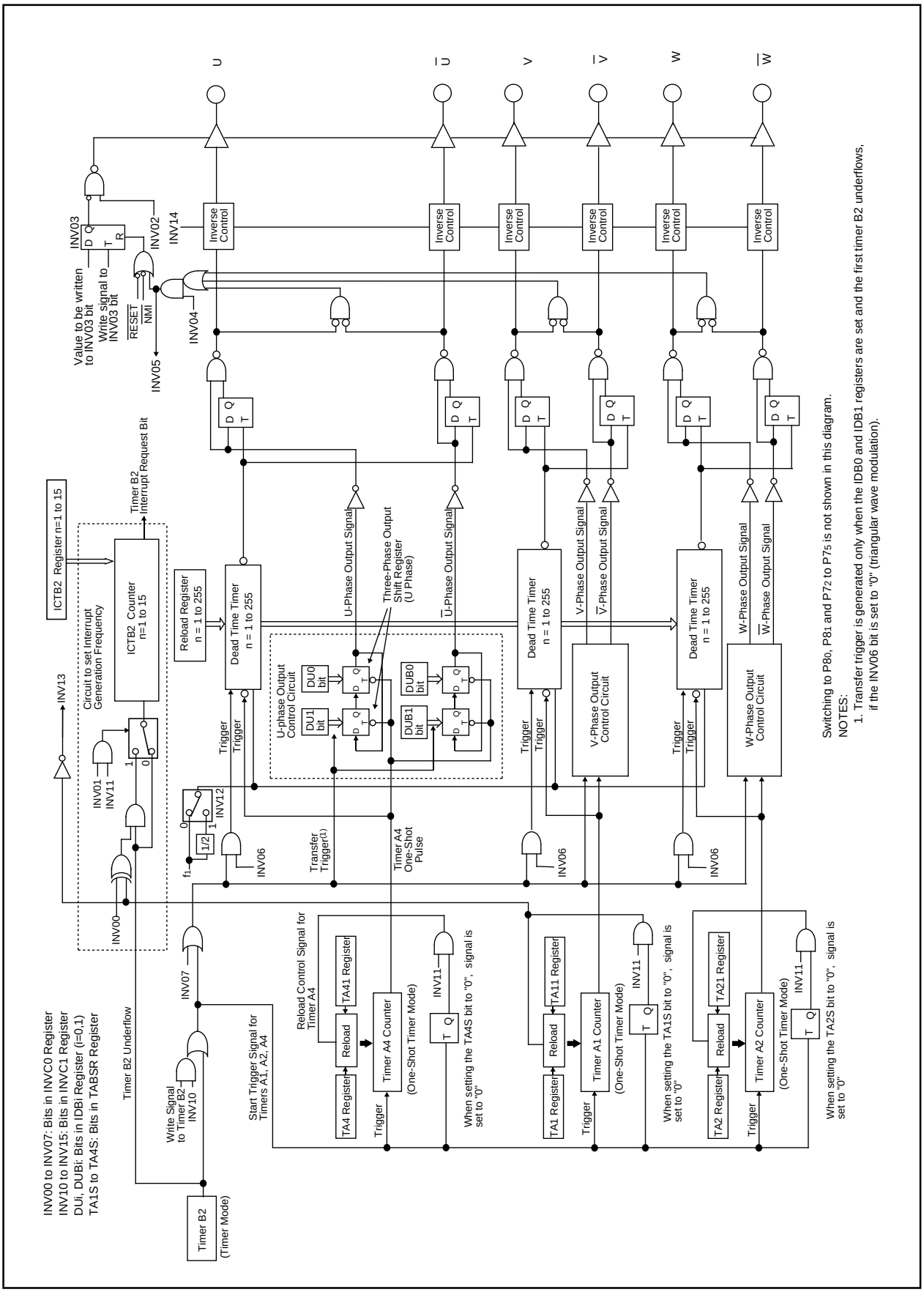
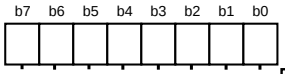


Figure 15.1 Three-Phase Motor Control Timer Functions Block Diagram

Three-Phase PWM Control Register 0(1)



Symbol	Address	After Reset
INVC0	0308₁₆	00₁₆

Bit Symbol	Bit Name	Function	RW
INV00	Interrupt Enable Output Polarity Select Bit(3)	0: The ICTB2 counter is incremented by one on the rising edge of the timer A1 reload control signal 1: The ICTB2 counter is incremented by one on the falling edge of the timer A1 reload control signal	RW
INV01	Interrupt Enable Output Specification Bit(2, 3)	0: ICTB2 counter is incremented by one when timer B2 underflows 1: Selected by the INV00 bit	RW
INV02	Mode Select Bit(4, 5, 6)	0: No three-phase control timer functions 1: Three-phase control timer function	RW
INV03	Output Control Bit(6, 7)	0: Disables three-phase control timer output 1: Enables three-phase control timer output	RW
INV04	Positive and Negative-Phases Concurrent Active Disable Function Enable Bit	0: Enables concurrent active output 1: Disables concurrent active output	RW
INV05	Positive and Negative-Phases Concurrent Active Output Detect Flag(8)	0: Not detected 1: Detected	RW
INV06	Modulation Mode Select(9, 10)	0: Triangular wave modulation mode 1: Sawtooth wave modulation mode	RW
INV07	Software Trigger Select	Transfer trigger is generated when the INV07 bit is set to "1". Trigger to the dead time timer is also generated when setting the INV06 bit to "1". Its value is "0" when read.	RW

NOTES:

1. Set the INVC0 register after the PRC1 bit in the PRCR register is set to "1" (write enable). Rewrite the INV00 to INV02 and INV06 bits when the timers A1,A2, A4 and B2 stop.
2. Set the INV01 bit to "1" after setting the ICTB2 register .
3. The INV00 and INV01 bits are enabled only when the INV11 bit is set to "1" (three-phase mode 1). The ICTB2 counter is incremented by one every time the timer B2 underflows, regardless of INV00 and INV01 bit settings, when the INV11 bit is set to "0" (three-phase mode).
   When setting the INV01 bit to "1", set the timer A1 count start flag before the first timer B2 underflow.
   When the INV00 bit is set to "1", the first interrupt is generated when the timer B2 underflows *n-1* times, if *n* is the value set in the ICTB2 counter. Subsequent interrupts are generated every *n* times the timer B2 underflows.
4. Set the INV02 bit to "1" to operate the dead time timer, U-, V-and W-phase output control circuits and ICTB2 counter.
5. Set pins after the INV02 bit is set to "1". See Table 15.2 for pin settings.
6. When the INV02 bit is set to "1" (three-phase control timer functions) and the INV03 bit to "0" (three-phase control timer output disabled), U, $\overline{U}$, V, $\overline{V}$, W and $\overline{W}$ pins, including pins shared with other output functions, enter a high-impedance state.
7. The INV03 bit is set to "0" when the followings occurs :
   - Reset
   - A concurrent active state occurs while INV04 bit is set to "1"
   - The INV03 bit is set to "0" by program
   - A signal applied to the $\overline{NMI}$ pin changes "H" to "L"
8. The INV05 bit can not be set to "1" by program. Set the INV04 bit to "0", as well, when setting the INV05 bit to "0".
9. The following table describes how the INV06 bit works.

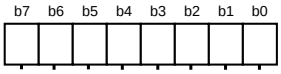
Item	INV06 = 0	INV06 = 1
Mode	Triangular wave modulation mode	Sawtooth wave modulation mode
Timing to Transfer from the IDB0 and IDB1 Registers to Three-Phase Output Shift Register	Transferred once by generating a transfer trigger after setting the IDB0 and IDB1 registers	Transferred every time a transfer trigger is generated
Timing to Trigger the Dead Time Timer when the INV16 Bit=0	On the falling edge of a one-shot pulse of the timer A1, A2 or A4	By a transfer trigger, or the falling edge of a one-shot pulse of the timer A1, A2 or A4
INV13 Bit	Enabled when the INV11 bit=1 and the INV06 bit=0	Disabled

Transfer trigger : Timer B2 underflows and write to the INV07 bit, or write to the TB2 register when INV10 = 1

10. When the INV06 bit is set to "1", set the INV11 bit to "0" (three-phase mode 0) and the PWCON bit in the TB2SC register to "0" (reload timer B2 with timer B2 underflow).

Figure 15.2 INVC0 Register

Three-Phase PWM Control Register 1(1)



Symbol	Address	After Reset
INVC1	0309_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
INV10	Timer A1, A2 and A4 Start Trigger Select Bit	0: Timer B2 underflow 1: Timer B2 underflow and write to the timer B2	RW
INV11	Timer A1-1, A2-1, A4-1 Control Bit(2, 3)	0: Three-phase mode 0 1: Three-phase mode 1	RW
INV12	Dead Time Timer Count Source Select Bit	0 : f_1 1 : f_1 divided-by-2	RW
INV13	Carrier Wave Detect Flag(4)	0: Timer A1 reload control signal is "0" 1: Timer A1 reload control signal is "1"	RO
INV14	Output Polarity Control Bit	0 : Active "L" of an output waveform 1 : Active "H" of an output waveform	RW
INV15	Dead Time Disable Bit	0: Enables dead time 1: Disables dead time	RW
INV16	Dead Time Timer Trigger Select Bit	0: Falling edge of a one-shot pulse of the timer A1, A2, A4(5) 1: Rising edge of the three-phase output shift register (U-, V-, W-phase)	RW
—— (b7)	Reserved Bit	Set to "0"	RW

NOTES:

1. Rewrite the INVC1 register after the PRC1 bit in the PRCR register is set to "1" (write enable). The timers A1, A2, A4, and B2 must be stopped during rewrite.
2. The following table lists how the INV11 bit works.

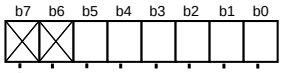
Item	INV11 = 0	INV11 = 1
Mode	Three-phase mode 0	Three-phase mode 1
TA11, TA21 and TA41 Registers	Not used	Used
INV00 and INV01 Bits in the INVC0 Register	Disabled. The ICTB2 counter is incremented whenever the timer B2 underflows	Enabled
INV13 Bit	Disabled	Enabled when INV11=1 and INV06=0

3. When the INV06 bit is set to "1" (sawtooth wave modulation mode), set the INV11 bit to "0" (three-phase mode 0). Also, when the INV11 bit is set to "0", set the PWCON bit in the TB2SC register to "0" (timer B2 is reloaded when the timer B2 underflows).
4. The INV13 bit is enabled only when the INV06 bit is set to "0" (Triangular wave modulation mode) and the INV11 bit to "1" (three-phase mode 1).
5. If the following conditions are all met, set the INV16 bit to "1" (rising edge of the three-phase output shift register).
   - The INV15 bit is set to "0" (dead time timer enabled)
   - The Dij bit (i=U, V or W, j=0, 1) and DiBj bit always have different values when the INV03 bit is set to "1". (The positive-phase and negative-phase always output opposite level signals.)

   If above conditions are not met, set the INV16 bit to "0" (falling edge of a one-shot pulse of the timer A1, A2, A4).

Figure 15.3 INVC1 Register

Three-Phase Output Buffer Register i(1) (i=0, 1)

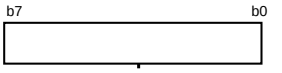


Symbol	Address	After Reset
IDB0, IDB1	030A16, 030B16	XX11 11112

Bit Symbol	Bit Name	Function	RW
DUi	U-Phase Output Buffer i	Write output level 0: Active level 1: Inactive level When read, the value of the three-phase shift register is read.	RW
DUBi	$\overline{U}$-Phase Output Buffer i		RW
DVi	V-Phase Output Buffer i		RW
DVBi	$\overline{V}$-Phase Output Buffer i		RW
DWi	W-Phase Output Buffer i		RW
DWBi	$\overline{W}$-Phase Output Buffer i		RW
___ (b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is "0."		RO

NOTES:
1. Values of the IDB0 and IDB1 registers are transferred to the three-phase output shift register by a transfer trigger.
   After the transfer trigger occurs, the values written in the IDB0 register determine each phase output signal first. Then the value written in the IDB1 register on the falling edge of timers A1, A2 and A4 one-shot pulse determines each phase output signal.

Dead Time Timer(1, 2)



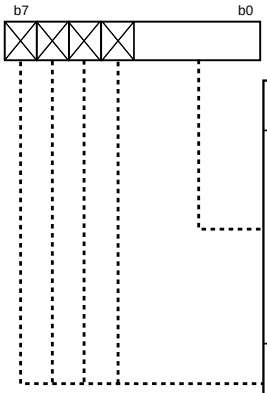
Symbol	Address	After Reset
DTT	030C16	Indeterminate

Function	Setting Range	RW
If setting value is *n*, the timer stops when counting *n* times a count source selected by the INV12 bit after start trigger occurs. Positive or negative phase, which changes from inactive level to active level, shifts when the dead time timer stops.	1 to 255	WO

NOTES:
1. Use the MOV instruction to set the DTT register.
2. The DTT register is enabled when the INV15 bit in the INVC1 register is set to "0" (dead time enabled). No dead time can be set when the INV15 bit is set to "1" (dead time disabled). The INV06 bit in the INVC0 register determines start trigger of the DTT register.

Figure 15.4 IDB0, IDB1 and DTT Registers

Timer B2 Interrupt Generation Frequency Set Counter(1, 2, 3)

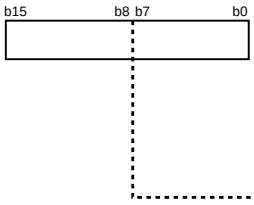


Symbol	Address	After Reset
ICTB2	030D16	Indeterminate

Function	Setting Range	RW
When the INV01 bit is set to "0" (the ICTB2 counter increments whenever the timer B2 underflows) and the setting value is *n*, the timer B2 interrupt is generated every *n*th time timer B2 underflow occurs. When the INV01 bit is set to "1" (the INV00 bit selects count timing of the ICTB2 counter) and setting value is *n*, the timer B2 interrupt is generated every *n*th time timer B2 underflow meeting the condition selected in the INV00 bit occurs .	1 to 15	WO
Nothing is assigned. When write, set to "0".		—

NOTES:
1. Use the MOV instruction to set the ICTB2 register.
2. If the INV01 bit in the INVC0 register is set to "1", set the ICTB2 register when the TB2S bit is set to "0" (timer B2 counter stopped),
   If the INV01 bit is set to "0" and the TB2S bit to "1" (timer B2 counter start), do not set the ICTB2 register when the timer B2 underflows.
3. If the INV00 bit is set to "1", the first interrupt is generated when the timer B2 underflows *n-1* times, *n* being the value set in the ICTB2 counter. Subsequent interrupts are generated every *n* times the timer B2 underflows.

Timer Ai, Ai-1 Register (i=1, 2, 4)(1, 2, 3, 4, 5, 6, 7)

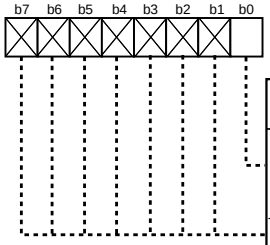


Symbol	Address	After Reset
TA1, TA2, TA4	034916 - 034816, 034B16 - 034A16, 034F16 - 034E16	Indeterminate
TA11, TA21, TA41	030316 - 030216, 030516 - 030416, 030716 - 030616	Indeterminate

Function	Setting Range	RW
If setting value is *n*, the timer stops when the *n*th count source is counted after a start trigger is generated. Positive phase changes to negative phase, and vice versa, when the timers A1, A2 and A4 stop.	000016 to FFFF16	WO

NOTES:
1. Use a 16-bit data for read and write..
2. If the TAi or TAi1 register is set to "000016", no counters start and no timer Ai interrupt is generated.
3. Use the MOV instruction to set the TAi and TAi1 registers.
4. When the INV15 bit in the INVC1 register is set to "0" (dead timer enabled), phase switches from an inactive level to an active level when the dead time timer stops.
5. When the INV11 bit is set to "0" (three-phase mode 0), the value of the TAi register is transferred to the reload register by a timer Ai start trigger.
   When the INV11 bit is set to "1" (three-phase mode 1), the value of the TAi1 register is first transferred to the reload register by a timer Ai start trigger. Then, the value of the TAi register is transferred by the next trigger. The values of the TAi1 and TAi registers are transferred alternately to the reload register with every timer Ai start trigger.
6. Do not write to these registers when the timer B2 underflows.
7. Follow the procedure below to set the TAi1 register.
   (1) Write value to the TAi1 register.
   (2) Wait one timer Ai count source cycle.
   (3) Write the same value as (1) to the TAi1 register.

Timer B2 Special Mode Register



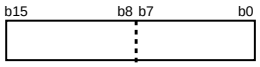
Symbol	Address	After Reset
TB2SC	035E16	XXXX XXX02

Bit Symbol	Bit Name	Function	RW
PWCON	Timer B2 Reload Timing Switching Bit(1)	0 : Timer B2 underflow 1 : Timer A output in odd-number times	RW
Nothing is assigned. When write, set to "0". When read, its content is "0."			—

NOTES:
1. When setting the INV11 bit to "0" (three-phase mode 0) or the INV06 bit to "1" (sawtooth wave modulation mode), set the PWCON bit to "0" (timer B2 underflow).

Figure 15.5 ICTB2 Register, TA1, TA2, TA4, TA11, TA21 and TA41 Registers and TB2SC Register

Timer B2 Register(1)

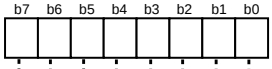


Symbol	Address	After Reset
TB2	0355$_{16}$ - 0354$_{16}$	Indeterminate

Function	Setting Range	RW
If setting value is *n*, count source is divided by *n*+1. The timers A1, A2 and A4 start every time an underflow occurs.	0000$_{16}$ to FFFF$_{16}$	RW

NOTES:
1. Use a 16-bit data for read and write.

Trigger Select Register

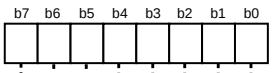


Symbol	Address	After Reset
TRGSR	0343$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
TA1TGL	Timer A1 Event/Trigger Select Bit	Set to "01$_2$" (TB2 underflow) before using a V-phase output control circuit	RW
TA1TGH			RW
TA2TGL	Timer A2 Event/Trigger Select Bit	Set to "01$_2$" (TB2 underflow) before using a W-phase output control circuit	RW
TA2TGH			RW
TA3TGL	Timer A3 Event/Trigger Select Bit	b5 b4 0 0 : Selects an input to the TA3$_{IN}$ pin 0 1 : Selects TB2 overflow(1) 1 0 : Selects TA2 overflow(1) 1 1 : Selects TA4 overflow(1)	RW
TA3TGH			RW
TA4TGL	Timer A4 Event/Trigger Select Bit	Set to "01$_2$" (TB2 underflow) before using a U-phase output control circuit	RW
TA4TGH			RW

NOTES:
1. Overflow or underflow

Count Start Flag



Symbol	Address	After Reset
TABSR	0340$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA1S	Timer A1 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA2S	Timer A2 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA3S	Timer A3 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TA4S	Timer A4 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB0S	Timer B0 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB1S	Timer B1 Count Start Flag	0 : Stops counting 1 : Starts counting	RW
TB2S	Timer B2 Count Start Flag	0 : Stops counting 1 : Starts counting	RW

Figure 15.6 TB2, TRGSR and TABSR Registers

Timer Ai Mode Register (i=1, 2, 4)

b7	b6	b5	b4	b3	b2	b1	b0
		0	1			1	0

Symbol	Address	After Reset
TA1MR, TA2MR, TA4MR	035716, 035816, $035A16$	0000 $0X00_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation Mode Select Bit	Set to "10_2" (one-shot timer mode) with the three-phase motor control timer function	RW
TMOD1			
(b2)	Nothing is assigned. When write, set to "0".		—
MR1	External Trigger Select Bit	Set to "0" with the three-phase motor control timer function	RW
MR2	Trigger Select Bit	Set to "1"(selected by the TRGSR register) with the three-phase motor control timer function	RW
MR3	Set to "0" with the three-phase motor control timer function		RW
TCK0	Count Source Select Bit	b7 b6 0 0 : f_1 0 1 : f_8 1 0 : f_{2n}(1) 1 1 : f_{C32}	RW
TCK1			RW

NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Timer B2 Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
			0			0	0

Symbol	Address	After Reset
TB2MR	$035D16$	00XX 0000_2

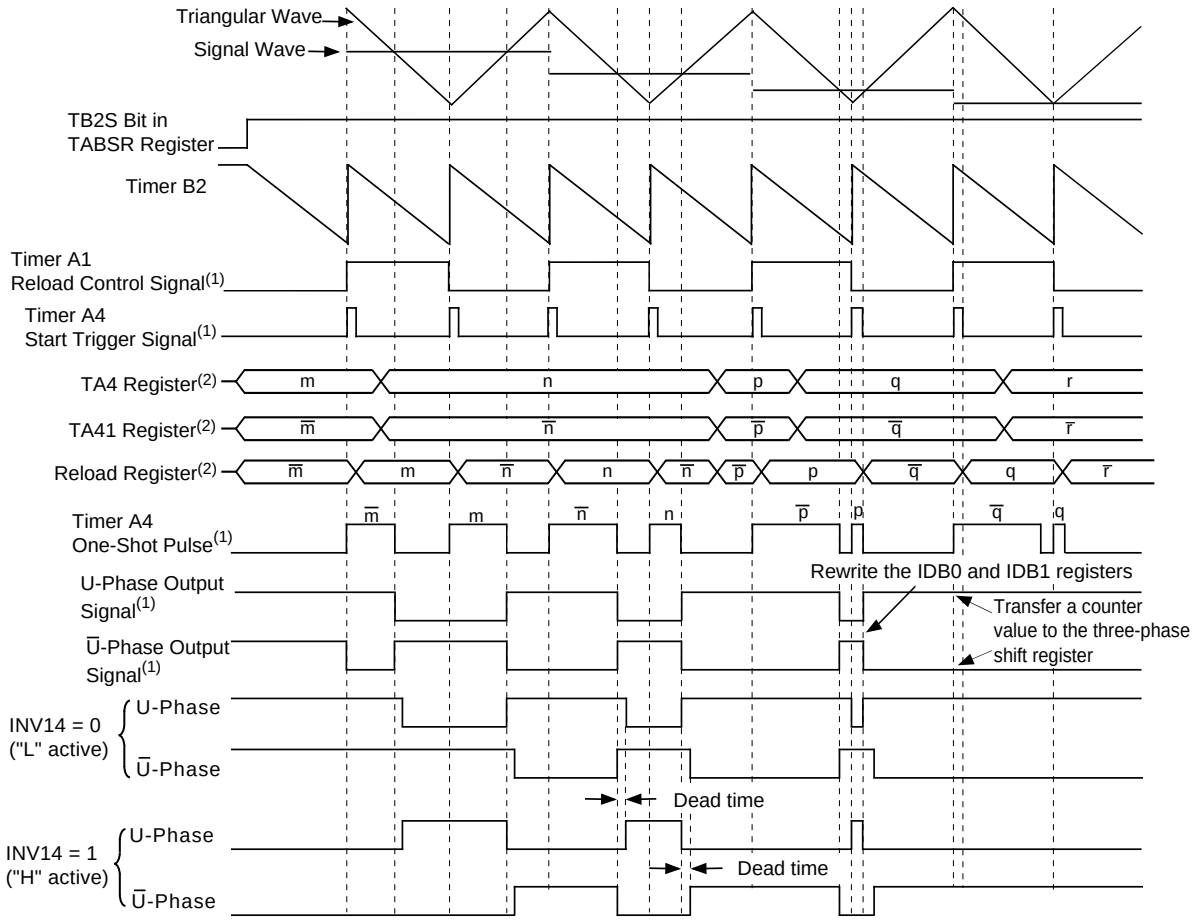
Bit Symbol	Bit Name	Function	RW
TMOD0	Operation Mode Select Bit	Set to "00_2" (timer mode) when using the three-phase motor control timer function	RW
TMOD1			
MR0	Disabled when using the three-phase motor control timer function. When write, set to "0". When read, its content is indeterminate.		—
MR1			
MR2	Set to "0" when using three-phase motor control timer function		RW
MR3	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		RW
TCK0	Count Source Select Bit	b7 b6 0 0 : f_1 0 1 : f_8 1 0 : f_{2n}(1) 1 1 : f_{C32}	RW
TCK1			RW

NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Figure 15.7 TA1MR, TA2MR, TA4MR Registers and TB2MR Register

The three-phase control timer function is available by setting the INV02 bit in the INVC0 register to "1". The timer B2 is used for carrier wave control and timers A4, A1, A2 for three-phase PWM output (U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$) control. An exclusive dead time timer controls dead time. Figure 15.8 shows an example of the triangular modulation waveform. Figure 15.9 shows an example of the sawtooth modulation waveform.

Triangular waveform as a Carrier Wave



INV00, INV01: Bits in the INVC0 register
INV11, INV14: Bits in the INVC1 register

NOTES:
1. Internal signals. See Figure 15.1.
2. Applies only when the INV11 bit is set to "1" (three-phase mode).

The above applies to INVC0 = 00XX11XX$_2$ and INVC1 = 010XXXX0$_2$ (X varies depending on each system.)
Examples of PWM output change are

(a) When INV11=1 (three-phase mode 1)
- INV01=0 and ICTB2=2$_{16}$ (The timer B2 interrupt is generated with every second timer B2 underflow) or INV01=1, INV00=1and ICTB2=1$_{16}$ (The timer B2 interrupt is generated on the falling edge of the timer A1 reload control signal)
- Default value of the timer: TA41=$\overline{m}$, TA4=m
  The TA4 and TA41 registers are changed whenever the timer B2 interrupt is generated.
  First time: TA41=$\overline{n}$, TA4:=n.
  Second time: TA41=$\overline{p}$, TA4=p.
- Default value of the IDB0 and IDB1 registers
  DU0=1, DUB0=0, DU1=0, DUB1=1
  They are changed to DU0=1, DUB0=0, DU1=1, DUB1=0 by the third timer B2 interrupt.

(b) When INV11=0 (three-phase mode 0)
- INV01=0, ICTB2=1$_{16}$ (The timer B2 interrupt is generated whenever the timer B2 underflows)
- Default value of the timer: TA4=$\overline{m}$
  The TA4 register is changed whenever the timer B2 interrupt is generated.
  First time: TA4=m. Second time: TA4=$\overline{n}$.
  Third time: TA4=n. Fourth time: TA=$\overline{p}$.
  Fifth time: TA4=p.
- Default value of the IDB0 and IDB1 registers:
  DU0=1, DUB0=0, DU1=0, DUB1=1
  They are changed to DU0=1, DUB0=0, DU1=1, DUB1=0 by the sixth timer B2 interrupt.

Figure 15.8 Triangular Wave Modulation Operation

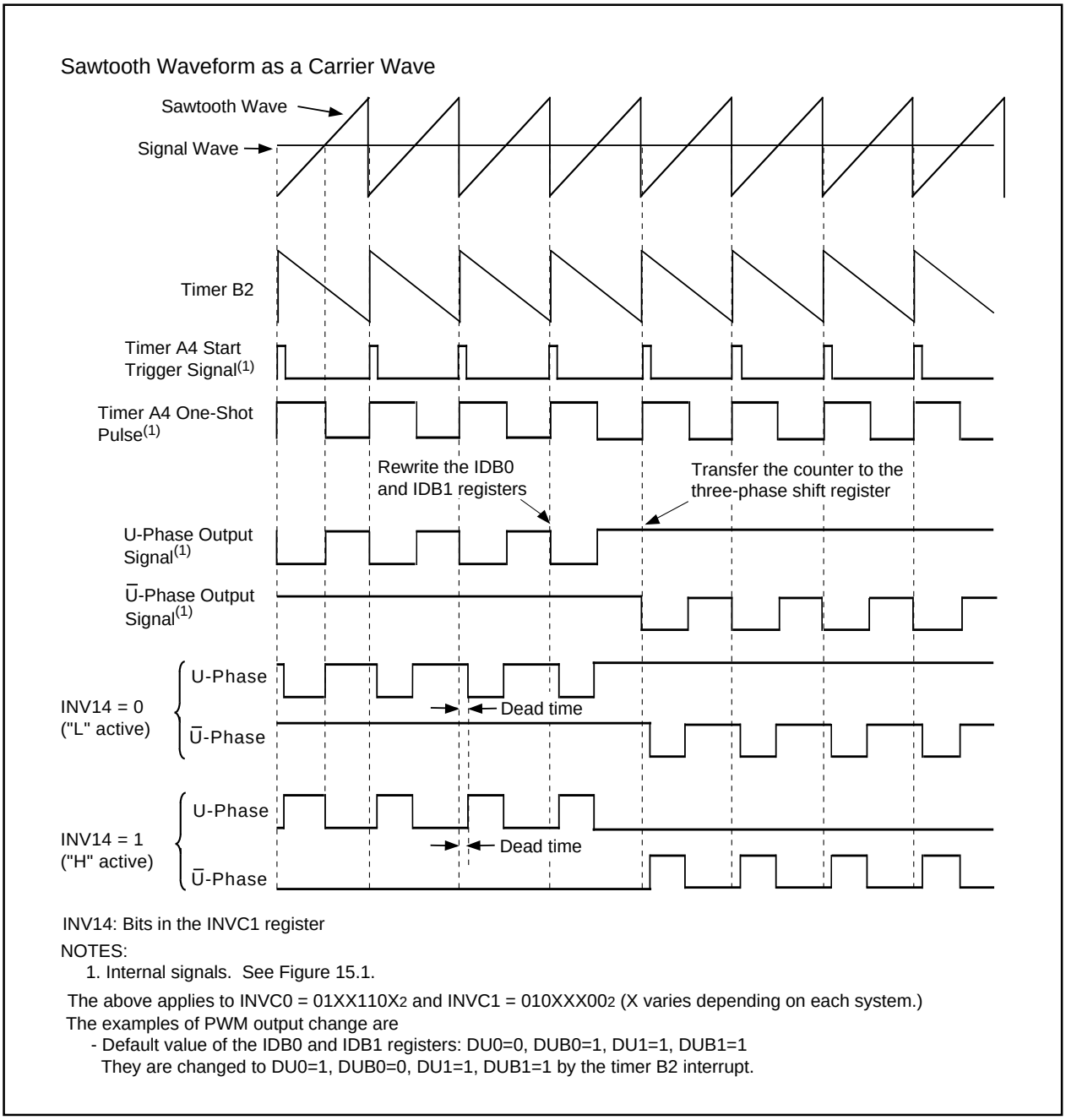


Figure 15.9 Sawtooth Wave Modulation Operation

16. Serial I/O

Serial I/O consists of five channels (UART0 to UART4).

Each UARTi (i=0 to 4) has an exclusive timer to generate the transfer clock and operates independently.

Figure 16.1 shows a UARTi block diagram.

UARTi supports the following modes :

- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode)
- Special mode 1 (I^2C mode)
- Special mode 2
- Special mode 3 (Clock-divided synchronous function, GCI mode)
- Special mode 4 (Bus conflict detect function, IE mode)
- Special mode 5 (SIM mode)

Figures 16.2 to 16.9 show registers associated with UARTi.

Refer to the tables listing each mode for register and pin settings.

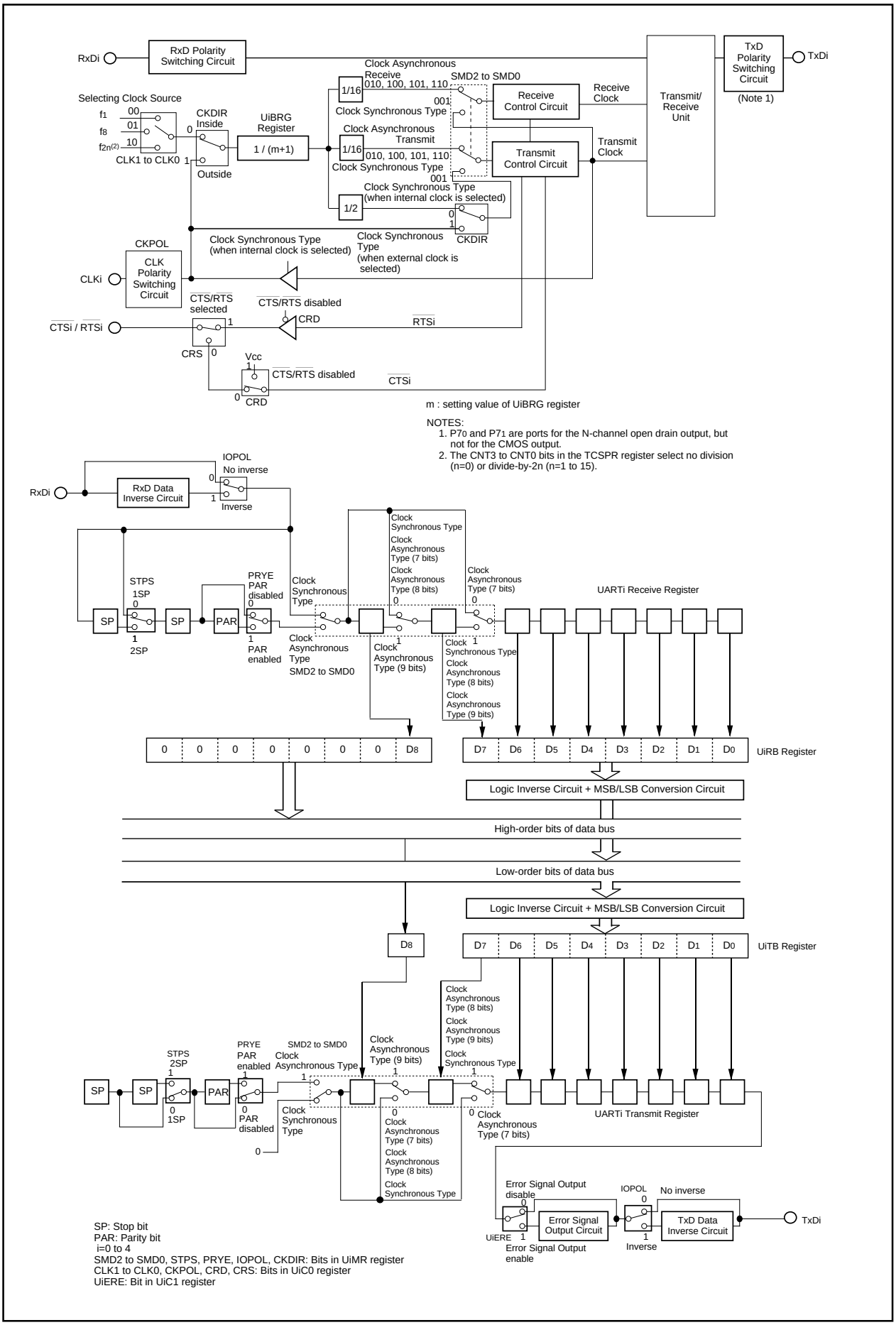
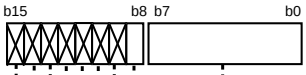


Figure 16.1 UARTi Block Diagram

UARTi Transmit Buffer Register (i=0 to 4)(1)

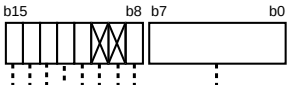


Symbol	Address	After Reset
U0TB to U2TB	036B16-036A16, 02EB16-02EA16, 033B16-033A16	Indeterminate
U3TB, U4TB	032B16-032A16, 02FB16-02FA16	Indeterminate

Bit Symbol	Function	RW
(b7 - b0)	Transmit data (D7 to D0)	WO
(b8)	Transmit data (D8)	WO
(b15 - b9)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.	—

NOTES:
1. Use the MOV instruction to set the UiTB register.

UARTi Receive Buffer Register (i=0 to 4)



Symbol	Address	After Reset
U0RB to U2RB	036F16 - 036E16, 02EF16 - 02EE16, 033F16 - 033E16	Indeterminate
U3RB, U4RB	032F16 - 032E16, 02FF16 - 02FE16	Indeterminate

Bit Symbol	Bit Name	Function	RW
(b7 - b0)	—	Received data (D7 to D0)	RO
(b8)	—	Received data (D8)	RO
(b10 - b9)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
ABT	Arbitration Lost Detect Flag(1)	0: Not detected (win) 1: Detected (lose)	RW
OER	Overrun Error Flag(2)	0: No overrun error occurs 1: Overrun error occurs	RO
FER	Framing Error Flag(2, 3)	0: No framing error occurs 1: Framing error occurs	RO
PER	Parity Error Flag(2, 3)	0: No parity error occurs 1: Parity error occurs	RO
SUM	Error Sum Flag(2, 3)	0: No error occurs 1: Error occurs	RO

NOTES:
1. The ABT bit can be set to "0" only.
2. When the SMD2 to SMD0 bits in the UiMR register is set to "0002" (serial I/O disable) or the RE bit in the UiC1 register is set to "0" (receive disable), the OER, FER, PER and SUM bits are set to "0" (no error occurs).
   When all OER, FER and PER bits are set to "0" (no error), the SUM bit is set to "0" (no error).
   Also, the FER and PER bits are set to "0" by reading low-order bits in the UiRB register.
3. These error flags are disabled when the SMD2 to SMD0 bits in the UiMR register are set to "0012" (clock synchronous serial I/O mode, special mode 2, or special mode 3) or to "0102" (I^2C mode).
   When read, the contents are indeterminate.

Figure 16.2 U0TB to U4TB Registers and U0RB to U4RB Registers

UARTi Baud Rate Register (i=0 to 4)(1, 2)

b7 b0

Symbol	Address	After Reset
U0BRG to U4BRG	0369_{16}, $02E9_{16}$, 0339_{16}, 0329_{16}, $02F9_{16}$	Indeterminate

Function	Setting Range	RW
If the setting value is *m*, the UiBRG register divides a count source by *m+1*	00_{16} to FF_{16}	WO

NOTES:
1. Use the MOV instruction to set the UiBRG register.
2. Set the UiBRG register data transmit and receive is stopped.

UARTi Transmit/Receive Mode Register (i=0 to 4)

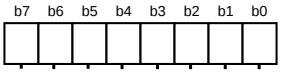
b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
U0MR to U4MR	0368_{16}, $02E8_{16}$, 0338_{16}, 0328_{16}, $02F8_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O Mode Select Bit	b2 b1 b0 0 0 0: Serial I/O disabled 0 0 1: Clock synchronous serial I/O mode 0 1 0: I^2C mode 1 0 0: UART mode, 7-bit transfer data 1 0 1: UART mode, 8-bit transfer data 1 1 0: UART mode, 9-bit transfer data Do not set value other than the above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/External Clock Select Bit	0 : Internal clock 1 : External clock	RW
STPS	Stop Bit Length Select Bit	0 : 1 stop bit 1 : 2 stop bits	RW
PRY	Odd/Even Parity Select Bit	Enables when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity Enable Bit	0 : Disables a parity 1 : Enables a parity	RW
IOPOL	TxD,RxD Input/Output Polarity Switch Bit	0: Not inversed 1: Inverse	RW

Figure 16.3 U0BRG to U4BRG Registers and U0MR to U4MR Registers

UARTi Transmit/Receive Control Register 0 (i=0 to 4)



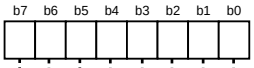
Symbol	Address	After Reset
U0C0 to U4C0	$036C_{16}$, $02EC_{16}$, $033C_{16}$, $032C_{16}$, $02FC_{16}$	$0000\ 1000_2$

Bit Symbol	Bit Name	Function	RW
CLK0	UiBRG Count Source Select Bit	b0 b1 0 0: Selects f_1 0 1: Selects f_8 1 0: Selects f_{2n}(2) 1 1: Do not set to this value	RW
CLK1			RW
CRS	$\overline{CST}/\overline{RTS}$ Function Select Bit	Enabled when CRD=0 0 : Selects $\overline{CTS}$ function 1 : Selects $\overline{RTS}$ function	RW
TXEPT	Transmit Register Empty Flag	0 : Data in the transmit register (during transmission) 1 : No data in the transmit register (transmission is completed)	RO
CRD	$\overline{CTS}/\overline{RTS}$ Disable Bit	0 : Enables $\overline{CTS}/\overline{RTS}$ function 1 : Disables $\overline{CTS}/\overline{RTS}$ function	RW
NCH	Data Output Select Bit(1)	0 : TxDi/SDAi and SCLi are ports for the CMOS output 1 : TxDi/SDAi and SCLi are ports for the N-channel open drain output	RW
CKPOL	CLK Polarity Select Bit	0 : Data is transmitted on the falling edge of the transfer clock and data is received on the rising edge 1 : Data is transmitted on the rising edge of the transfer clock and data is received on the falling edge	RW
UFORM	Transfer Format Select Bit(3)	0 : LSB first 1 : MSB first	RW

NOTES:
1. $P7_0$/TxD2 are ports for the N-channel open drain output, but not for the CMOS output.
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).
3. The UFORM bit is enabled when the SMD2 to SMD0 bits in the UiMR register are set to "001_2" (clock synchronous serial I/O mode), or "101_2" (UART mode, 8-bit transfer data).
   Set this bit to "1" when the SMD2 to SMD0 bits are set to "010_2" (I^2C mode), and to "0" when the SMD2 to SMD0 bits are set to "100_2"(UART mode, 7-bit transfer data) or "110_2"(UART mode, 9-bit transfer data)

Figure 16.4 U0C0 to U4C0 Registers

UARTi Transmit/Receive Control Register 1 (i=0 to 4)

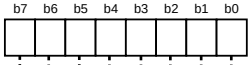


Symbol	Address	After Reset
U0C1 to U4C1	$036D_{16}$, $02ED_{16}$, $033D_{16}$, $032D_{16}$, $02FD_{16}$	$0000\ 0010_2$

Bit Symbol	Bit Name	Function	RW
TE	Transmit Enable Bit	0: Transmit disable 1: Transmit enable	RW
TI	Transmit Buffer Empty Flag	0: Data in the UiTB register 1: No data in the UiTB register	RO
RE	Receive Enable Bit	0: Receive disable 1: Receive enable	RW
RI	Receive Complete Flag	0: Data in the UiRB register 1: No data in the UiRB register	RO
UiIRS	UARTi Transmit Interrupt Cause Select Bit	0: No data in the UiTB register (TI = 1) 1: Transmission is completed (TXEPT = 1)	RW
UiRRM	UARTi Continuous Receive Mode Enable Bit	0: Disables continuous receive mode to be entered 1: Enables continuous receive mode to be entered	RW
UiLCH	Data Logic Select Bit	0: Not inversed 1: Inverse	RW
SCLKSTPB /UiERE	Clock-Divided Synchronous Stop Bit / Error Signal Output Enable Bit(1)	Clock-divided synchronous stop bit (special mode 3) 0: Stops synchronizing 1: Starts synchronizing Error signal output enable bit (special mode 5) 0: Not output 1: Output	RW

NOTES:
1. Set the SCLKSTPB/UiERE bit after setting the SMD2 to SMD0 bits in the UiMR register.
2. The UiLCH bit is enabled when the SMD2 to SMD0 bits are set to "001_2" (clock synchronous serial I/O mode), "100_2"(UART mode, 7-bit transfer data), or "101_2" (UART mode, 8-bit transfer data). Set this bit to "0" when the SMD2 to SMD0 bits are set to "010_2" (I^2C mode) or "110_2"(UART mode, 9-bit transfer data)

UARTi Special Mode Register (i=0 to 4)



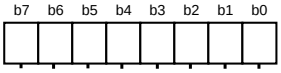
Symbol	Address	After Reset
U0SMR to U4SMR	0367_{16}, $02E7_{16}$, 0337_{16}, 0327_{16}, $02F7_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
IICM	I^2C Mode Select Bit	0: Except I^2C mode 1: I^2C mode	RW
ABC	Arbitration Lost Detect Flag Control Bit	0: Update per bit 1: Update per byte	RW
BBS	Bus Busy Flag	0: Stop condition detected 1: Start condition detected (Busy)	RW(1)
LSYN	SCLL Sync Output Enable Bit	0: Disabled 1: Enabled	RW
ABSCS	Bus Conflict Detect Sampling Clock Select Bit	0: Rising edge of transfer clock 1: Timer Aj underflow(2)	RW
ACSE	Auto Clear Function Select Bit for Transmit Enable Bit	0: No auto clear function 1: Auto clear at bus conflict	RW
SSS	Transmit Start Condition Select Bit	0: Not related to RxDi 1: Synchronized with RxDi	RW
SCLKDIV	Clock Divide Synchronous Bit	(Note 3)	RW

NOTES:
1. The BBS bit is set to "0" by program. It is unchanged if set to "1".
2. UART0: timer A3 underflow signal, UART1: timer A4 underflow signal, UART2: timer A0 underflow signal, UART3: timer A3 underflow signal, UART4: timer A4 underflow signal.
3. Refer to notes for the SU1HIM bit in the UiSMR2 register.

Figure 16.5 U0C1 to U4C1 Registers and U0SMR to U4SMR Registers

UARTi Special Mode Register 2 (i=0 to 4)



Symbol	Address	After Reset
U0SMR2 to U4SMR2	0366_{16}, $02E6_{16}$, 0336_{16}, 0326_{16}, $02F6_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
IICM2	I^2C Mode Select Bit 2	(Note 1)	RW
CSC	Clock Synchronous Bit	0: Disabled 1: Enabled	RW
SWC	SCL Wait Output Bit	0: Disabled 1: Enabled	RW
ALS	SDA Output Stop Bit	0: Disabled 1: Enabled	RW
STC	UARTi Initialize Bit	0: Disabled 1: Enabled	RW
SWC2	SCL Wait Output Bit 2	0: Transfer clock 1: "L" output	RW
SDHI	SDA Output Inhibit Bit	0: Output 1: No output (high-impedance)	RW
SU1HIM	External Clock Synchronous Enable Bit	(Note 2)	RW

NOTES:
1. Refer to 16.3 Special mode 1 (I^2C Mode).
2. The external clock synchronous function can be selected by combining the SU1HIM bit and the SCLKDIV bit in the UiSMR register.

SCLKDIV bit in the UiSMR Register	SU1HIM bit in the UiSMR2 Register	External Clock Synchronous Function Selection
0	0	No synchronization
0	1	Same division as the external clock
1	0 or 1	External clock divided by 2

Figure 16.6 U0SMR2 to U4SMR2 Registers

UARTi Special Mode Register 3 (i=0 to 4)

b7	b6	b5	b4	b3	b2	b1	b0

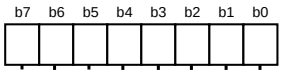
Symbol	Address	After Reset
U0SMR3 to U4SMR3	0365_{16}, $02E5_{16}$, 0335_{16}, 0325_{16}, $02F5_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SSE	$\overline{SS}$ Pin Function Enable Bit(1)	0: Disables $\overline{SS}$ pin function 1: Enables $\overline{SS}$ pin function	RW
CKPH	Clock-Phase Set Bit	0: No clock delay 1: Clock delay	RW
DINC	Serial Input Port Set Bit	0: Selects the TxDi and RxDi pins (master mode) 1: Selects the STxDi and SRxDi pins (slave mode)	RW
NODC	Clock Output Select Bit	0: CMOS output 1: N-channel open drain output	RW
ERR	Fault Error Flag(2)	0: No error 1: Error	RW
DL0	SDAi Digital Delay Time Set Bit(3, 4)	b7 b6 b5 000 : No delay 001 : 1-to-2 cycles of BRG count source 010 : 2-to-3 cycles of BRG count source 011 : 3-to-4 cycles of BRG count source 100 : 4-to-5 cycles of BRG count source 101 : 5-to-6 cycles of BRG count source 110 : 6-to-7 cycles of BRG count source 111 : 7-to-8 cycles of BRG count source	RW
DL1			RW
DL2			RW

NOTES:
1. Set the $\overline{SS}$ pin after the CRD bit in the UiC0 register is set to "1" ($\overline{CTS}/\overline{RTS}$ function disabled).
2. The ERR bit is set to "0" by program. It is unchanged if set to "1".
3. Digital delay is generated from a SDAi output by the DL2 to DL0 bits in I^2C mode. Set these bits to "000_2" (no delay) except in the I^2C mode.
4. When the external clock is selected, approximately 100ns delay is added.

Figure 16.7 U0SMR3 to U4SMR3 Registers

UARTi Special Mode Register 4 (i=0 to 4)



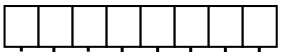
Symbol	Address	After Reset
U0SMR4 to U04SMR4	0364_{16}, $02E4_{16}$, 0334_{16}, 0324_{16}, $02F4_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
STAREQ	Start Condition Generate Bit(1)	0: Clear 1: Start	RW
RSTAREQ	Restart Condition Generate Bit(1)	0: Clear 1: Start	RW
STPREQ	Stop Condition Generate Bit(1)	0: Clear 1: Start	RW
STSPSEL	SCL, SDA Output Select Bit	0: Selects the serial I/O circuit 1: Selects the start/stop condition generation circuit	RW
ACKD	ACK Data Bit	0: ACK 1: NACK	RW
ACKC	ACK Data Output Enable Bit	0: Serial I/O data output 1: ACK data output	RW
SCLHI	SCL Output Stop Enable Bit	0: Disabled 1: Enabled	RW
SWC9	SCL Wait Output Bit 3	0: SCL "L" hold disabled 1: SCL "L" hold enabled	RW

NOTES:
1. When each condition is generated, the STAREQ, RSTAREQ or STPREQ bit is set to "0". When a condition generation is incomplete, the bit remains unchanged as "1".

Figure 16.8 U0SMR4 to U4SMR4 Registers

External Interrupt Request Cause Select Register



Symbol: IFSR
Address: $031F_{16}$
After Reset: 00_{16}

Bit Symbol	Bit Name	Function	RW
IFSR0	INT0 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR1	INT1 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR2	INT2 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR3	INT3 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR4	INT4 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR5	INT5 Interrupt Polarity Select Bit(1)	0 : One edge 1 : Both edges	RW
IFSR6	UART0, 3 Interrupt Cause Select Bit	0 : UART3 bus conflict, start condition detect, stop condition detect, fault error detect 1 : UART0 bus conflict, start condition detect, stop condition detect, fault error detect	RW
IFSR7	UART1, 4 Interrupt Cause Select Bit	0 : UART4 bus conflict, start condition detect, stop condition detect, fault error detect 1 : UART1 bus conflict, start condition detect, stop condition detect, fault error detect	RW

NOTES:
1.When level sense is selected, set this bit to "0".
When both edges are selected, set the POL bit in the INTilC register (i = 0 to 5) to "0" (falling edge).

Figure 16.9 IFSR Register

16.1 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received with the transfer clock. Table 16.1 lists specifications of clock synchronous serial I/O mode. Table 16.2 lists registers to be used and settings. Tables 16.3 to 16.5 list pin settings. When UARTi (i=0 to 4) operation mode is selected, the TxDi pin outputs an "H" signal before transfer starts (the TxDi pin is in a high-impedance state when the N-channel open drain output is selected). Figure 16.10 shows transmit and receive timings in clock synchronous serial I/O mode.

Table 16.1 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer Data Format	• Transfer data : 8 bits long
Transfer Clock	• The CKDIR bit in the UiMR register (i=0 to 4) is set to "0" (internal clock selected): $\frac{f_j}{2(m+1)}$ f_j=f_1, f_8, f_{2n}(1) m :setting value of the UiBRG register 00_{16} to FF_{16}. • The CKDIR bit is set to "1" (external clock selected) : an input from the CLKi pin
Transmit/Receive Control	• Selected from the $\overline{CTS}$ function, $\overline{RTS}$ function or $\overline{CTS}$/$\overline{RTS}$ function disabled
Transmit Start Condition	• To start transmitting, the following requirements must be met(2): - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register) - Apply an "L" signal to the $\overline{CTSi}$ pin when the $\overline{CTS}$ function is selected
Receive Start Condition	• To start receiving, the following requirements must be met(2): - Set the RE bit in the UiC1 register to "1" (receive enable) - Set the TE bit to "1" (transmit enable) - Set the TI bit to "0" (data in the UiTB register)
Interrupt Request Generation Timing	• Transmit interrupt timing can be selected from the followings: - The UiIRS bit in the UiC1 register is set to "0" (no data in the transmit buffer) : when data is transferred from the UiTB register to the UARTi transmit register (transfer started) - The UiIRS bit is set to "1" (transmission completed) : when a data transfer from the UARTi transmit register is completed • Receive interrupt timing When data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detect	• Overrun error(3) This error occurs when the seventh bit of the next received data is read before reading the UiRB register
Selectable Function	• CLK polarity Transferred data is output and input on either the rising edge or falling edge of the transfer clock • LSB first/MSB first Data is transmitted/received in either bit 0 or in bit 7 • Continuous receive mode Data can be received simultaneously by reading the UiRB register • Serial data logic inverse This function inverses transmitted/received data logically

NOTES:

1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).
2. To start transmission/reception when selecting the external clock, these conditions must be met after the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and data is received on the rising edge) and the CLKi pin is held high ("H"), or when the CKPOL bit is set to "1" (Data is transmitted on the rising edge of the transfer clock and data is received on the falling edge) and the CLKi pin is held low ("L").
3. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).

Table 16.2 Registers to be Used and Setting Value in Clock Synchronous Serial I/O Mode

Register	Bit	Function
UiTB	0 to 7	Set transmit data
UiRB	0 to 7	Received data can be read
	OER	Overrun error flag
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to "001_2"
	CKDIR	Select the internal clock or external clock
	IOPOL	Set to "0"
UiC0	CLK1 to CLK0	Select count source for the UiBRG register
	CRS	Select $\overline{CTS}$ or $\overline{RTS}$ when using either
	TXEPT	Transmit register empty flag
	CRD	Enables or disables the $\overline{CTS}$ or $\overline{RTS}$ function
	NCH	Select output format of the TxDi pin
	CKPOL	Select transmit clock polarity
	UFORM	Select either LSB first or MSB first
UiC1	TE	Set to "1" to enable data transmission and reception
	TI	Transmit buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select how the UARTi transmit interrupt is generated
	UiRRM	Set to "1" when using continuous receive mode
	UiLCH	Set to "1" when using data logic inverse
	SCLKSTPB	Set to "0"
UiSMR	0 to 7	Set to "00_{16}"
UiSMR2	0 to 7	Set to "00_{16}"
UiSMR3	0 to 2	Set to "000_2"
	NODC	Select clock output format
	4 to 7	Set to "0000_2"
UiSMR4	0 to 7	Set to "00_{16}"

i=0 to 4

Table 16.3 Pin Settings in Clock Synchronous Serial I/O Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	$\overline{CTS0}$ input	PS0_0=0	-	PD6_0=0
	$\overline{RTS0}$ output	PS0_0=1	-	-
P61	CLK0 input	PS0_1=0	-	PD6_1=0
	CLK0 output	PS0_1=1	-	-
P62	RxD0 input	PS0_2=0	-	PD6_2=0
P63	TxD0 output	PS0_3=1	-	-
P64	$\overline{CTS1}$ input	PS0_4=0	-	PD6_4=0
	$\overline{RTS1}$ output	PS0_4=1	PSL0_4=0	-
P65	CLK1 input	PS0_5=0	-	PD6_5=0
	CLK1 output	PS0_5=1	-	-
P66	RxD1 input	PS0_6=0	-	PD6_6=0
P67	TxD1 output	PS0_7=1	-	-

Table 16.4 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70(1)	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	-
P71(1)	RxD2 input	PS1_1=0	-	-	PD7_1=0
P72	CLK2 input	PS1_2=0	-	-	PD7_2=0
	CLK2 output	PS1_2=1	PSL1_2=0	PSC_2=0	-
P73	$\overline{CTS2}$ input	PS1_3=0	-	-	PD7_3=0
	$\overline{RTS2}$ output	PS1_3=1	PSL1_3=0	PSC_3=0	-

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

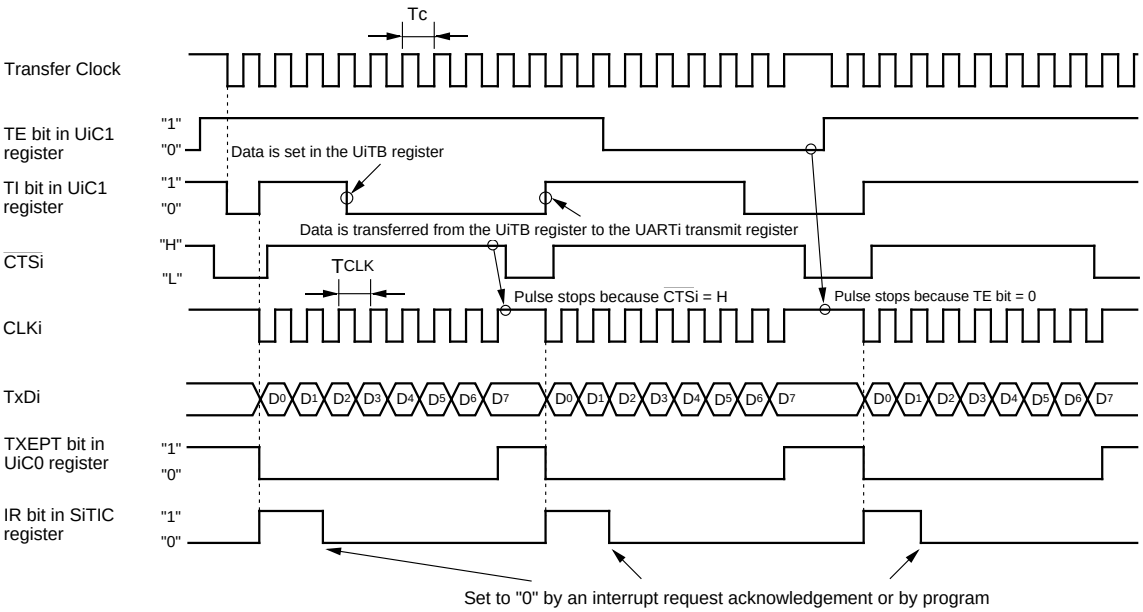
Table 16.5 Pin Settings (3)

Port	Function	Setting		
		PS3 Register(1)	PSL3 Register	PD9 Register(1)
P90	CLK3 input	PS3_0=0	-	PD9_0=0
	CLK3 output	PS3_0=1	-	-
P91	RxD3 input	PS3_1=0	-	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	-
P93	$\overline{CTS3}$ input	PS3_3=0	PSL3_3=0	PD9_3=0
	$\overline{RTS3}$ output	PS3_3=1	-	-
P94	$\overline{CTS4}$ input	PS3_4=0	PSL3_4=0	PD9_4=0
	$\overline{RTS4}$ output	PS3_4=1	-	-
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
	CLK4 output	PS3_5=1	-	-
P96	TxD4 output	PS3_6=1	-	-
P97	RxD4 input	PS3_7=0	-	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

(1) Transmit Timing (Internal clock selected)



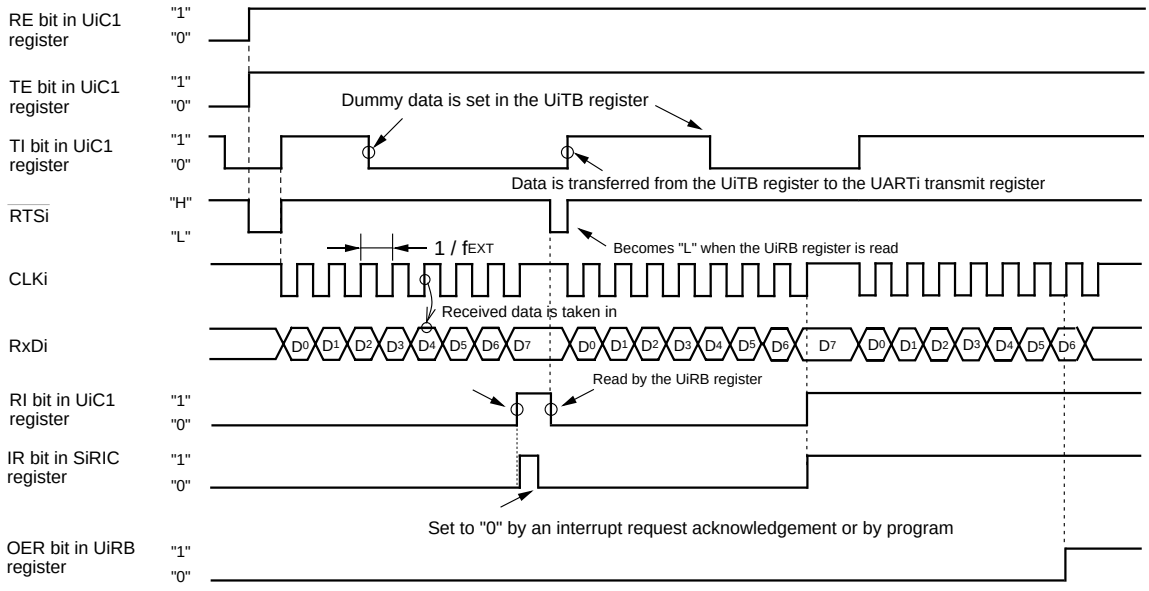
The above applies to the following settings:
- The CKDIR bit in the UiMR register is set to "0" (internal clock selected)
- The CRD bit in the UiC0 register is set to "0" (RTS/CTS function enabled)
  The CRS bit is set to "0" (CTS function selected)
- The CKPOL bit the in UiC0 register is set to "0" (data transmitted on the falling edge of the transfer clock)
- The UiIRS bit in the UiC1 register is set to "0" (no data in the UiTB register)

$T_C = 2(m+1)/fj$

fj : Count source frequency set in the UiBRG register (f_1, f_8, f_{2n}(1))
m : Setting value of the UiBRG register
i = 0 to 4

NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

(2) Receive Timing (External clock selected)



The above applies to the following settings:
- The CKDIR bit in the UiMR register is set to "1" (external clock selected)
- The CRD bit in the UiC0 register is set to "0" (RTS/CTS function enabled)
  The CRS bit is set to "1" (RTS function selected)
- The CKPOL bit in the UiC0 register is set to "0"
  (Data is received on the rising edge of the transfer clock)

fEXT: External clock frequency i=0 to 4

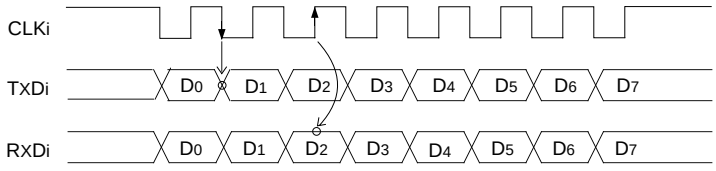
Meet the following conditions while "H" is applied to the CLKi pin before receiving data:
- Set the TE bit in the UiC1 register to "1" (transmit enable)
- Set the RE bit in the UiC1 register to "1" (receive enable)
- Write dummy data to the UiTB register

Figure 16.10 Transmit and Receive Operation

16.1.1 Selecting CLK Polarity

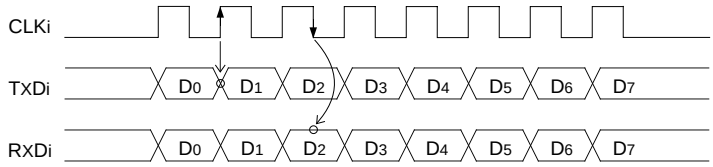
As shown in Figure 16.11, the CKPOL bit in the UiC0 register (i=0 to 4) determines the polarity of the transfer clock.

(1) When the CKPOL bit in the UiC0 register (i=0 to 4) is set to "0"
(Data is transmitted on the falling edge of the transfer clock and data is received on the rising edge)



NOTES:
1. The CLKi pin is held high ("H") when no data is transferred.
2. The above applies when the UFORM bit in the UiC0 register is set to "0" (LSB first) and the UiLCH bit in the UiC1 register is set to "0" (not inversed).

(2) When the CKPOL bit in the UiC0 register is set to "1"
(Data is transmitted on the rising edge of the transfer clock and data is received on the falling edge)



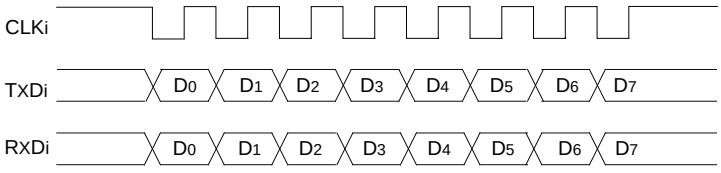
NOTES:
3. The CLKi pin is held low ("L") when no data is transferred.
4. The above applies when the UFORM bit in the UiC0 register is set to "0" (LSB first) and the UiLCH bit in the UiC1 register is set to "0" (not inversed).

Figure 16.11 Transfer Clock Polarity

16.1.2 Selecting LSB First/MSB First

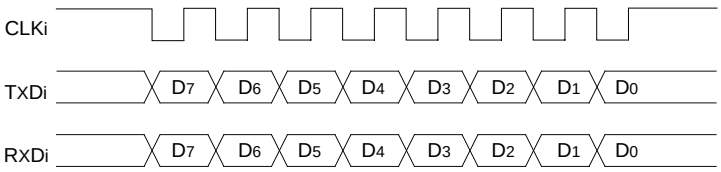
As shown in Figure 16.12, the UFORM bit in the UiC0 register (i=0 to 4) determines a data transfer format.

(1) When the UFORM bit in the UiC0 register (i=0 to 4) is set to "0"
(LSB first)



NOTES:
1. The above applies when the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and received on the rising edge) and the UiLCH bit in the UiC1 register is set to "0" (not inversed).

(2) When the UFORM bit in the UiC0 register is set to "1" (MSB first)



NOTES:
2. The above applies when the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and received on the rising edge) and the UiLCH bit in the UiC1 register is set to "0" (not inversed).

Figure 16.12 Transfer Format

16.1.3 Continuous Receive Mode

When the UiRRM bit in the UiC1 register (i=0 to 4) is set to "1" (continuous receive mode), the TI bit is set to "0" (data in the UiTB register) by reading the UiRB register. When the UiRRM bit is set to "1", do not set dummy data in the UiTB register by program.

16.1.4 Serial Data Logic Inverse Function

When the UiLCH bit in the UiC1 register is set to "1" (inverse), data logic written in the UiTB register is inversed when transmitted. The inversed receive data logic can be read by reading the UiRB register. Figure 16.13 shows a switching example of the serial data logic.

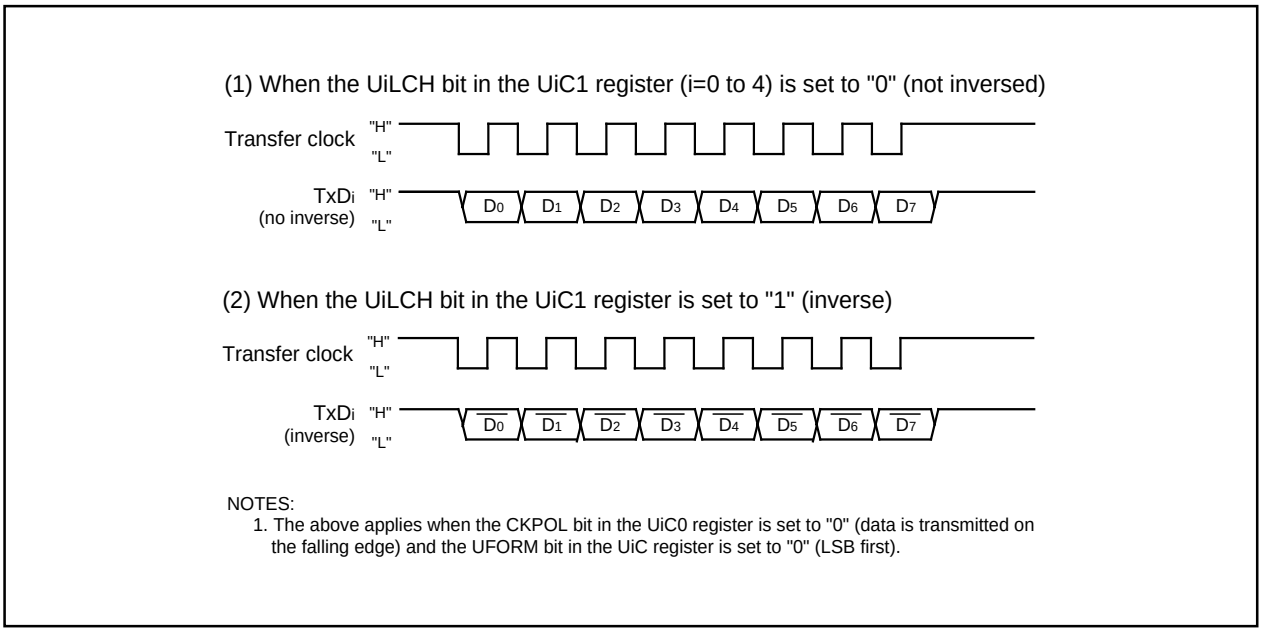


Figure 16.13 Serial Data Logic Switching

16.2 Clock Asynchronous Serial I/O (UART) Mode

In UART mode, data is transmitted and received after setting a desired bit rate and data transfer format. Table 16.6 lists specifications of UART mode.

Table 16.6 UART Mode Specifications

Item	Specification
Transfer Data Format	• Character bit (transfer data) : selected from 7 bits, 8 bits, or 9 bits • Start bit: 1 bit • Parity bit: selected from odd, even, or none • Stop bit: selected from 1 bit or 2 bits
Transfer Clock	• The CKDIR bit in the UiMR register is set to "0" (internal clock selected) : $f_j/16(m+1)$ $f_j = f_1, f_8, f_{2n}$(1) m: setting value of the UiBRG register 00_{16} to FF_{16} • The CKDIR bit is set to "1" (external clock selected) : $f_{EXT}/16(m+1)$ f_{EXT}: clock applied to the CLKi pin
Transmit/Receive Control	• Select from $\overline{CTS}$ function, $\overline{RTS}$ function or $\overline{CTS}/\overline{RTS}$ function disabled
Transmit Start Condition	• To start transmitting, the following requirements must be met: - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register) - Apply an "L" signal to the $\overline{CTS}$i pin when the $\overline{CTS}$ function is selected
Receive Start Condition	• To start receiving, the following requirements must be met: - Set the RE bit in the UiC1 register to "1" (receive enable) - The start bit is detected
Interrupt Request Generation Timing	• Transmit interrupt timing can be selected from the followings: - The UiIRS bit in the UiC1 register is set to "0" (no data in the transmit buffer) : when data is transferred from the UiTB register to the UARTi transmit register (transfer started) - The UiIRS bit is set to "1" (transmission completed) : when data transmission from the UARTi transfer register is completed • Receive interrupt timing when data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detect	• Overrun error(2) This error occurs when the bit before the last stop bit of the next received data is read prior to reading the UiRB register (the first stop bit when selecting 2 stop bits) • Framing error This error occurs when the number of stop bits set is not detected • Parity error When parity is enabled, this error occurs when the number of "1" in parity and character bits does not match the number of "1" set • Error sum flag This flag is set to "1" when any of an overrun, framing or parity errors occur
Selectable Function	• LSB first or MSB first Data is transmitted/received in either bit 0 or in bit 7 •Serial data logic inverse Logic values of data to be transmitted and received data are inversed. The start bit and stop bit are not inversed •TxD, RxD I/O polarity switching TxD pin output and RxD pin input are inversed

NOTES:

1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).
2. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register remains unchanged as "1" (interrupt requested).

Table 16.7 lists registers to be used and settings. Tables 16.8 to 16.10 list pin settings. When UARTi (i=0 to 4) operation mode is selected, the TxDi pin outputs an "H" signal before transfer is started (the TxDi pin is in a high-impedance state when the N-channel open drain output is selected). Figure 16.14 shows an example of a transmit operation in UART mode. Figure 16.15 shows an example of a receive operation in UART mode.

Table 16.7 Registers to be Used and Settings in UART

Register	Bit	Function
UiTB	0 to 8	Set transmit data(1)
UiRB	0 to 8	Received data can be read(1)
	OER, FER, PER, SUM	Error flags
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to "100_2" when transfer data is 7 bits long Set to "101_2" when transfer data is 8 bits long Set to "110_2" when transfer data is 9 bits long
	CKDIR	Select the internal clock or external clock
	STPS	Select stop bit length
	PRY, PRYE	Select parity enable or disable, odd or even
	IOPOL	Select TxD / RxD I/O polarity
UiC0	CLK0, CLK1	Select count source for the UiBRG register
	CRS	Select either $\overline{CTS}$ or $\overline{RTS}$ when using either
	TXEPT	Transfer register empty flag
	CRD	Enables or disables the $\overline{CTS}$ or $\overline{RTS}$ function
	NCH	Select output format of the TxDi pin
	CKPOL	Set to "0"
	UFORM	Select the LSB first or MSB first when a transfer data is 8 bits long Set to "0" when transfer data is 7 bits or 9 bits long
UiC1	TE	Set to "1" to enable data transmission
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select how the UARTi transmit interrupt is generated
	UiRRM	Set to "0"
	UiLCH	Select whether or not data logic is inversed when transfer data length is 7 or 8 bits. Set to "0" when transfer data length is 9 bits.
	UiERE	Set to either "0" or "1"
UiSMR	0 to 7	Set to "00_{16}"
UiSMR2	0 to 7	Set to "00_{16}"
UiSMR3	0 to 7	Set to "00_{16}"
UiSMR4	0 to 7	Set to "00_{16}"

NOTES:

1. Use bits 0 to 6 when transfer data is 7 bits long, bits 0 to 7 when 8 bits long, bits 0 to 8 when 9 bits long.

Table 16.8 Pin Settings in UART (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	$\overline{CTS0}$ input	PS0_0=0	–	PD6_0=0
	$\overline{RTS0}$ output	PS0_0=1	–	–
P61	CLK0 input	PS0_1=0	–	PD6_1=0
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P64	$\overline{CTS1}$ input	PS0_4=0	–	PD6_4=0
	$\overline{RTS1}$ output	PS0_4=1	PSL0_4=0	–
P65	CLK1 input	PS0_5=0	–	PD6_5=0
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

Table 16.9 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70(1)	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71(1)	RxD2 input	PS1_1=0	–	–	PD7_1=0
P72	CLK2 input	PS1_2=0	–	–	PD7_2=0
P73	$\overline{CTS2}$ input	PS1_3=0	–	–	PD7_3=0
	$\overline{RTS2}$ output	PS1_3=1	PSL1_3=0	PSC_3=0	–

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

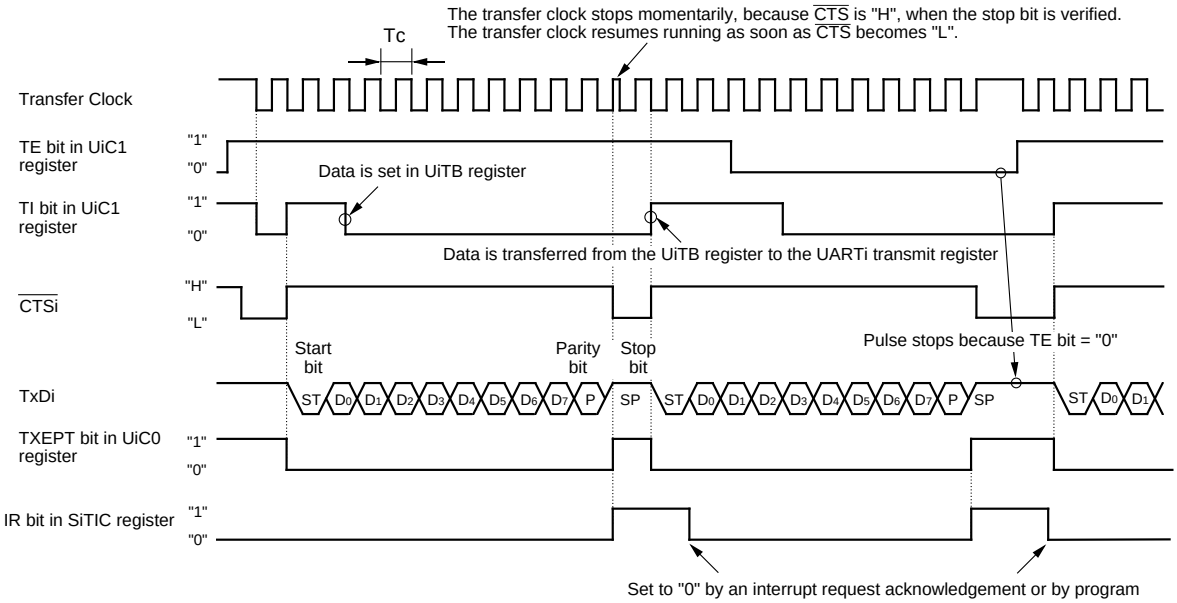
Table 16.10 Pin Settings (3)

Port	Function	Setting		
		PS3 Register(1)	PSL3 Register	PD9 Register(1)
P90	CLK3 input	PS3_0=0	–	PD9_0=0
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P93	$\overline{CTS3}$ input	PS3_3=0	PSL3_3=0	PD9_3=0
	$\overline{RTS3}$ output	PS3_3=1	–	–
P94	$\overline{CTS4}$ input	PS3_4=0	PSL3_4=0	PD9_4=0
	$\overline{RTS4}$ output	PS3_4=1	–	–
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers set immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

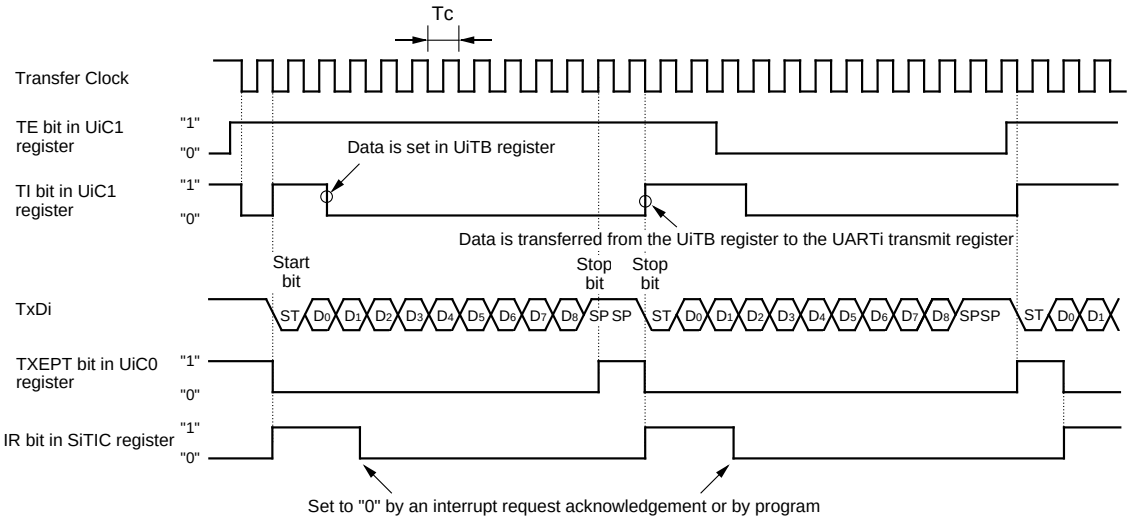
(1) 8-bit Data Transmission Timing (with a parity and 1 stop bit)



i=0 to 4
The above timing applies to the following settings :
- The PRYE bit in the UiMR register is set to "1" (parity enabled)
- The STPS bit in the UiMR register is set to "0" (1 stop bit)
- The CRD bit in the UiC0 register is set to "0" and the CRS bit is set to "0" (CTS function selected)
- The UiIRS bit in the UiC1 register is set to "1" (transmission completed)

Tc = 16 (m + 1) / fj or 16 (m + 1) / fEXT
fj : count source frequency set in the UiBRG register (f1, f8, f2n(1))
fEXT : count source frequency set in the UiBRG register (external clock)
m : setting value of the UiBRG register
NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

(2) 9-bit Data Transmit Timing (with no parity and 2 stop bits)



i=0 to 4
The above timing applies to the following settings :
- The PRYE bit in the UiMR register is set to "0" (parity disabled)
- The STPS bit in the UiMR register is set to "1" (2 stop bits)
- The CRD bit in the UiC0 register is set to "1" (CTS function disabled)
- The UiIRS bit in the UiC1 register is set to "0" (no data in the transmit buffer)

Tc = 16 (m + 1) / fj or 16 (m + 1) / fEXT
fj : count source frequency set in the UiBRG register (f1, f8, f2n(1))
fEXT : count source frequency set in the UiBRG register (external clock)
m : setting value of the UiBRG register
NOTES:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Figure 16.14 Transmit Operation

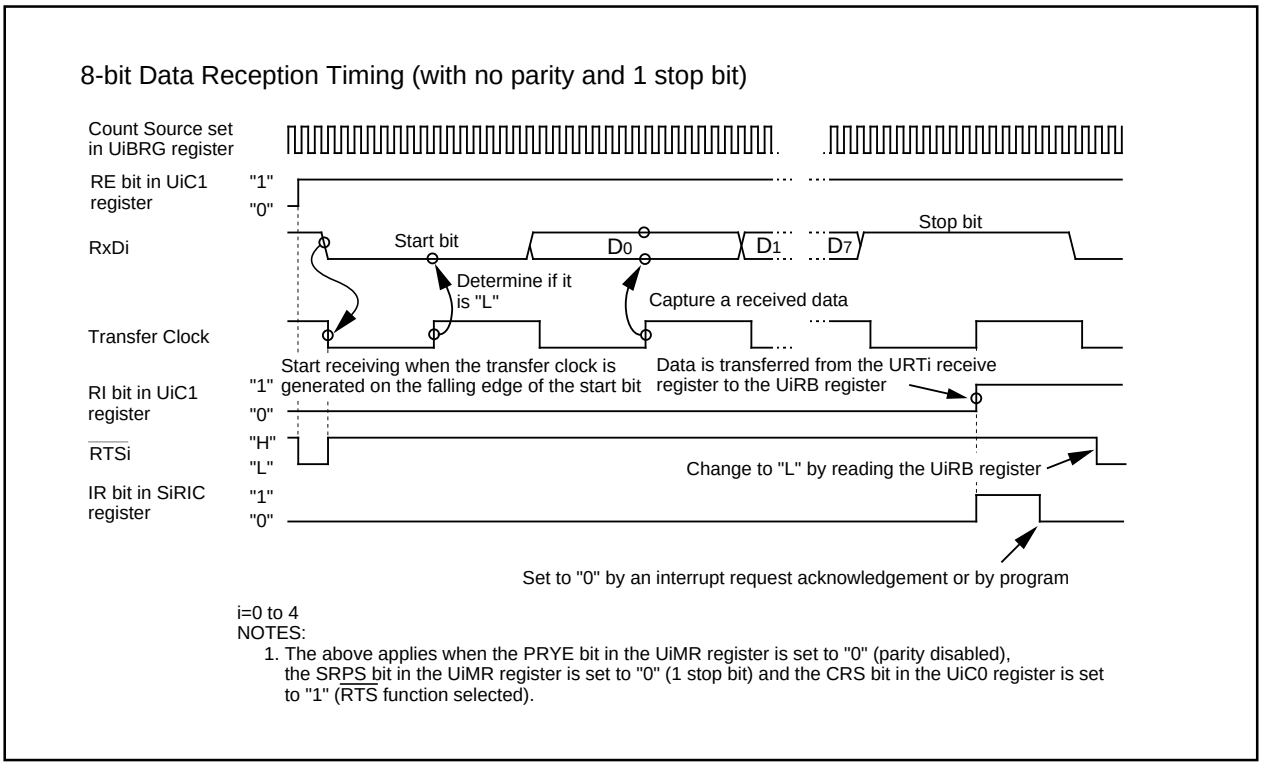


Figure 16.15 Receive Operation

16.2.1 LSB First / MSB First Select Function

As shown in Figure 16.16, the UFORM bit in the UiC0 register (i=0 to 4) determines data transfer format. This function is available for 8-bit transfer data.

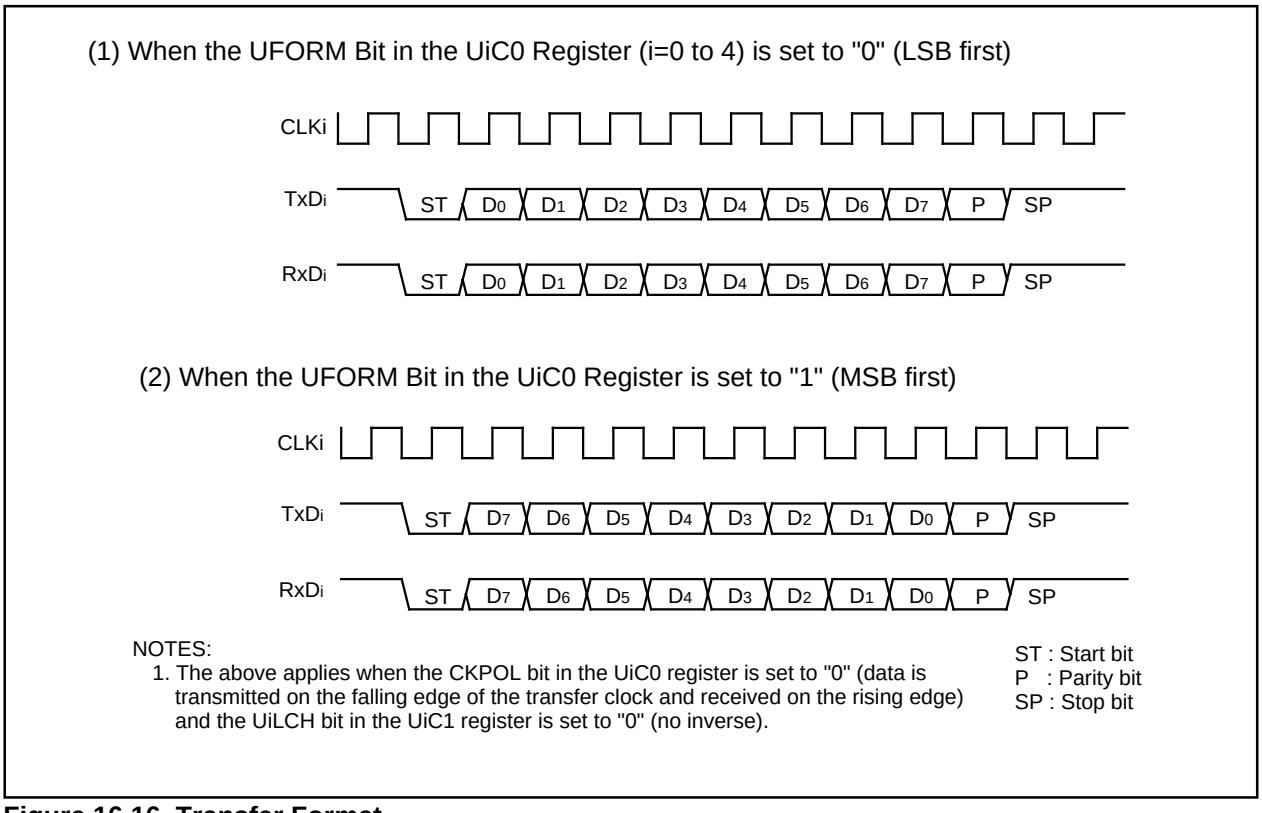


Figure 16.16 Transfer Format

16.2.2 Serial Data Logic Inverse Function

After the UiLCH bit in the UiC1 register is set to "1", data logic is inversed when writing to the UiTB register (i=0 to 4) and reading from the UiRB register. Figure 16.17 shows a serial data logic.

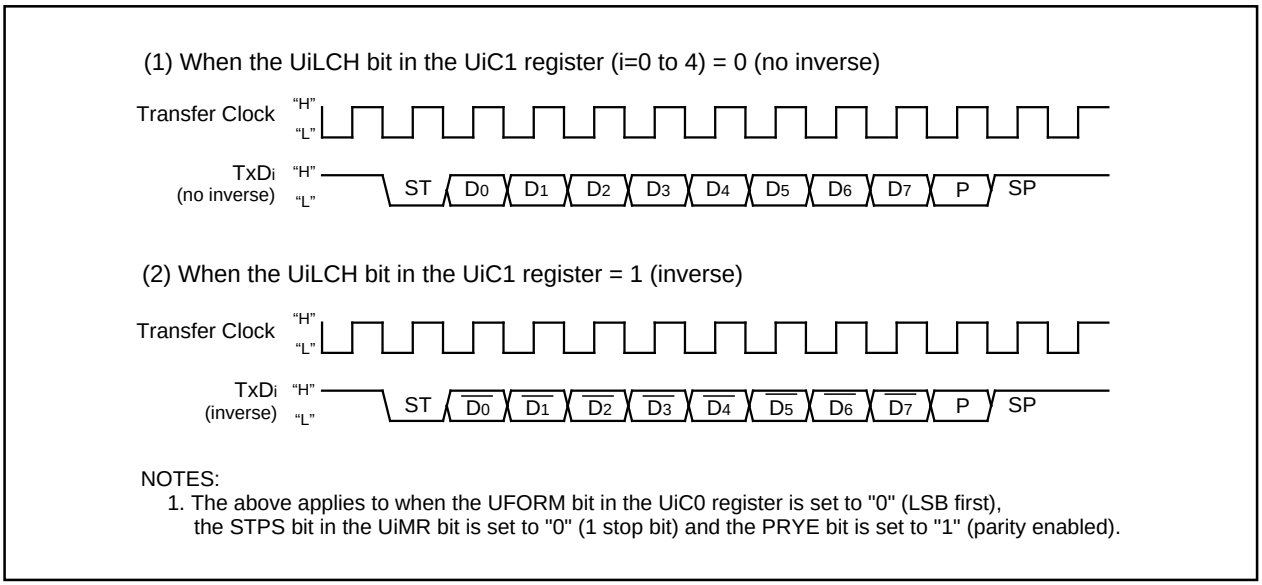


Figure 16.17 Serial Data Logic Inverse

16.2.3 TxD and RxD I/O Polarity Inverse Function

TxD pin output and RxD pin input are inversed. All I/O data level, including the start bit, stop bit and parity bit, are inversed. Figure 16.18 shows TxD and RxD I/O polarity inverse.

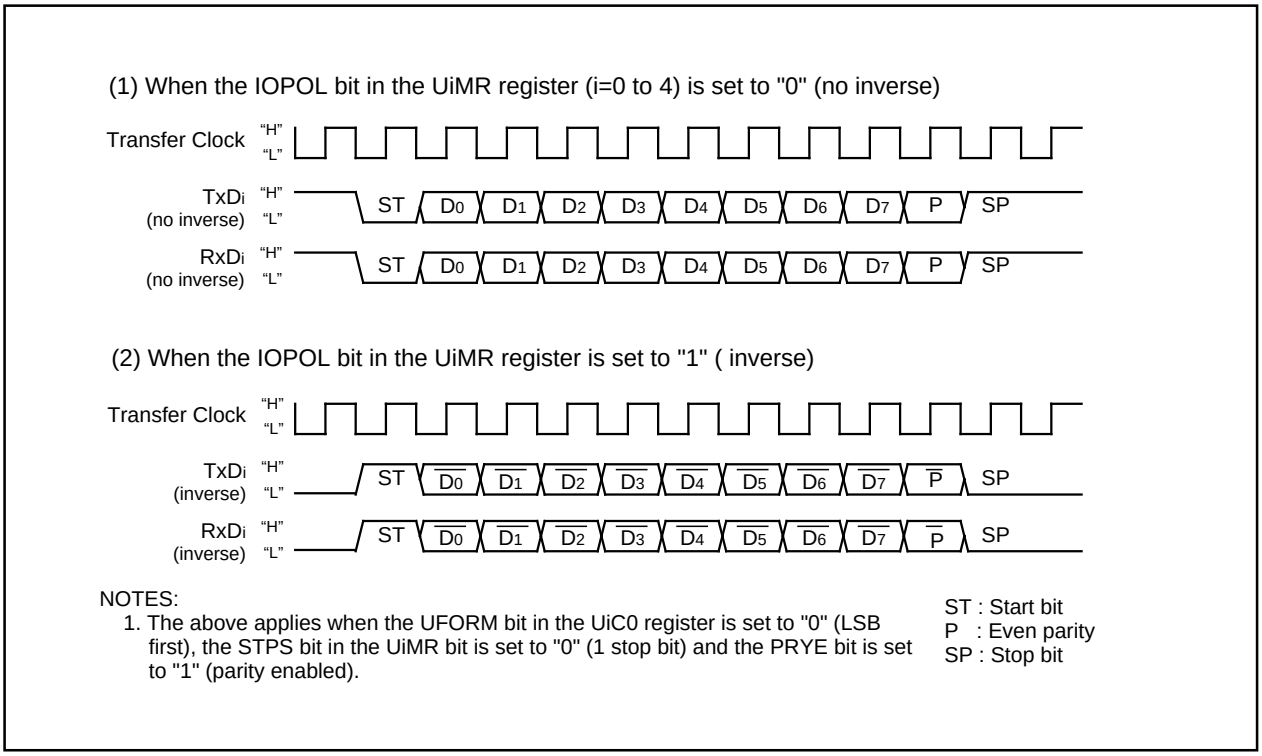


Figure 16.18 TxD, RxD I/O Polarity Reverse Function

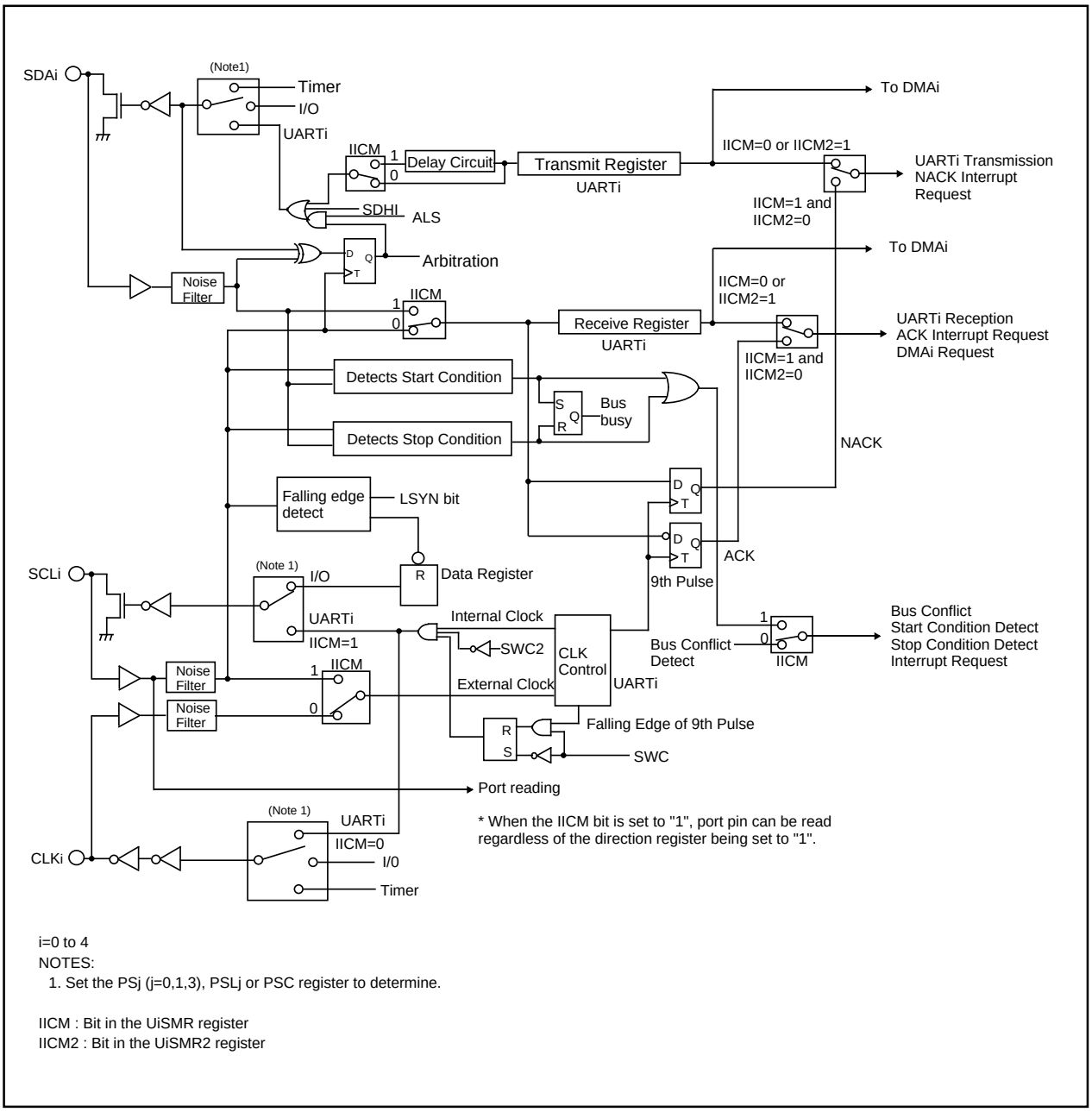
16.3 Special Mode 1 (I²C Mode)

I²C mode is a mode to communicate with external devices with a simplified I²C . Table 16.11 lists specifications of I²C mode. Table 16.12 lists registers to be used and settings, Table 16.13 lists each function. Figure 16.19 shows a block diagram of I²C mode. Figure 16.20 shows timings for transfer to the UiRB register and interrupts. Tables 16.14 to 16.16 list pin settings.

As shown in Table 16.13, I²C mode is entered when the SMD2 to SMD0 bits in the UiMR register is set to "010₂" and the IICM bit in the UiMR register is set to "1". SDAi output changes after SCLi becomes low and stabilizes due to a SDAi output via the delay circuit.

Table 16.11 I²C Mode Specifications

Item	Specifications
Interrupt	Start condition detect, stop condition detect, no acknowledgment detect, acknowledgment detect
Selectable Function	• Arbitration lost The update timing of the ABT bit in the UiRB register can be selected. Refer to **16.3.3 Arbitration**. • SDAi digital delay Selected from no digital delay or 2 to 8 cycle delay of the count source of BRG. Refer to **16.3.5 SDA Output**. • Clock phase setting Selected from clock delay or no clock delay. Refer to **16.3.4 Transfer Clock**.



i=0 to 4
NOTES:
1. Set the PSj (j=0,1,3), PSLj or PSC register to determine.

IICM : Bit in the UiSMR register
IICM2 : Bit in the UiSMR2 register

Figure 16.19 I²C Mode Block Diagram

Table 16.12 Registers To Be Used and Settings (I²C Mode)

Register	Bit	Function	
		Master	Slave
UiTB	0 to 7	Set transmit data	
UiRB	0 to 7	Received data can be read	
	8	ACK or NACK bit can be read	
	ABT	Arbitration lost detect flag	Disabled
	OER	Overrun error flag	
UiBRG	0 to 7	Set bit rate	Disabled
UiMR	SMD2 to SMD0	Set to "010$_2$"	
	CKDIR	Set to "0"	Set to "1"
	IOPOL	Set to "0"	
UiC0	CLK1 to CLK0	Select count source of the UiBRG register	Disabled
	CRS	Disabled because CRD = 1	
	TXEPT	Transfer register empty flag	
	CRD, NCH	Set to "1"	
	CKPOL	Set to "0"	
	UFORM	Set to "1"	
UiC1	TE	Set to "1" to enable data transmission	
	TI	Transfer buffer empty flag	
	RE	Set to "1" to enable data reception	
	RI	Reception complete flag	
	UiRRM, UiLCH, UiERE	Set to "0"	
UiSMR	IICM	Set to "1"	
	ABC	Select an arbitration lost detect timing	Disabled
	BBS	Bus busy flag	
	3 to 7	Set to "00000$_2$"	
UiSMR2	IICM2	See Table 16.13	
	CSC	Set to "1" to enable clock synchronization	Set to "0"
	SWC	Set to "1" to output fixed "L" from the SDAi on the falling edge of the ninth bit of the transfer clock	
	ALS	Set to "1" to terminate SDA output when detecting the arbitration lost	Not used. Set to "0"
	STC	Not used. Set to "0"	Set to "1" to reset UARTi by detecting the start condition
	SWC2	Set to "1" to forcibly output an "L" signal from SCL	
	SDHI	Set to "1" to disable SDA output	
	SU1HIM	Set to "0"	
UiSMR3	SSE	Set to "0"	
	CKPH	See Table 16.13.	
	DINC, NODC, ERR	Set to "0"	
	DL2 to DL0	Set digital delay value	
UiSMR4	STAREQ	Set to "1" when generating a start condition	Not used. Set to "0"
	RSTAREQ	Set to "1" when generating a restart condition	
	STPREQ	Set to "1" when generating a stop condition	
	STSPSEL	Set to "1" when using a condition generating function	
	ACKD	Select ACK or NACK	
	ACKC	Set to "1" to output ACK data	
	SCLHI	Set to "1" to enable SCL output stop when detecting stop condition	Not used. Set to "0"
	SWC9	Not used. Set to "0"	Set to "1" to output fixed "L" from SCLi on the falling edge of the ninth bit of the transfer clock
IFSR	IFSR6, IFSR7	Set to "1"	

i=0 to 4

Table 16.13 I²C Mode Functions

Function	Clock Synchronous Serial I/O Mode (SMD2 to SMD0=001₂, IICM=0)	I²C Mode (SMD2 to SMD0=010₂, IICM=1)			
		IICM2=0 (NACK/ACK interrupt)		IICM2=1 (UART transmit / UART receive interrupt)	
		CKPH=0 (No clock delay)	CKPH=1 (Clock delay)	CKPH=0 (No clock delay)	CKPH=1 (Clock delay)
Interrupt Numbers 39 to 41 Generated(1) (See Figure 16.20)	-	Start condition or stop condition detect (See Table 16.17)			
Interrupt Number 17, 19, 33, 35 and 37 Generated(1) (See Figure 16.20)	UARTi Transmission - Transmission started or completed (selected by the UiIRS register)	No Acknowlegement Detect (NACK) - Rising edge of 9th bit of SCLi		UARTi Transmission - Rising edge of 9th bit of SCLi	UARTi Transmission - Next falling edge after the 9th bit of SCLi
Interrupt Numbers 18, 20, 34, 36 and 38 Generated(1) (See Figure 16.20)	UARTi Reception - Receiving at 8th bit CKPOL=0(rising edge) CKPOL=1(falling edge)	Acknowlegement Detect (ACK) - Rising edge of 9th bit of SCLi		UARTi Reception - Falling edge of 9th bit of SCLi	
Data Transfer Timing from the UART Receive Shift Register to the UiRB Register	CKPOL=0(rising edge) CKPOL=1(falling edge)	Rising edge of 9th bit of SCLi		Falling edge of 9th bit of SCLi	Falling edge and rising edge of 9th bit of SCLi
UARTi Transmit Output Delay	No delay	Delay			
P6₃, P6₇, P7₀, P9₂, P9₆ Pin Functions	TxDi output	SDAi input and output			
P6₂, P6₆, P7₁, P9₁, P9₇ Pin Functions	RxDi input	SCLi input and output			
P6₁, P6₅, P7₂, P9₀, P9₅ Pin Functions	Select CLKi input or output	– (Not used in I²C mode)			
Noise Filter Width	15ns	200ns			
Reading RxDi and SCLi Pin Levels	Can be read if port direction bit is set to "0"	Can be read regardless of the port direction bit			
Default Value of TxDi, SDAi Output	CKPOL=0 (H) CKPOL=1 (L)	Values set in the port register before entering I²C mode(2)			
SCLi Default and End Value	–	H	L	H	L
DMA Generated (See Figure 16.20)	UARTi reception	Acknowlegement detect (ACK)		UARTi Reception - Falling edge of 9 bit of SCLi	
Store Received Data	1st to 8th bits of the received data are stored into bits 0 to 7 in the UiRB register	1st to 8th bits of the received data are stored into bits 7 to 0 in the UiRB register		1st to 7th bits of the received data are stored into bits 6 to 0 in the UiRB register. 8th bit is stored into bit 8 in the UiRB register.	1st to 8th bits are stored into bits 7 to 0 in the UiRB register(3)
Reading Received Data	The UiRB register status is read				Bits 6 to 0 in the UiRB registerts(4) are read as bit 7 to 1. Bit 8 in the UiRB register is read as bit 0

i=0 to 4

NOTES:

1. Follow the procedures below to change how an interrupt is generated.
   (a) Disable interrupt of corresponding interrupt number.
   (b) Change how an interrupt is generated.
   (c) Set the IR bit of a corresponding interrupt number to "0" (no interrupt requested).
   (d) Set the ILVL2 to ILVL0 bits of a corresponding interrupt number.
2. Set default value of the SDAi output when the SMD2 to SMD0 bits in the UiMR register are set to "000₂" (serial I/O disabled).
3. Second data transfer to the UiRB register (on the rising edge of the ninth bit of SCLi).
4. First data transfer to the UiRB register (on the falling edge of the ninth bit of SCLi).

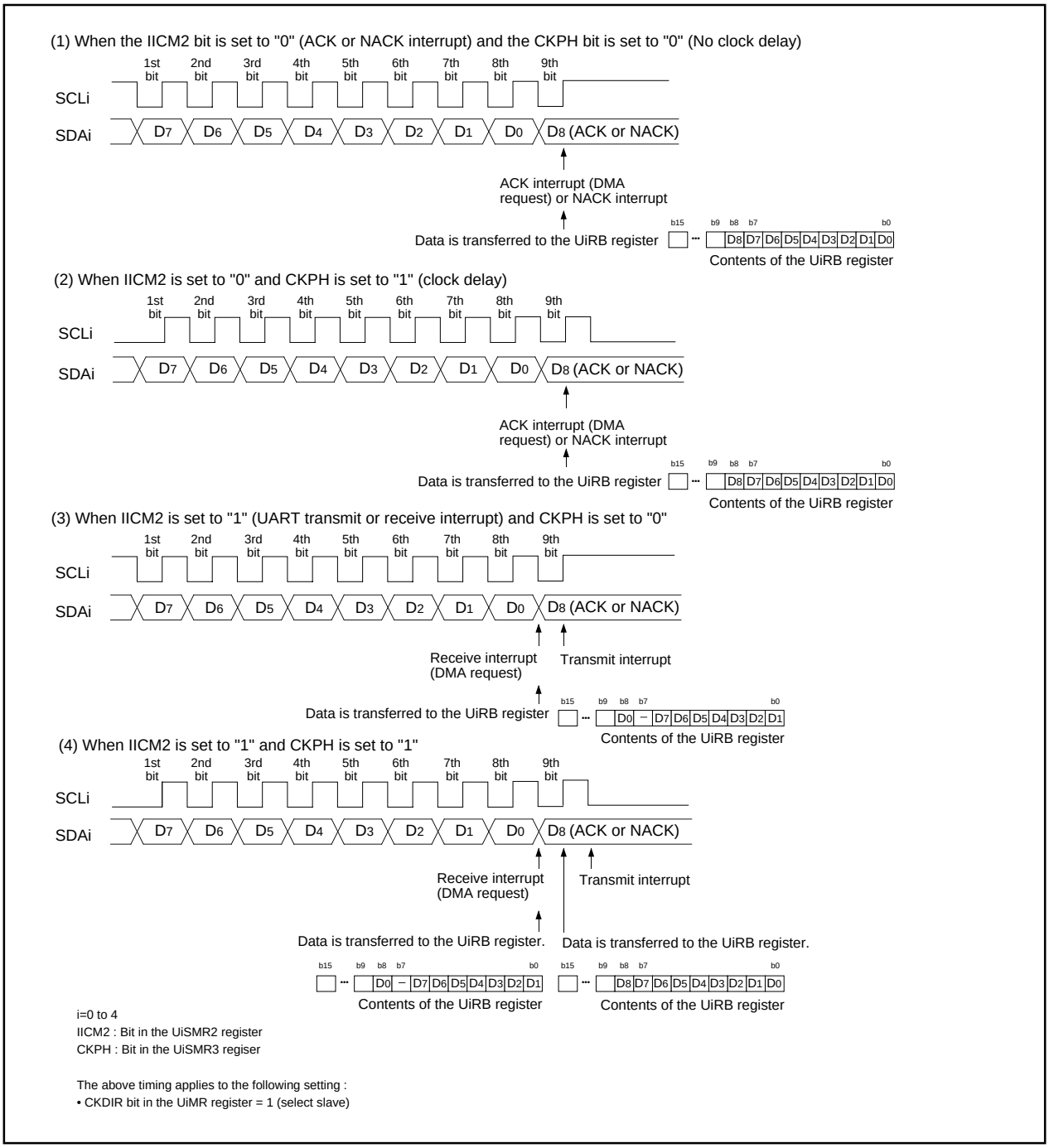


Figure 16.20 UiRB Register Transfer and Interrupt Timings

Table 16.14 Pin Settings in I²C Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P62	SCL0 output	PS0_2=1	PSL0_2=0	-
	SCL0 input	PS0_2=0	-	PD6_2=0
P63	SDA0 output	PS0_3=1	-	-
	SDA0 input	PS0_3=0	-	PD6_3=0
P66	SCL1 output	PS0_6=1	PSL0_6=0	-
	SCL1 input	PS0_6=0	-	PD6_6=0
P67	SDA1 output	PS0_7=1	-	-
	SDA1 input	PS0_7=0	-	PD6_7=0

Table 16.15 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
$P7_0$(1)	SDA2 output	PS1_0=1	PSL1_0=0	PSC_0=0	-
	SDA2 input	PS1_0=0	-	-	PD7_0=0
$P7_1$(1)	SCL2 output	PS1_1=1	PSL1_1=0	PSC_1=0	
	SCL2 input	PS1_1=0	-	-	PD7_1=0

NOTES:
1. $P7_0$ and $P7_1$ are ports for the N-channel open drain output.

Table 16.16 Pin Settings (3)

Port	Function	Setting		
		PS3 Register(1)	PSL3 Register	PD9 Register(1)
$P9_1$	SCL3 output	PS3_1=1	PSL3_1=0	-
	SCL3 input	PS3_1=0	-	PD9_1=0
$P9_2$	SDA3 output	PS3_2=1	PSL3_2=0	-
	SDA3 input	PS3_2=0	-	PD9_2=0
$P9_6$	SDA4 output	PS3_6=1	-	-
	SDA4 input	PS3_6=0	-	PD9_6=0
$P9_7$	SCL4 output	PS3_7=1	PSL3_7=0	-
	SCL4 input	PS3_7=0	-	PD9_7=0

NOTES:
1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

16.3.1 Detecting Start Condition and Stop Condition

The microcomputer detects either a start condition or stop condition. The start condition detect interrupt is generated when the SCLi (i=0 to 4) pin is held high ("H") and the SDAi pin changes high ("H") to low ("L"). The stop condition detect interrupt is generated when the SCLi pin is held high ("H") and the SDAi pin changes low ("L") to high ("H"). The start condition detect interrupt shares interrupt control registers and vectors with the stop condition detect interrupt. The BBS bit in the UiSMR register determines which interrupt is requested.

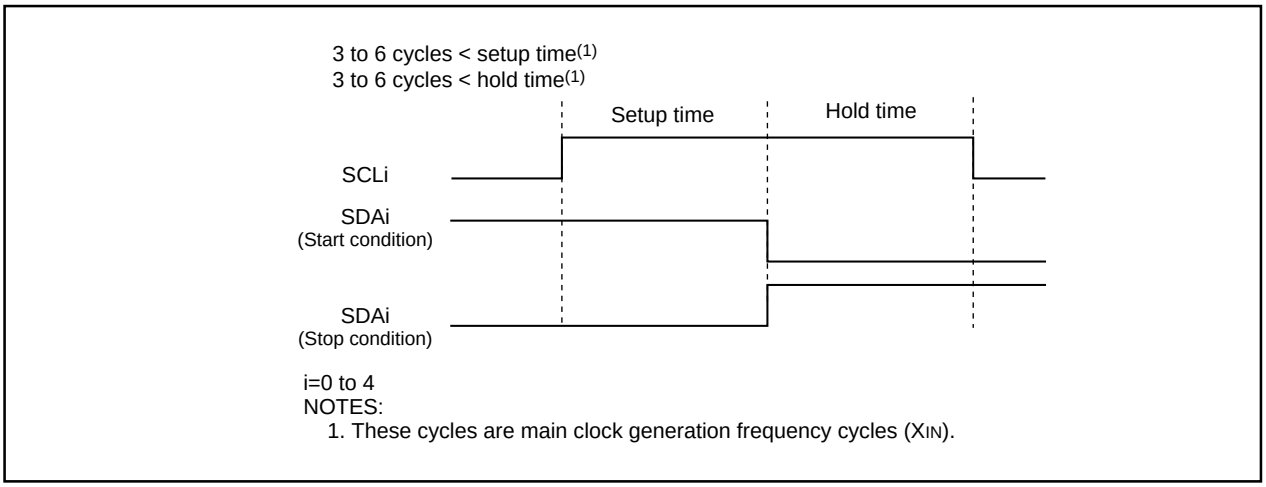


Figure 16.21 Start Condition or Stop Condition Detect

16.3.2 Start Condition or Stop Condition Output

The start condition is generated when the STAREQ bit in the UiSMR4 register (i=0 to 4) is set to "1" (start). The restart condition is generated when the RSTAREQ bit in the UiSMR4 register is set to "1" (start). The stop condition is generated when the STPREQ bit in the UiSMR4 is set to "1" (start).

The start condition is output when the STAREQ bit is set to "1" and the STSPSEL bit in the UiSMR4 register is set to "1" (start or stop condition generation circuit selected). The restart condition is output when the RSTAREQ bit and STSPSEL bit are set to "1". The stop condition is output when the STPREQ bit and the STSPSEL bit are set to "1".

When the start condition, stop condition or restart condition is output, do not generate an interrupt between the instruction to set the STAREQ bit, STPREQ bit or RSTAREQ bit to "1" and the instruction to set the STSPSEL bit to "1". When the start condition is output, set the STAREQ bit to "1" before the STSPSEL bit is set to "1".

Table 16.17 lists function of the STSPSEL bit. Figure 16.22 shows functions of the STSPSEL bit.

Table 16.17 STSPSEL Bit Function

Function	STSPSEL = 0	STSPSEL = 1
Start condition and stop condition output	Program with a port determines how the start condition or stop condition is output	The STAREQ bit, RSTAREQ bit and STPREQ bit determine how the start condition or stop condition is output
Timing to generate a start condition and stop condition interrupt request	The start condition and stop condition are detected	Start condition and stop condition generation are completed

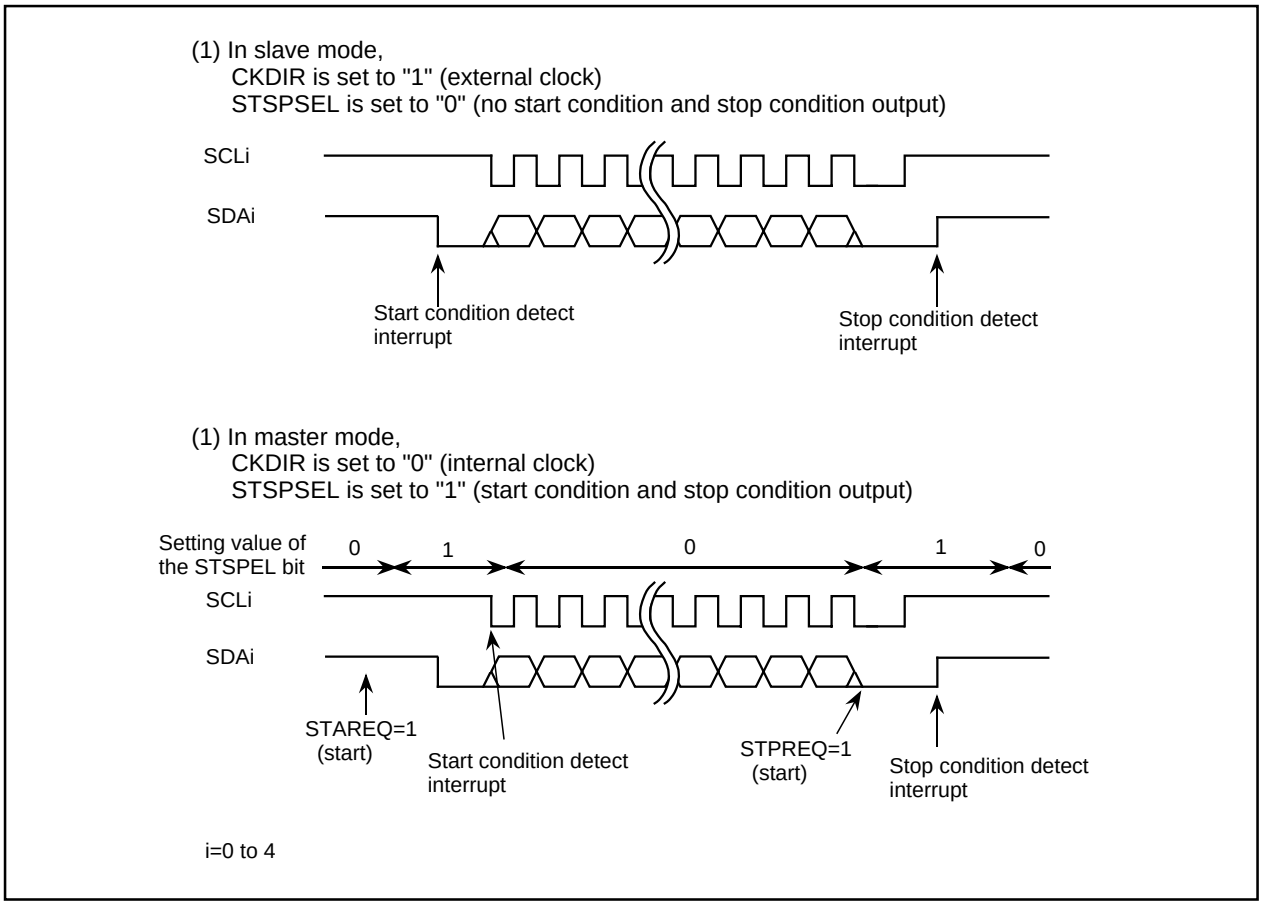


Figure 16.22 STSPSEL Bit Function

16.3.3 Arbitration

The ABC bit in the UiSMR register (i=0 to 4) determines an update timing for the ABT bit in the UiRB register. On the rising edge of SCLi, the microcomputer determines whether a transmit data matches data input to the SDAi pin.

When the ABC bit is set to "0" (update per bit), the ABT bit is set to "1" as soon as a data discrepancy is detected. The ABT bit is set to "0" if not detected. When the ABC bit is set to "1", the ABT bit is set to "1" (detected-arbitration is lost) on the falling edge of the ninth bit of the transfer clock if any discrepancy is detected. When the ABT bit is updated per byte, set the ABT bit to "0" (not detected-arbitration is won) between an ACK detection in the first byte data and the next byte data to be transferred. When the ALS bit in the UiSMR2 register is set to "1" (SDA output stop enabled), the arbitration lost occurs. As soon as the ABT bit is set to "1", the SDAi pin is placed in a high-impedance state.

16.3.4 Transfer Clock

The transfer clock transmits and receives data as is shown in Figure 16.22

The CSC bit in the UiSMR2 register (i=0 to 4) synchronizes an internally generated clock (internal SCLi) with the external clock that is applied to the SCLi pin. When the CSC bit is set to "1" (clock synchronous enabled) and the internal SCLi is held high ("H"), the internal SCLi become low ("L") if the SCLi pin is on the falling edge. The UiBRG register is reloaded to start counting for the "L" leg. A counter stops when the SCLi pin is held "L" and then the internal SCLi changes "L" to "H". Counting is resumed when the SCLi pin become "H". The transfer clock of UARTi is equivalent to the AND for signals from the internal SCLi and the SCLi pin.

The transfer clock is synchronized between a half cycle before the falling edge of first bit of the internal SCLi and the rising edge of the ninth bit. Select the internal clock as the transfer clock while the CSC bit is set to "1".

The SWC bit in the UiSMR2 register determines whether the SCLi pin is fixed to output an "L" signal on the falling edge of the ninth cycle of the transfer clock or not.

When the SCLHI bit in the UiSMR4 register is set to "1" (enabled), a SCLi output stops when a stop condition is detected (high-impedance).

When the SWC2 bit in the UiSMR2 register is set to "1" (0 output), the SCLi pin forcibly outputs an "L" signal while transmitting and receiving. The fixed "L" signal applied to the SCLi pin is cancelled by setting the SWC2 bit to "0" (transfer clock) and the transfer clock is input to and output from the SCLi pin.

When the CKPH bit in the UiSMR3 register is set to "1" and the SWC9 bit in the UiSMR4 register is set to "1" (SCL "L" hold enabled), the SCLi pin is fixed to output an "L" signal on the next falling edge after the ninth bit of the clock. The fixed "L" signal applied to the SCLi pin is cancelled by setting the SWC9 bit to "0" (SCL "L" hold disabled).

16.3.5 SDA Output

Values in bits 7 to 0 (D_7 to D_0) in the UiTB register (i=0 to 4) are output in descending order from D_7. The ninth bit (D_8) is ACK or NACK.

Set the default value of SDAi transmit output when the IICM bit is set to "1" (I^2C mode) and the SMD2 to SMD0 bits in the UiMR register are set to "000_2" (serial I/O disabled).

The DL2 to DL0 bits in the UiSMR3 register determine no delay in the SDAi output or a delay of 2 to 8 UiBRG register count source cycles.

When the SDHI bit in the UiSMR2 register is set to "1" (SDA output disabled), the SDAi pin is forcibly placed in a high-impedance state. Do not set in the SDHI bit on the rising edge of the URTi transfer clock.

The ABT bit in the UiRB register may be set to "1" (detected).

16.3.6 SDA Input

When the IICM2 bit in the UiSMR2 register (i=0 to 4) is set to "0", the first eight bits of received data are stored into bits 7 to 0 (D_7 to D_0) in the UiRB register. The ninth bit (D_8) is ACK or NACK.

When the IICM2 bit is set to "1", the first seven bits (D_7 to D_1) of received data are stored into bits 6 to 0 in the UiRB register. Store the eighth bit (D_0) into bit 8 in the UiRB register.

If the IICM bit in the UiSMR register is set to "1" and the CKPH bit is set to "1", the same data as that of when setting the IICM2 bit to "0" can be read. To read the data, read the UiRB register after the rising edge of the ninth bit of the transfer clock.

16.3.7 ACK, NACK

When the STSPSEL bit in the UiSMR4 register (i=0 to 4) is set to "0" (serial I/O circuit selected) and the ACKC bit in the UiSMR4 register is set to "1" (ACK data output), the SDAi pin outputs the value set in the ACKD bit.

If the IICM2 bit is set to "0", the NACK interrupt request is generated when the SDAi pin is held high ("H") on the rising edge of the ninth bit of the transfer clock. The ACK interrupt request is generated when the SDAi pin is held low ("L") on the rising edge of the ninth bit of the transfer clock.

When ACK is selected to generate a DMA request, the DMA transfer is activated by an ACK detection.

16.3.8 Transmit and Receive Reset

When the STC bit in the UiSMR2 register is set to "1" (UARTi initialization enabled) and a start condition is detected,

- the transmit shift register is reset and the content of the UiTB register is transferred to the transmit shift register. The first bit starts transmitting when the next clock is input. UARTi output value remains unchanged between when clock is input and when data of the first bit is output. The value remains the same value as when start condition was detected.
- the receive shift register is reset and the first bit starts receiving when the next clock is input.
- the SWC bit is set to "1" (SCL wait output enabled). The SCLi pin becomes low ("L") on the falling edge of the ninth bit of the transfer clock.

If UARTi transmission and reception are started with this function, the TI bit remains unchanged. Select the external clock as the transfer clock when using this function.

16.4 Special Mode 2

In special mode 2, serial communication between one or multiple masters and multiple slaves is available. The $\overline{SSi}$ input pin (i=0 to 4) controls the serial bus communication. Table 16.18 lists specifications of special mode 2. Table 16.19 lists registers to be used and settings. Tables 16.20 to 16.22 list pin settings.

Table 16.18. Special Mode 2 Specifications

Item	Specification
Transfer Data Format	Transfer data : 8 bits long
Transfer Clock	The CKDIR bit in the UiMR register (i=0 to 4) is set to "0" (internal clock selected) : $f_j/2(m+1)$ $f_j = f_1, f_8, f_{2n}$(1) m : setting value of the UiBRG register 00_{16} to FF_{16} The CKDIR bit to "1" (external clock selected) : input clock from the CLKi pin
Transmit/Receive Control	Select from $\overline{CTS}$ function, $\overline{RTS}$ function or $\overline{CTS}/\overline{RTS}$ function disabled
Transmit Start Condition	•To start transmitting, the following requirements must be met(2) : - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register) - Apply an "L" signal to the $\overline{CTS}$i pin when the $\overline{CTS}$ function is selected
Receive Start Condition	• To start receiving, the following requirement must be met(2) : - Set the RE bit in the UiC1 register to "1" (receive enable) - Set the TE bit to "1" (receive enable) - Set the TI bit to "0" (data in the UiTB register)
Interrupt Request Generation Timing	• Transmit interrupt timing can be selected from the followings: - The UiIRS bit in the UiC1 register is set to "0" (no data in a transmit buffer) : when data is transferred from the UiTB register to the UARTi transmit register (transmission started) - The UiIRS register is set to "1" (transmission completed): when data transmission from UARTi transfer register is completed • Receive interrupt timing When data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detection	•Overrun error(3) This error occurs when the seventh bit of the next received data is read before reading the UiRB register
Selectable Function	• CLK polarity Select from the rising edge or falling edge of the transfer clock when transferred data is output and input • LSB first or MSB first Data is transmitted/received in either bit 0 or in bit 7 • Continuous receive mode Reception is enabled simultaneously by reading the UiRB register • Serial data logic inverse This function inverses transmitted/received data logically • TxD, RxD I/O polarity switching TxD pin output and RxD pin input are inversed. All I/O data levels are also inversed • Clock phase Select from one of 4 combinations of transfer data polarity and phases • $\overline{SSi}$ input pin function Output pin is placed in a high-impedance state to avoid data conflict between master and other masters or slaves

NOTES:

1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).
2. To start transmission/reception when selecting the external clock, these conditions must be met after the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and data is received on the rising edge) and the CLKi pin is held high ("H"), or when the CKPOL bit is set to "1" (Data is transmitted on the rising edge of the transfer clock and data is received on the falling edge) and the CLKi pin is held low ("L").
3. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).

Table 16.19. Registers To Be Used and Settings in Special Mode 2

Register	Bit	Function
UiTB	0 to 7	Set transmit data
UiRB	0 to 7	Received data can be read
	OER	Overrun error flag
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to "001$_2$"
	CKDIR	Set to "0" in master mode or "1" in slave mode
	IOPOL	Set to "0"
UiC0	CLK0, CLK1	Select count source for the UiBRG register
	CRS	Disabled since CRD = 1
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Select the output format of the TxDi pin
	CKPOL	Clock phase can be set by the combination of the CKPOL bit and the CKPH bit in the UiSMR3 register
	UFORM	Select either LSB first or MSB first
UiC1	TE	Set to "1" to enable data transmission and reception
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select how the UARTi transmit interrupt is generated
	UiRRM	Set to "1" to enable continuous receive mode
	UiLCH, SCLKSTPB	Set to "0"
UiSMR	0 to 7	Set to "00$_{16}$"
UiSMR2	0 to 7	Set to "00$_{16}$"
UiSMR3	SSE	Set to "1"
	CKPH	Clock phase can be set by the combination of the CKPH bit and the CKPOL bit in the UiC0 register
	DINC	Set to "0" in master mode or "1" in slave mode
	NODC	Set to "0"
	ERR	Fault error flag
	5 to 7	Set to "000$_2$"
UiSMR4	0 to 7	Set to "00$_{16}$"
IFSR	IFSR6, IFSR7	Select how fault error occurs

i=0 to 4

Table 16.20 Pin Settings in Special Mode 2 (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	$\overline{SS0}$ input	PS0_0=0	–	PD6_0=0
P61	CLK0 input (slave)	PS0_1=0	–	PD6_1=0
	CLK0 output (master)	PS0_1=1	–	–
P62	RxD0 input (master)	PS0_2=0	–	PD6_2=0
	STxD0 output (slave)	PS0_2=1	PSL0_2=1	–
P63	TxD0 output (master)	PS0_3=1	–	–
	SRxD0 input (slave)	PS0_3=0	–	PD6_3=0
P64	$\overline{SS1}$ input	PS0_4=0	–	PD6_4=0
P65	CLK1 input (slave)	PS0_5=0	–	PD6_5=0
	CLK1 output (master)	PS0_5=1	–	–
P66	RxD1 input (master)	PS0_6=0	–	PD6_6=0
	STxD1 output (slave)	PS0_6=1	PSL0_6=1	–
P67	TxD1 output (master)	PS0_7=1	–	–
	SRxD1 input (slave)	PS0_7=0	–	PD6_7=0

Table 16.21 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70(1)	TxD2 output (master)	PS1_0=1	PSL1_0=0	PSC_0=0	–
	SRxD2 input (slave)	PS1_0=0	–	–	PD7_0=0
P71(1)	RxD2 input (master)	PS1_1=0	–	–	PD7_1=0
	STxD2 output (slave)	PS1_1=1	PSL1_1=1	PSC_1=0	–
P72	CLK2 input (slave)	PS1_2=0	–	–	PD7_2=0
	CLK2 output (master)	PS1_2=1	PSL1_2=0	PSC_2=0	–
P73	$\overline{SS2}$ input	PS1_3=0	–	–	PD7_3=0

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 16.22 Pin Settings (3)

Port	Function	Setting		
		PS3 Register(1)	PSL3 Register	PD9 Register(1)
P90	CLK3 input (slave)	PS3_0=0	–	PD9_0=0
	CLK3 output (master)	PS3_0=1	–	–
P91	RxD3 input (master)	PS3_1=0	–	PD9_1=0
	STxD3 output (slave)	PS3_1=1	PSL3_1=1	–
P92	TxD3 output (master)	PS3_2=1	PSL3_2=0	–
	SRxD3 input (slave)	PS3_2=0	–	PD9_2=0
P93	$\overline{SS3}$ input	PS3_3=0	PSL3_3=0	PD9_3=0
P94	$\overline{SS4}$ input	PS3_4=0	PSL3_4=0	PD9_4=0
P95	CLK4 input (slave)	PS3_5=0	PSL3_5=0	PD9_5=0
	CLK4 output (master)	PS3_5=1	–	–
P96	TxD4 output (master)	PS3_6=1	–	–
	SRxD4 input (slave)	PS3_6=0	PSL3_6=0	PD9_6=0
P97	RxD4 input (master)	PS3_7=0	–	PD9_7=0
	STxD4 output (slave)	PS3_7=1	PSL3_7=1	–

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

16.4.1 $\overline{SSi}$ Input Pin Function (i=0 to 4)

When the SSE bit in the UiSMR3 register is set to "1" ($\overline{SS}$ function enabled), the $\overline{SSi}$ input pin function is selected, activating the pin function.

The DINC bit in the UiSMR3 register determines which microcomputer performs as master or slave. When multiple microcomputers perform as the masters (multi-master system), the $\overline{SSi}$ pin setting determines which master microcomputer is active and when.

16.4.1.1 When Setting the DINC Bit to "1" (Slave Mode)

When an "H" signal is applied to the $\overline{SSi}$ pin, the STxDi and SRxDi pins are placed in a high-impedance state and the transfer clock input to the CLKi pin is ignored. When a low-level signal ("L") is applied to the $\overline{SSi}$ input pin, the transfer clock input is valid and serial communication is enabled.

16.4.1.2 When Setting the DINC Bit to "0" (Master Mode)

When an "H" signal is applied to the $\overline{SSi}$ pin, serial communication is available due to transmission privilege. The master outputs the transfer clock. When an "L" signal is applied to the $\overline{SSi}$ pin, it indicates that another master is active and TxDi, RxDi and CLKi pins are placed in a high-impedance state. Moreover, a fault error occurs and the IR bit in the BCNiIC register is set to "1" (interrupt requested). The ERR bit in the UiSMR3 register indicates whether a fault error occurs.

In master mode, software interrupt numbers 39, 40 and 41 are used for the fault error interrupt. The fault error interrupt is generated when the ERR bit changes "0" to "1". The fault error interrupt of UART0 and of UART3 share an interrupt vector. The fault error interrupt of UART1 and of UART4 share an interrupt vector. The IFSR6 and IFSR7 bits in the IFSR register determine which fault error interrupt is used.

Communication is not terminated even if a fault error is generated while communicating. To stop communication, the SMD 2 to SMD0 bit in the UiMR register is set to "000$_2$" (serial I/O disabled).

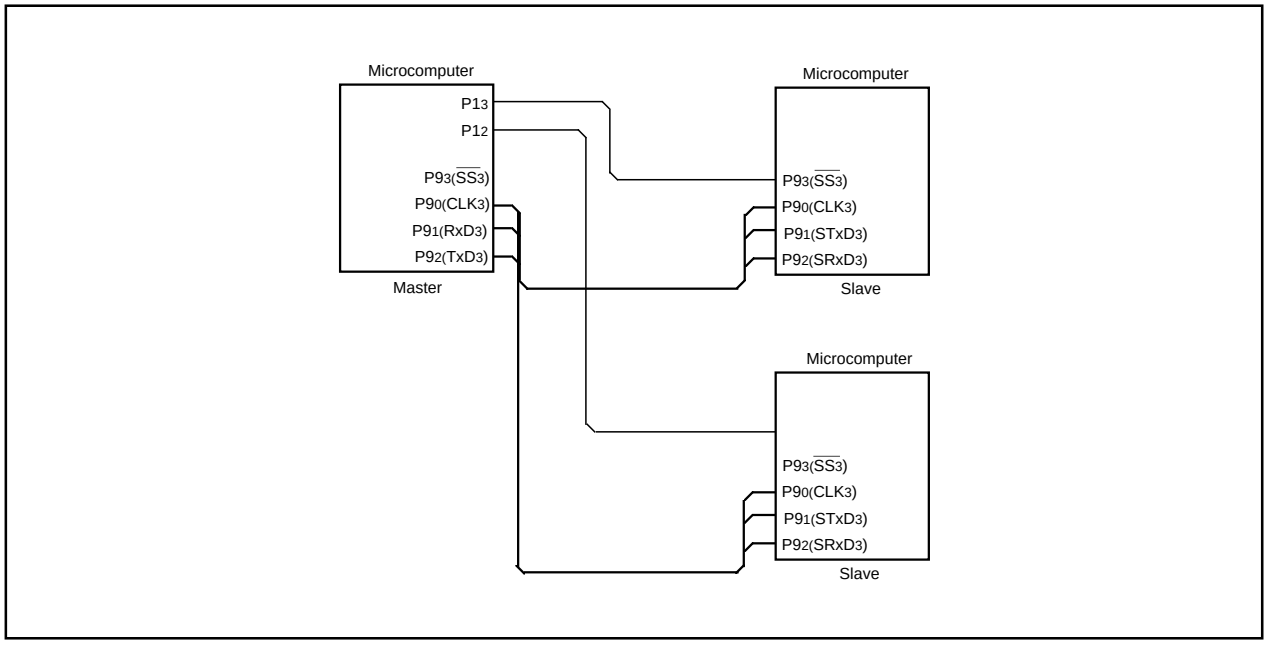


Figure 16.23 Serial Bus Communication Control with $\overline{SS}$ Pin

16.4.2 Clock Phase Function

The CKPH bit in the UiSMR3 register (i=0 to 4) and the CKPOL bit in the UiC0 register select one of four combinations of transfer clock polarity and phases.

The transfer clock phase and polarity must be the same between the master and the slave involved in the transfer.

16.4.2.1 When setting the DINC Bit to "0" (Master (Internal Clock))

Figure 16.24 shows transmit and receive timing.

16.4.2.2 When Setting the DINC Bit to "1" (Slave (External Clock))

When the CKPH bit is set to "0" (no clock delay) and the $\overline{SSi}$ input pin is held high ("H"), the STxDi pin is placed in a high-impedance state. When the $\overline{SSi}$ input pin becomes low ("L"), conditions to start a serial transfer are met, but output is indeterminate. The serial transmission is synchronized with the transfer clock. Figure 16.25 shows the transmit and receive timing.

When the CKPH bit is set to "1" (clock delay) and the $\overline{SSi}$ input pin is held high ("H"), the STxDi pin is placed in a high-impedance state. When the $\overline{SSi}$ pin becomes low ("L"), the first data is output. The serial transmission is synchronized with the transfer clock. Figure 16.26 shows the transmit and receive timing.

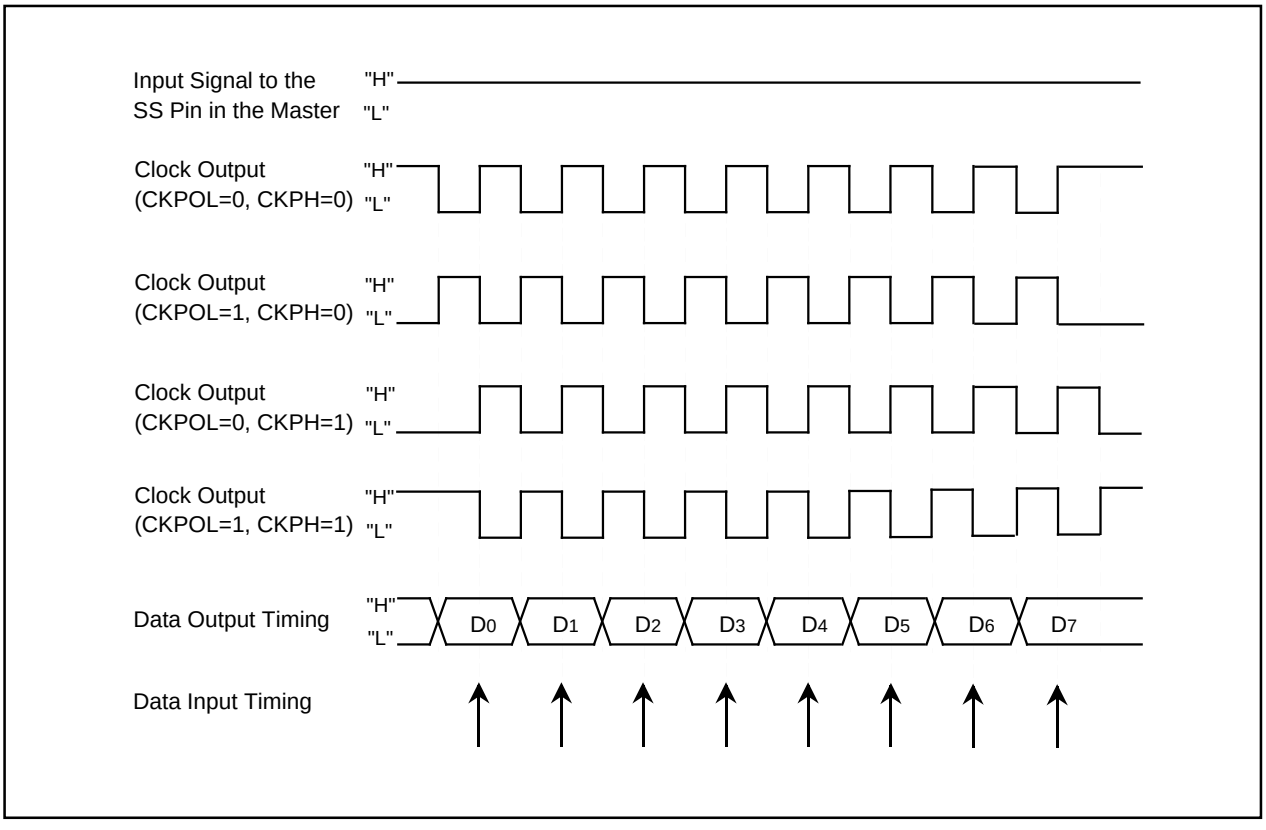
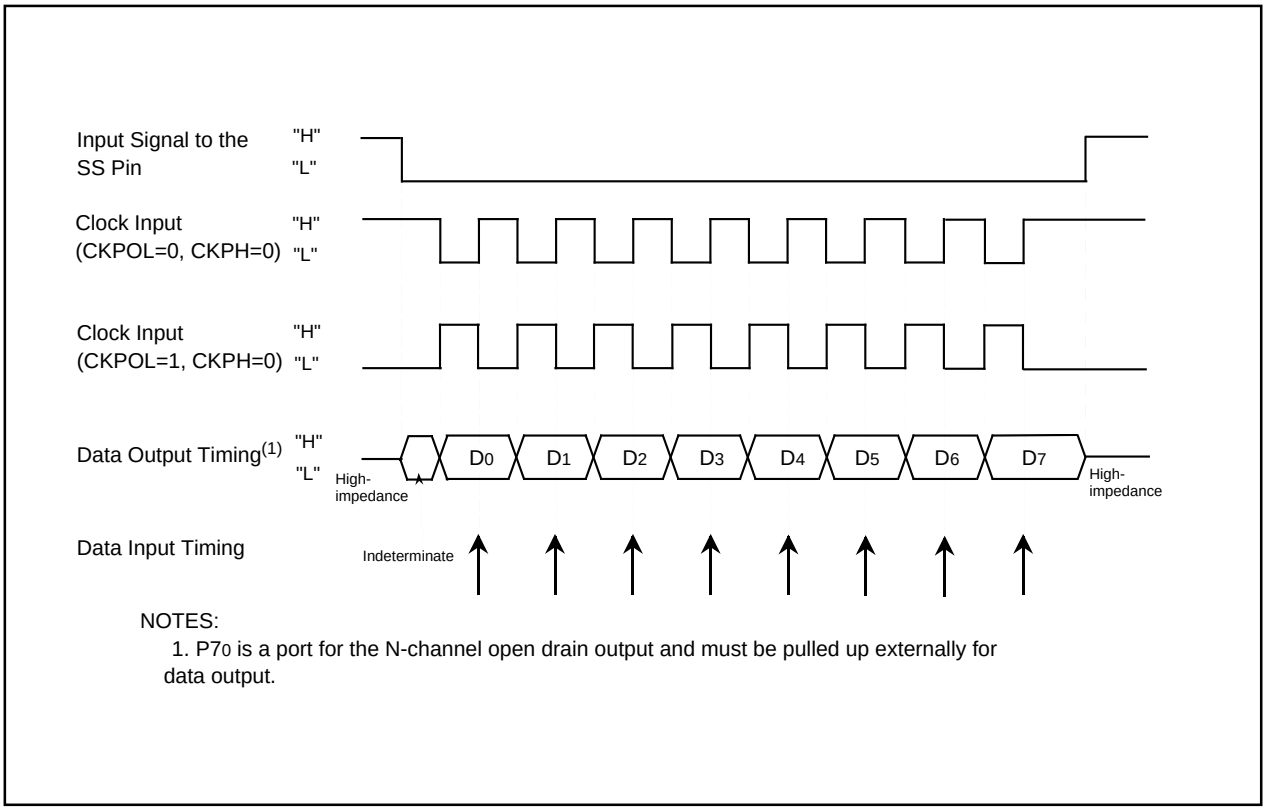
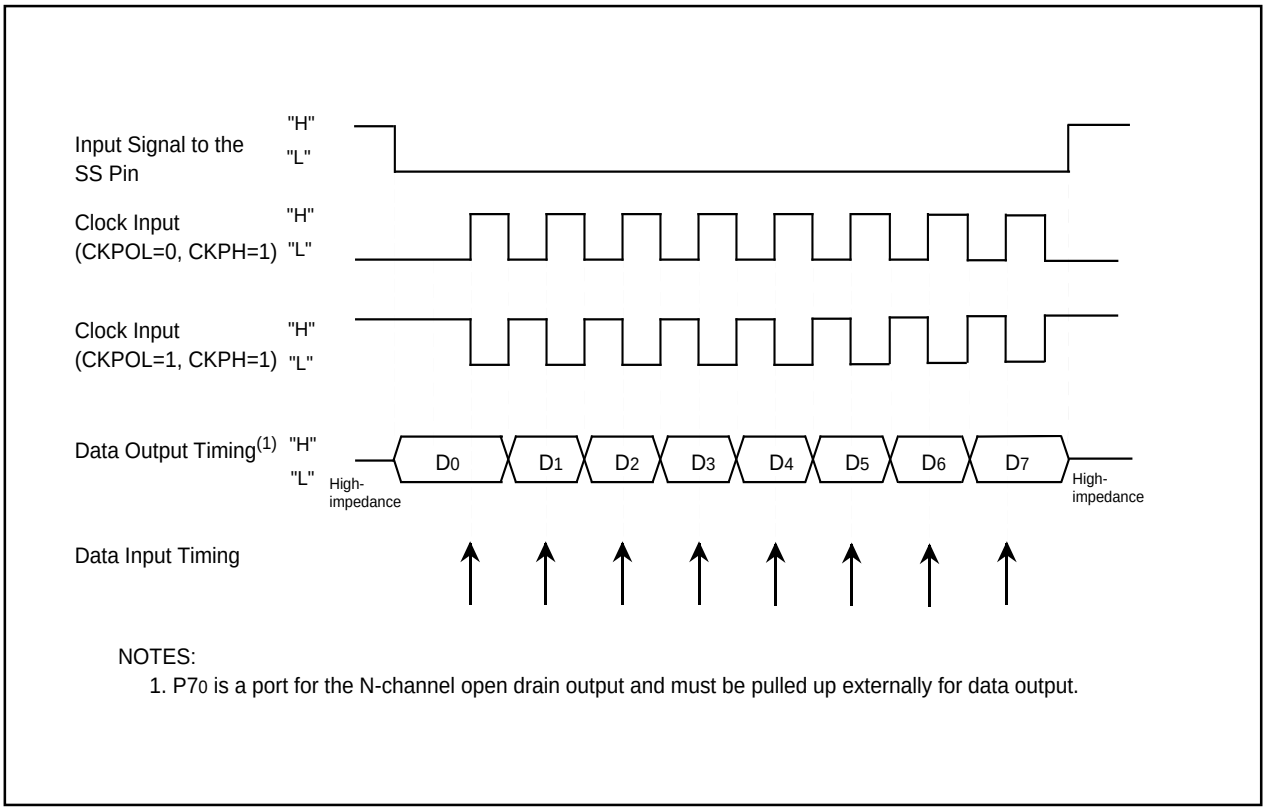


Figure 16.24 Transmit and Receive Timing in Master Mode (Internal Clock)



NOTES:
1. P7$_0$ is a port for the N-channel open drain output and must be pulled up externally for data output.

Figure 16.25 Transmit and Receive Timing in Slave Mode (External Clock) (CKPH=0)



NOTES:
1. P7$_0$ is a port for the N-channel open drain output and must be pulled up externally for data output.

Figure 16.26 Transmit and Receive Timing in Slave Mode (External Clock) (CKPH=1)

16.5 Special Mode 3 (GCI Mode)

In GCI mode, the external clock is synchronized with the transfer clock used in the clock synchronous serial I/O mode.

Table 16.23 lists specifications of GCI mode. Table 16.24 lists registers to be used and settings. Tables 16.25 to 16.27 list pin settings.

Table16.23 GCI Mode Specifications

Item	Specification
Transfer Data Format	Transfer data : 8 bits long
Transfer Clock	The CKDIR bit in the UiMR register (i=0 to 4) is set to "1" (external clock selected): an input from the CLKi pin
Clock Synchronization Function	The $\overline{\text{CTSi}}$ pin inputs a trigger
Transmit/Receive Start Conditions	When a trigger signal is applied to the CTSi pin under the following conditions: • Set the TE bit in the UiC1 register to "1" (transmit enable) • Set the RE bit in the UiC1 register to "1" (receive enable) • Set the TI bit in the UiC1 register to "0" (data in UiTB register)
Interrupt Request Generation Timing	Transmit interrupt timing can be selected from the followings: • The UiIRS bit in the UiC1 register is set to "0" (UiTB register empty) : when data is transferred from the UiTB register to the UARTi transmit register (transmission started) • The UiIRS bit is set to "1" (transmit completed): when a data transmission from the UARTi transfer register is completed Receive interrupt timing when data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detection	Overrun error(1) This error occurs when the seventh bit of the next received data is read before reading the UiRB register.

NOTES:

1. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).

Table 16.24 Registers To Be Used and Settings in GCI Mode

Register	Bit	Function
UiTB	0 to 7	Set transmit data
UiRB	0 to 7	Received data
	OER	Overrun error flag
UiBRG	0 to 7	Set to "00$_{16}$"
UiMR	SMD2 to SMD0	Set to "001$_2$"
	CKDIR	Set to "1"
	IOPOL	Set to "0"
UiC0	CLK1 to CLK0	Set to "00$_2$"
	CRS	Disabled because CRD = 1
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Select the output format of the TxDi pin
	CKPOL	Set to "0"
	UFORM	Set to "0"
UiC1	TE	Set to "1" to enable data transmission and reception
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select how the UARTi transmit interrupt is generated
	UiRRM, UiLCH	Set to "0"
	SCLKSTPB	Set to "0"
UiSMR	0 to 6	Set to "0000000$_2$"
	SCLKDIV	See Table 16.28
UiSMR2	0 to 6	Set to "0000000$_2$"
	SU1HIM	See Table 16.28
UiSMR3	0 to 2	Set to "000$_2$"
	NODC	Set to "0"
	4 to 7	Set to "0000$_2$"
UiSMR4	0 to 7	Set to "00$_{16}$"

i=0 to 4

Table 16.25 Pin Settings in CGI Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	$\overline{CTS0}$ input(1)	PS0_0=0	–	PD6_0=0
P61	CLK0 input	PS0_1=0	–	PD6_1=0
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P64	$\overline{CTS1}$ input(1)	PS0_4=0	–	PD6_4=0
P65	CLK1 input	PS0_5=0	–	PD6_5=0
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

NOTES:
1. $\overline{CTS}$ input is used to input a trigger.

Table 16.26 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70(1)	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71(1)	RxD2 input	PS1_1=0	–	–	PD7_1=0
P72	CLK2 input	PS1_2=0	–	–	PD7_2=0
P73	$\overline{CTS2}$ input(2)	PS1_3=0	–	–	PD7_3=0

NOTES:
1. P70 and P71 are ports for the N-channel open drain output.
2. $\overline{CTS}$ input is used to input a trigger.

Table 16.27 Pin Settings (3)

Port	Function	Setting		
		PS3 Register(1)	PSL3 Register	PD9 Register(1)
P90	CLK3 input	PS3_0=0	–	PD9_0=0
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P93	$\overline{CTS3}$ input(2)	PS3_3=0	PSL3_3=0	PD9_3=0
P94	$\overline{CTS4}$ input(2)	PS3_4=0	PSL3_4=0	PD9_4=0
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:
1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.
2. $\overline{CTS}$ input is used to input a trigger.

To generate the internal clock synchronized with the external clock, first set the SU1HIM bit in the UiSMR2 register (i=0 to 4) and the SCLKDIV bit in the UiSMR register to values shown in Table 16.28. Then apply a trigger signal to the CTSi pin. Either the same clock cycle as the external clock or external clock divided by two can be selected as the transfer clock. The SCLKSTPB bit in the UiC1 register controls the transfer clock. Set the SCLKSTPB bit accordingly, to start or stop the transfer clock during an external clock operation. Figure 16.27 shows an example of the clock-divided synchronous function.

Table 16.28 Clock-Divided Synchronous Function Select

SCLKDIV Bit in UiSMR Register	SU1HIM Bit in UiSMR2 Register	Clock-Divided Synchronous Function	Example of Waveform
0	0	Not synchronized	-
0	1	Same division as the external clock	A in Figure 16.27
1	0 or 1	Same division as the external clock divided by 2	B in Figure 16.27

i=0 to 4

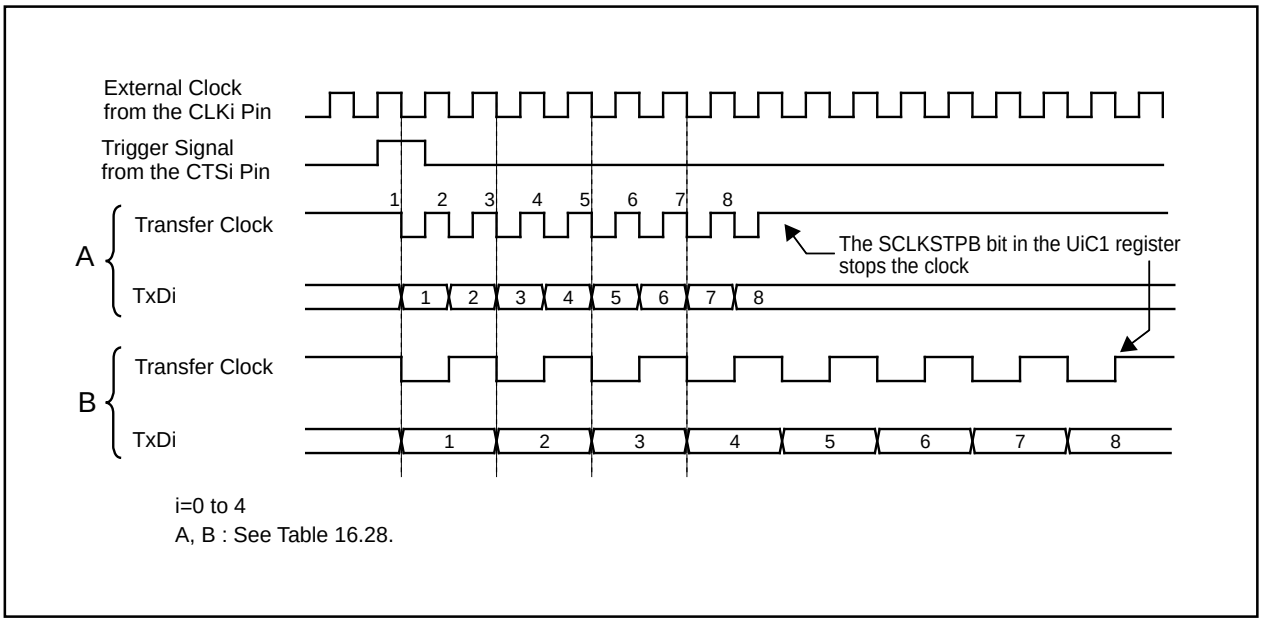


Figure 16.27 Clock-Divided Synchronous Function

16.6 Special Mode 4 (IE Mode)

In IE mode, devices connected with the IEBus can communicate in UART mode.

Table 16.29 lists registers to be used and settings. Tables 16.30 to 16.32 list pin settings.

Table 16.29. Registers To Be Used and Settings in IE Mode

Register	Bit	Function
UiTB	0 to 8	Set transmit data
UiRB	0 to 8	Received data can be read
	OER, FER, PER, SUM	Error flags
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to "110_2"
	CKDIR	Select the internal clock or external clock
	STPS	Set to "0"
	PRY	Disabled because PRYE=0
	PRYE	Set to "0"
	IOPOL	Select TxD and RxD I/O polarity
UiC0	CLK1 to CLK0	Select the count source for the UiBRG register
	CRS	Disabled because CRD=1
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Select output format of the TxDi pin
	CKPOL	Set to "0"
	UFORM	Set to "0"
UiC1	TE	Set to "1" to enable data transmission
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select how the UARTi transmit interrupt is generated
	UiRRM, UiLCH, SCLKSTPB	Set to "0"
UiSMR	0 to 3	Set to "0000_2"
	ABSCS	Select bus conflict detect sampling timing
	ACSE	Set to "1" to automatically clear the transmit enable bit
	SSS	Select transmit start condition
	SCLKDIV	Set to "0"
UiSMR2	0 to 7	Set to "00_{16}"
UiSMR3	0 to 7	Set to "00_{16}"
UiSMR4	0 to 7	Set to "00_{16}"
IFSR	IFSR6, IFSR7	Select how the bus conflict interrupt occurs

i=0 to 4

Table 16.30 Pin Settings in IE Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P61	CLK0 input	PS0_1=0	–	PD6_1=0
	CLK0 output	PS0_1=1	–	–
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P65	CLK1 input	PS0_5=0	–	PD6_5=0
	CLK1 output	PS0_5=1	–	–
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

Table 16.31 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70(1)	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71(1)	RxD2 input	PS1_1=0	–	–	PD7_1=0
P72	CLK2 input	PS1_2=0	–	–	PD7_2=0
	CLK2 output	PS1_2=1	PSL1_2=0	PSC_2=0	–

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 16.32 Pin Settings (3)

Port	Function	Setting		
		PS3 Register(1)	PSL3 Register	PD9 Register(1)
P90	CLK3 input	PS3_0=0	–	PD9_0=0
	CLK3 output	PS3_0=1	–	–
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
	CLK4 output	PS3_5=1	–	–
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

If the output level of the TxDi pin (i=0 to 4) differs from the input level of the RxDi pin, an interrupt request is generated.

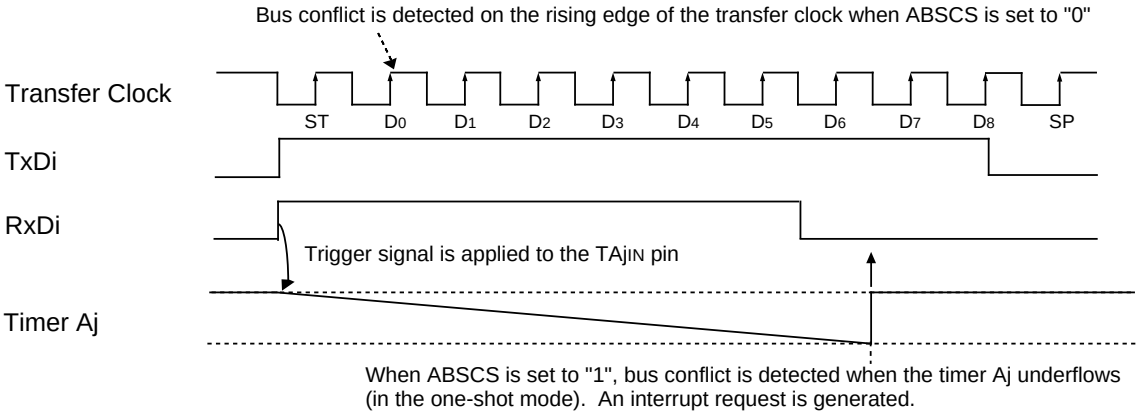
UART0 and UART3 are assigned software interrupt number 40. UART1 and UART4 are assigned number 41. When using the bus conflict detect function of UART0 or UART3, of UART1 or UART4, set the IFSR6 bit and the IFSR7 bit in the IFSR register accordingly.

When the ABSCS bit in the UiSMR register is set to "0" (rising edge of the transfer clock), it is determined, on the rising edge of the transfer clock, if the output level of the TxD pin and the input level of the RxD pin match. When the ABSCS bit is set to "1" (timer Aj underflow), it is determined when the timer Aj (timer A3 in UART0, timer A4 in UART1, timer A0 in UART2, timer A3 in UART3, the timer A4 in UART4) overflows. Use the timer Aj in one-shot timer mode.

When the ACSE bit in the UiSMR register is set to "1" (automatic clear at bus conflict) and the IR bit in the BCNiIC register to "1" (discrepancy detected), the TE bit is set to "0" (transmit disable).

When the SSS bit in the UiSMR register is set to "1" (synchronized with RxDi), the TxDi pin starts transmitting data on the falling edge of the RxDi pin. Figure 16.28 shows bits associated with the bus conflict detect function.

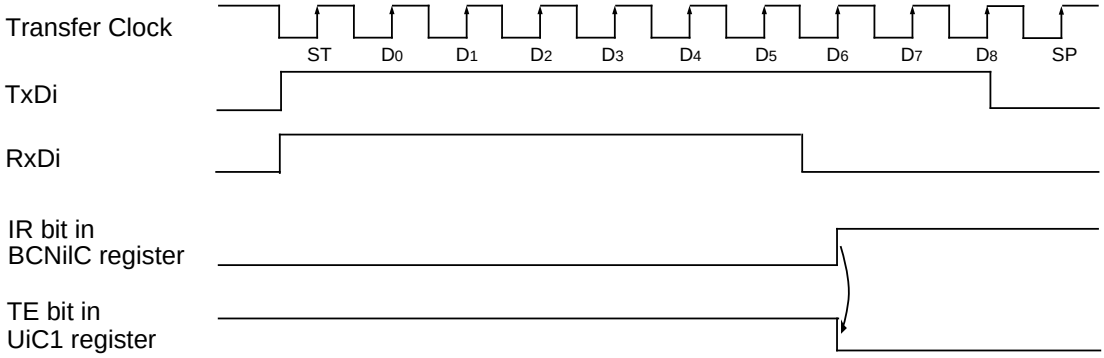
(1) The ABSCS Bit in the UiSMR Register (Bus conflict and sampling clock selected)
(i=0 to 4)



When ABSCS is set to "1", bus conflict is detected when the timer Aj underflows (in the one-shot mode). An interrupt request is generated.

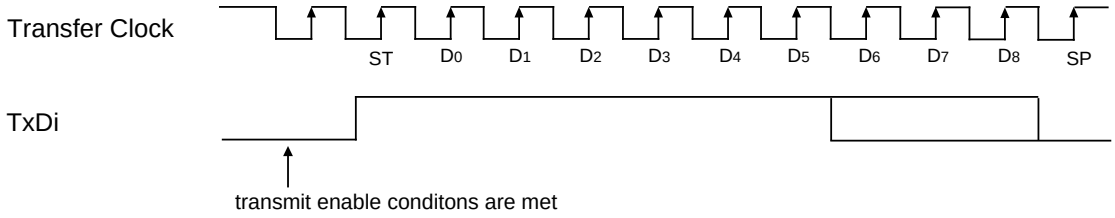
Timer Aj: timer A3 in UART0 or UART3, timer A4 in UART1 or UART4, timer A0 in UART2

(2) The ACSE Bit in the UiSMR Register (Transmit enable bit is automatically cleared)

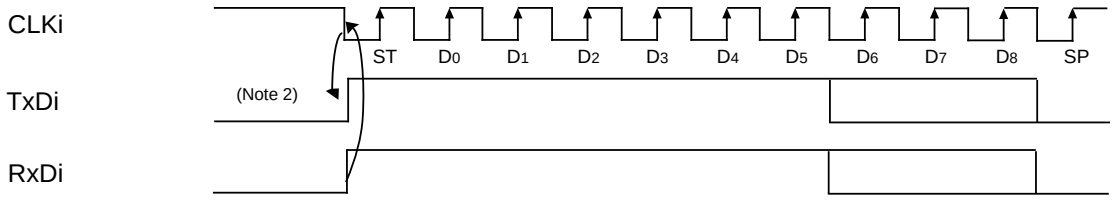


(3) The SSS bit in the UiSMR Register (Transmit start condition selected)

When SSS is set to "0", data is transmitted after one transfer clock cycle if data transmission is enabled.



When SSS is set to "1", data is transmitted on the rising edge of RxDi(1)



NOTES:
1. Data is transmitted on the falling edge of RxDi when IOPOL is set to "0".
   Data is transmitted on the rising edge of RxDi when IOPOL is set to "1".
2. Data transmission condition must be met before the falling edge of RxD.

Figure 16.28 Bit Function Related Bus Conflict Detection

16.7 Special Mode 5 (SIM Mode)

In SIM mode, SIM interface devices can communicate in UART mode. Both direct and inverse formats are available and the TxDi pin (i=0 to 4) can output an "L" signal when a parity error is detected.

Table 16.33 lists specifications of SIM mode. Table 16.34 lists registers to be used and register settings. Tables 16.35 to 16.37 list pin settings.

Table16.33 SIM Mode Specifications

Item	Specification
Transfer Data Format	• Transfer data: 8-bit UART mode • One stop bit • In direct format Parity: Even Data logic: Direct Transfer format: LSB first • In inverse format Parity: Odd Data logic: Inverse Transfer format: MSB first
Transfer Clock	The CKDIR bit in the UiMR register (i=0 to 4) is "0" (internal clock selected): $f_j/16(m+1)$(1) $f_j = f_1, f_8, f_{2n}$(2) m : setting value of the UiBRG register 00_{16} to FF_{16} Do not set the CKDIR bit to "1" (external clock selected)
Transmit/Receive Control	The CRD bit in the UiC0 register is set to "1" (CTS, RTS function disabled)
Other Setting Items	The UiIRS bit in the UiC1 register is set to "1" (transmission completed)
Transmit Start Condition	To start transmitting, the following requirements must be met: • Set the TE bit in the UiC1 register to "1" (transmit enable) • Set the TI bit in the UiC1 register to "0" (data being in the UiTB register)
Receive Start Condition	To start receiving, the following requirements must be met: • Set the RE bit in the UiC1 register to "1" (receive enable) • Detect the start bit
Interrupt Request Generation Timing	Transmit interrupt timing • The UiIRS bit is set to "1" (transmission is completed): when data transmission from the UARTi transfer register is completed Receive interrupt timing when data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detection	• Overrun error(1) This error occurs when the eighth bit of the next data is received before reading the UiRB register • Framing error This error occurs when the number of the stop bit set is not detected • Parity error This error occurs when the number of "1" in parity bit and character bits differ from the number set. • Error sum flag The SUM bit is set to "1" when an overrun error, framing error or parity error occurs.

NOTES:

1. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Table 16.34 Registers To Be Used and Settings

Register	Bit	Function
UiTB	0 to 7	Set transmit data
UiRB	0 to 7	Received data can be read
	OER, FER, PER, SUM	Error flags
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to "101_2"
	CKDIR	Set to "0"
	STPS	Set to "0"
	PRY	Set to "1" for direct format or "0" for inverse format
	PRYE	Set to "1"
	IOPOL	Set to "0"
UiC0	CLK1 to CLK0	Select count source for the UiBRG register
	CRS	Disabled because CRD=1
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Set to "1"
	CKPOL	Set to "0"
	UFORM	Set to "0" for direct format or "1" for inverse format
UiC1	TE	Set to "1" to enable data transmission
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Set to "1"
	UiRRM	Set to "0"
	UiLCH	Set to "0" for direct format or "1" for inverse format
	UiERE	Set to "1"
UiSMR	0 to 3	Set to "00_{16}"
UiSMR2	0 to 7	Set to "00_{16}"
UiSMR3	0 to 7	Set to "00_{16}"
UiSMR4	0 to 7	Set to "00_{16}"

i=0 to 4

Table 16.35 Pin Settings in SIM Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

Table 16.36 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70(1)	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71(1)	RxD2 input	PS1_1=0	–	–	PD7_1=0

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 16.37 Pin Settings (3)

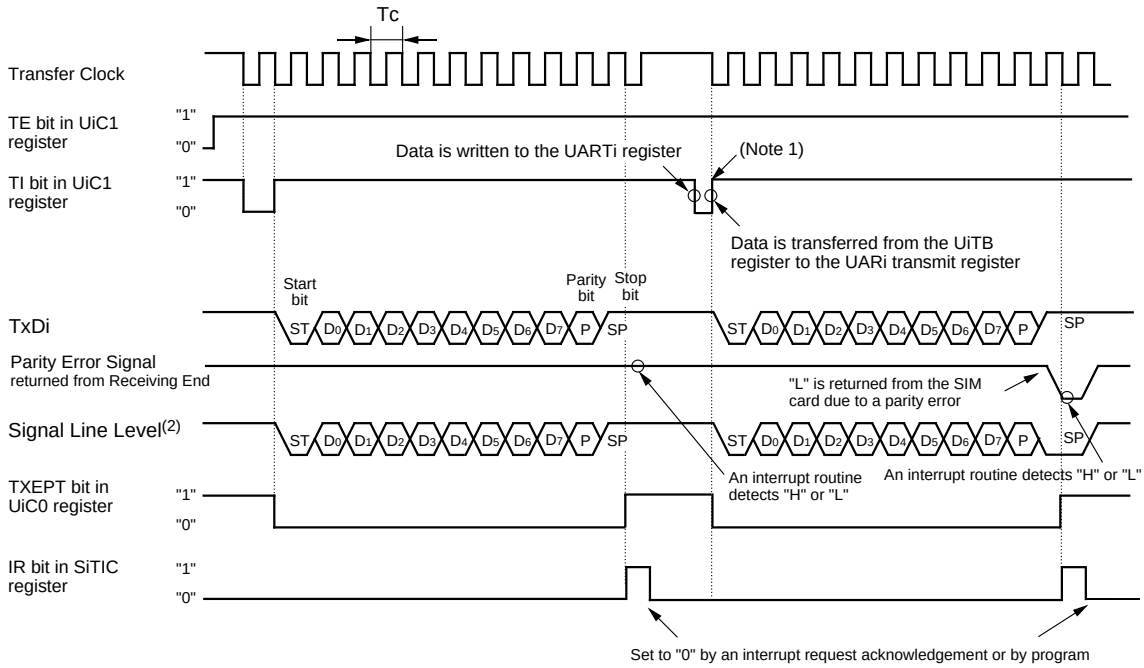
Port	Function	Setting		
		PS3 Register(1)	PSL3 Register	PD9 Register(1)
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

Figure 16.29 shows an example of a SIM interface operation. Figure 16.30 shows an example of a SIM interface connection. Connect TxDi to RxDi for a pull-up.

(1) Transmit Timing



i=0 to 4

The above applies to the following settings :

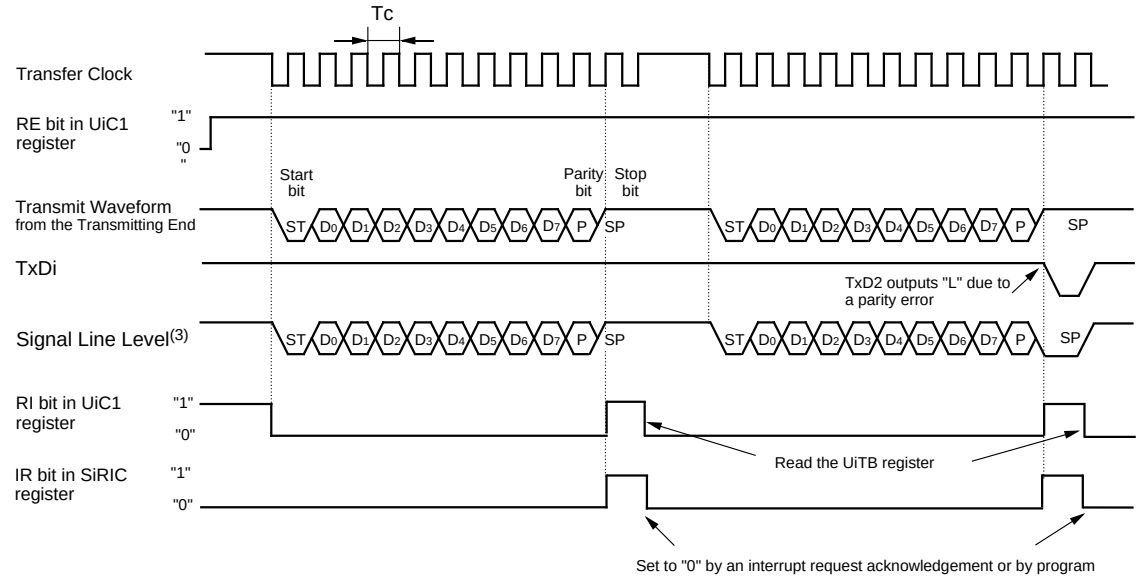
- The PRYE bit in the UiMR register is set to "1" (parity enabled)
- The STPS bit in the UiMR register is set to "0" (1 stop bit)
- The UiIRS bit in the UiC1 register is set to "1" (interrupt request generated when transmission completed)

Tc = 16(m+1) / fj

fj : frequency of UiBRG count source (f_1, f_8, f_{2n}(4))

m : setting value of UiBRG

(2) Receive Timing



i=0 to 4

The above applies to the following settings :

- The PRYE bit in the UiMR register is set to "1" (parity enabled)
- The STPS bit in the UiMR register is set to "0" (1 stop bit)
- The UiIRS bit in the UiC1 register is set to "1" (interrupt request generated when transmission completed)

Tc = 16(m+1) / fj

fj : frequency of UiBRG count source (f_1, f_8, f_{2n}(4))

m : setting value of UiBRG

NOTES:

1. Data transmission starts when BRG overflows after a value is set to the UiTB register on the rising edge of the TI bit.
2. Because TxDi and RxDi are connected, a composite waveform, consisting of transmit waveform from TxDi and parity error signal from the receiving end, is generated.
3. Because TxDi and RxDi are connected, a composite waveform, consisting of transmit waveform from the transmitting end and parity error signal from TxDi, is generated.
4. The CNT3 to CNT0 bits in the TCSPR register selects no division (n=0) or divide-by-2n (n=1 to 15).

Figure 16.29 SIM Interface Operation

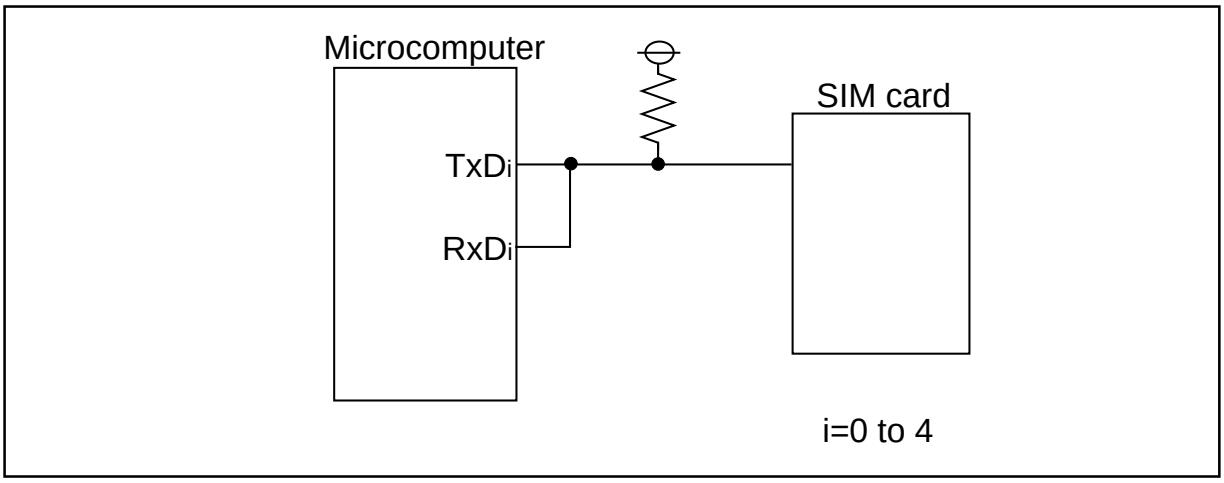


Figure 16.30 SIM Interface Connection

16.7.1 Parity Error Signal

16.7.1.1 Parity Error Signal Output Function

When the UiERE bit in the UiC1 register (i=0 to 4) is set to "1", the parity error signal can be output. The parity error signal is output when a parity error is detected upon receiving data. TxDi outputs an "L" signal in the timing shown in Figure 16.31. When reading the UiRB register during a parity error output, the PER bit in the UiRB register is set to "0" and TxDi again outputs an "H" signal simultaneously.

16.7.1.2 Parity Error Signal

To determine whether the parity error signal is output, the port that shares a pin with RxDi is read by using a transmit complete interrupt routine.

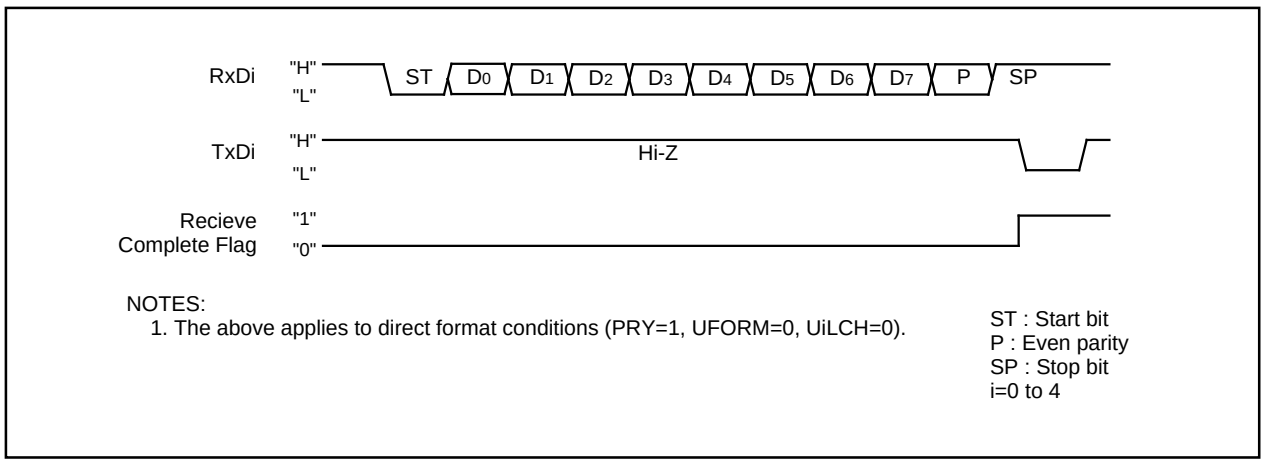


Figure 16.31 Parity Error Signal Output Timing (LSB First)

16.7.2 Format

16.7.2.1 Direct Format

Set the PRYE bit in the UiMR register (i=0 to 4) to "1", the PRY bit to "1", the UFORM bit in the UiC0 register to "0" and the UiLCH bit in the UiC1 register to "0". When data are transmitted, data set in UiTB register are transmitted with the even-numbered parity, starting from D_0. When data are received, received data are stored in the UiRB register, starting from D_0. The even-numbered parity determines whether a parity error occurs.

16.7.2.2 Inverse Format

Set the PRYE bit to "1", the PRY bit to "0", the UFORM bit to "1" and the UiLCH bit to "1". When data are transmitted, values set in the UiTB register are logically inversed and are transmitted with the odd-numbered parity, starting from D_7. When data are received, received data are logically inversed to be stored in the UiRB register, starting from D_7. The odd-numbered parity determines whether a parity error occurs.

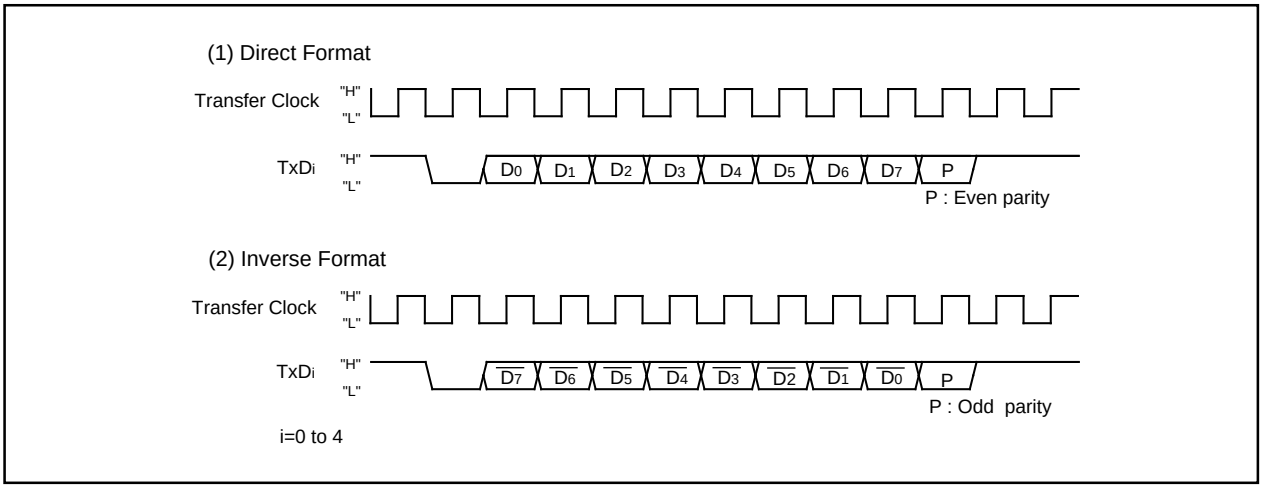


Figure 16.32 SIM Interface Format

17. A/D Converter

The A/D converter consists of two 10-bit successive approximation A/D converters, each with a capacitive coupling amplifier.

The result of an A/D conversion is stored into the A/D register corresponding to selected pins.

Table 17.1 lists specifications of the A/D converter. Figure 17.1 shows a block diagram of the A/D converter. Table 17.2 lists the differences between A/D0 and A/D1 conversions, which share the same conversion method. A/D0 and A/D1 can perform conversions simultaneously. Table 17.3 lists settings of the following pins; AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1 and $\overline{ADTRG}$. Figures 17.2 to 17.7 show registers associated with the A/D converter.

NOTE

In this section, the 144-pin package is given as the example.
The $AN15_0$ to $AN15_7$ pins are not included in the 100-pin package.

Table 17.1 A/D Converter Specifications

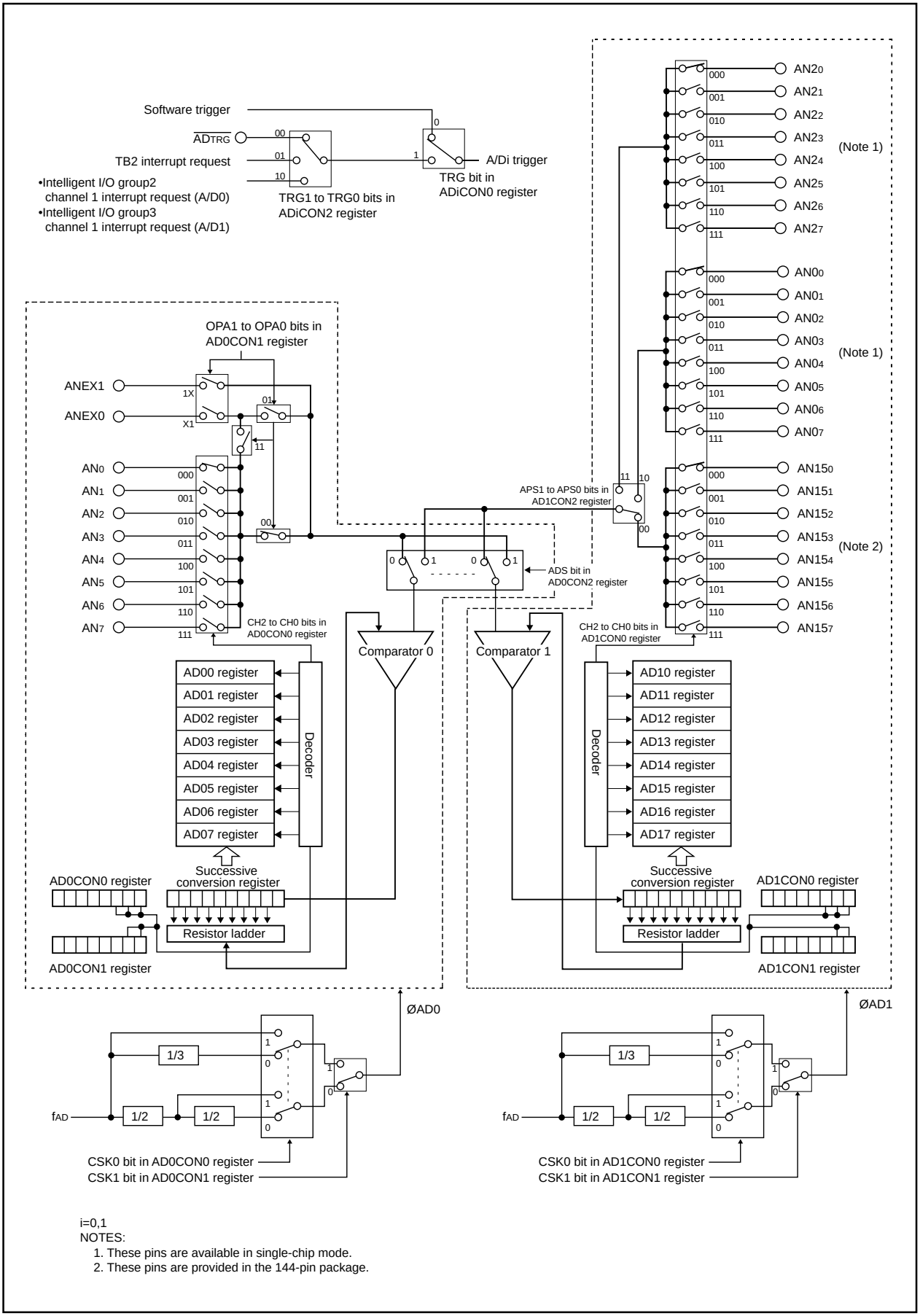
Item	Specification
A/D Conversion Method	Successive approximation (with a capacitive coupling amplifier)
Analog Input Voltage(1)	0V to AVCC (VCC)
Operating Clock, ØAD(2)	fAD, fAD/2, fAD/3, fAD/4
Resolution	Select from 8 bits or 10 bits
Operating Mode	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, repeat sweep mode 1
Analog Input Pins	34 pins 8 pins each for AN (AN0 to AN7), AN0 (AN00 to AN07), AN2 (AN20 to AN27), AN15 (AN150 to AN157) 2 extended input pins (ANEX0 and ANEX1)
A/D Conversion Start Condition	Software trigger • The ADST bit in the ADiCON0 (i=0, 1) register is set to "1" (A/D conversion started) by program • The PST bit in the AD0CON2 register is set to "1" (A/D0 and A/D1 start a conversion simultaneously) by program External trigger (re-trigger is enabled) When a falling edge is applied to the $\overline{\text{ADTRG}}$ pin after the ADST bit is set to "1" by program Hardware trigger (re-trigger is enabled) One of the following interrupt requests is generated after the ADST bit is set to "1" by program: • The timer B2 interrupt request of the three-phase motor control timer functions (after the ICTB2 counter completes counting) • The intelligent I/O interrupt request Channel 1 in the group 2 (A/D0), channel 1 in the group 3 (A/D1)
Conversion Rate Per Pin	• Without the sample and hold function 8-bit resolution : 49 ØAD cycles 10-bit resolution : 59 ØAD cycles • With the sample and hold function 8-bit resolution : 28 ØAD cycles 10-bit resolution : 33 ØAD cycles

NOTES:
1. Analog input voltage is not affected by the sample and hold function status.
2. ØAD frequency must be under 16 MHz when VCC=5V.
   ØAD frequency must be under 10 MHz when VCC=3.3V.
   Without the sample and hold function, the ØAD frequency must be 250 kHz or more.
   With the sample and hold function, the ØAD frequency must be 1 MHz or more.

Table 19.2 Difference between A/D0 and A/D1

Item	A/D0	A/D1
Analog Input Pins(1)	AN (AN0 to AN7)	Select from AN0 (AN00 to AN07), AN2 (AN20 to AN27) or AN15 (AN150 to AN157)
Extended Analog Input Pins	ANEX0, ANEX1	Not provided
External Op-Amp(1)	Enabled	Disabled
Intelligent I/O used as a Trigger	Channel 1 in group 2	Channel 1 in group 3

NOTES:
1. When the ADS bit in the AD0CON2 register is set to "0" (channel replacement disabled)



i=0,1
NOTES:
1. These pins are available in single-chip mode.
2. These pins are provided in the 144-pin package.

Figure 17.1 A/D Converter Block Diagram

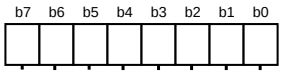
Table 17.3 Pin Settings

Port Name	Function		Bit and Setting		
		PD10, PD0, PD2, PD15, PD9(3) Registers	PS3(3), PS9 Registers	PSL3, IPS Registers	PUR0, PUR3, PUR4 Registers
P10$_0$	AN$_0$	PD10_0 = 0	-	-	PU30 = 0
P10$_1$	AN$_1$	PD10_1 = 0			
P10$_2$	AN$_2$	PD10_2 = 0			
P10$_3$	AN$_3$	PD10_3 = 0			
P10$_4$	AN$_4$	PD10_4 = 0			PU31 = 0
P10$_5$	AN$_5$	PD10_5 = 0			
P10$_6$	AN$_6$	PD10_6 = 0			
P10$_7$	AN$_7$	PD10_7 = 0			
P0$_0$	AN0$_0$(1)	PD0_0 = 0	-	-	PU00 = 0
P0$_1$	AN0$_1$(1)	PD0_1 = 0			
P0$_2$	AN0$_2$(1)	PD0_2 = 0			
P0$_3$	AN0$_3$(1)	PD0_3 = 0			
P0$_4$	AN0$_4$(1)	PD0_4 = 0			PU01 = 0
P0$_5$	AN0$_5$(1)	PD0_5 = 0			
P0$_6$	AN0$_6$(1)	PD0_6 = 0			
P0$_7$	AN0$_7$(1)	PD0_7 = 0			
P2$_0$	AN2$_0$(1)	PD2_0 = 0	-	-	PU04 = 0
P2$_1$	AN2$_1$(1)	PD2_1 = 0			
P2$_2$	AN2$_2$(1)	PD2_2 = 0			
P2$_3$	AN2$_3$(1)	PD2_3 = 0			
P2$_4$	AN2$_4$(1)	PD2_4 = 0	-	-	PU05 = 0
P2$_5$	AN2$_5$(1)	PD2_5 = 0			
P2$_6$	AN2$_6$(1)	PD2_6 = 0			
P2$_7$	AN2$_7$(1)	PD2_7 = 0			
P15$_0$	AN15$_0$(2)	PD15_0 = 0	PS9_0 = 0	IPS2 = 1	PU42 = 0
P15$_1$	AN15$_1$(2)	PD15_1 = 0	PS9_1 = 0		
P15$_2$	AN15$_2$(2)	PD15_2 = 0	-		
P15$_3$	AN15 $_3$(2)	PD15_3 = 0	-		
P15$_4$	AN15$_4$(2)	PD15_4 = 0	PS9_4 = 0		PU43 = 0
P15$_5$	AN15$_5$(2)	PD15_5 = 0	PS9_5 = 0		
P15$_6$	AN15$_6$(2)	PD15_6 = 0	-		
P15$_7$	AN15$_7$(2)	PD15_7 = 0	-		
P9$_5$	ANEX0	PD9_5 = 0	PS3_5 = 0	PSL3_5 = 1	PU27 = 0
P9$_6$	ANEX1	PD9_6 = 0	PS3_6 = 0	PSL3_6 = 1	
P9$_7$	$\overline{\text{ADTRG}}$	PD9_7 = 0	PS3_7 = 0	-	-

NOTES:

1. This pin is available in single-chip mode.
2. This pin is provided in the 144-pin package.
3. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

A/D0 Control Register 0(1)



Symbol	Address	After Reset
AD0CON0	039616	0016

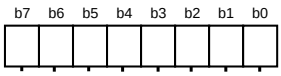
Bit Symbol	Bit Name	Function	RW
CH0	Analog Input Pin Select Bit(2, 3, 4)	b2 b1 b0 0 0 0 : AN0 0 0 1 : AN1 0 1 0 : AN2 0 1 1 : AN3 1 0 0 : AN4 1 0 1 : AN5 1 1 0 : AN6 1 1 1 : AN7	RW
CH1			RW
CH2			RW
MD0	A/D Operation Mode Select Bit 0(2)	b4 b3 0 0 : One-shot mode 0 1 : Repeat mode 1 0 : Single sweep mode 1 1 : Repeat sweep mode 0 or 1	RW
MD1			RW
TRG	Trigger Select Bit	0 : Software trigger 1 : External trigger, hardware trigger(5)	RW
ADST	A/D Conversion Start Flag	0 : A/D conversion stops 1 : A/D conversion starts(5)	RW
CKS0	Frequency Select Bit(6)	0 : Select from fAD/3 or fAD/4 1 : Select from fAD/1 or fAD/2	RW

NOTES:
1. When the AD0CON0 register is rewritten during the A/D conversion, the conversion result is indeterminate.
2. Analog input pins must be set again after changing A/D operation mode.
3. This bit is disabled in single sweep mode, repeat sweep mode 0 and repeat sweep mode 1.
4. Set the PSC_7 bit in the PSC register to "1" (AN4 to AN7) to use the P10 pin as a analog input pin.
5. To set the TRG bit to "1", select the cause of trigger by setting the TRG1 and TRG0 bits in the AD0CON2 register. Then set the ADST bit to "1" after the TRG bit is set to "1".
6. ∅AD frequency must be under 16 MHz when VCC=5V.
   ∅AD frequency must be under 10 MHz when VCC=3.3V.
   Combination of CKS0 and CKS1 bits selects ∅AD.

CKS0	CKS1	∅AD
0	0	fAD divided by 4
0	1	fAD divided by 3
1	0	fAD divided by 2
1	1	fAD

Figure 17.2 AD0CON0 Register

A/D0 Control Register 1(1)



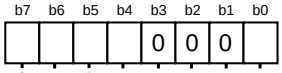
Symbol	Address	After Reset
AD0CON1	039716	0016

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D Sweep Pin Select Bit(2)	b0 b1 0 0 : AN0, AN1 (AN0) 0 1 : AN0 to AN3 (AN0, AN1) 1 0 : AN0 to AN5 (AN0 to AN2) 1 1 : AN0 to AN7 (AN0 to AN3)	RW
SCAN1			RW
MD2	A/D Operation Mode Select Bit 1	0 : Any mode other than repeat sweep mode 1 1 : Repeat sweep mode 1	RW
BITS	8/10-bit Mode Select Bit	0 : 8-bit mode 1 : 10-bit mode	RW
CKS1	Frequency Select Bit(3)	0 : Select from fAD/2 or fAD/4 1 : Select from fAD/1 or fAD/3	RW
VCUT	VREF Connection Bit	0 : No VREF connection(4) 1 : VREF connection	RW
OPA0	External Op-Amp Connection Mode Bit(5)	b6 b7 0 0 : ANEX0 and ANEX1 are not used(6) 0 1 : Signal into ANEX0 is A/D converted 1 0 : Signal into ANEX1 is A/D converted 1 1 : External op-amp connection mode	RW
OPA1			RW

NOTES:
1. When the AD0CON1 register is rewritten during the A/D conversion, the conversion result is indeterminate.
2. This bit is disabled in one-shot mode and repeat mode. Pins in parentheses are those most commonly used in the A/D conversions when the MD2 bit is set to "1".
3. ∅AD frequency must be under 16 MHz when VCC=5V. ∅AD frequency must be under 10 MHz when VCC=3.3V. Combination of the CKS0 and CKS1 bits selects ∅AD (see the AD0CON0 register).
4. Do not set the VCUT bit to "0" during the A/D conversion. This is a reference voltage for the A/D0. It does not affect D/A conversion.
5. In single sweep mode and repeat sweep mode 0 or 1, the OPA1 and OPA0 bits cannot be set to "01_2"or "10_2".
6. When the OPA1 to OPA0 bits is set to "00_2", set the PSL3_5 bit in PSL3 register to "0" (other than ANEX0) and the PSL3_6 bit to "0" (other than ANEX1).

Figure 17.3 AD0CON1 Register

A/D0 Control Register 2(1)

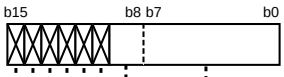


Symbol	Address	After Reset
AD0CON2	0394_{16}	$X000\ 0000_2$

Bit Symbol	Bit Name	Function	RW
SMP	A/D Conversion Method Select Bit	0 : Without the sample and hold function 1 : With the sample and hold function	RW
—— (b3 - b1)	Reserved Bit	Set to "0"	RW
ADS	A/D Channel Replace Select Bit(2)	0 : Disables channel replacement 1 : Enables channel replacement(5)	RW
TRG0	External Trigger Request Cause Select Bit	b6 b5 0 0 : Selects $\overline{\text{ADTRG}}$ 0 1 : Selects a timer B2 interrupt request of the three-phase motor control timer functions (after ICTB2 counter completes counting) 1 0 : Selects the intelligent I/O group 2 channel 1 interrupt 1 1 : Do not set to this value	RW
TRG1			RW
PST	Simultaneous Start Bit(2, 3, 4)	When this bit is set to "1", A/D0 and A/D1 start conversions simultaneously. When read, its content is indeterminate.	WO

NOTES:
1. When the AD0CON2 register is rewritten during the A/D conversion, the conversion result is indeterminate.
2. Do not set the APS1 and APS0 bits to "1" while either A/D0 or A/D1 is operating.
3. The PST bit is enabled when the TRG bit in the AD0CON0 register is set to "0" (software trigger). Do not set the PST bit to "1" when the TRG bit is set to "1" (external trigger).
4. Set both A/D0 and A/D1 to the same setting.
5. If the ADS bit is set to "1", do not select single sweep mode or repeat sweep mode as the A/D operation mode.

A/D0 Register i (i =0 to 7)



Symbol	Address	After Reset
AD00 to AD02	0381_{16} - 0380_{16}, 0383_{16} - 0382_{16}, 0385_{16} - 0384_{16}	Indeterminate
AD03 to AD05	0387_{16} - 0386_{16}, 0389_{16} - 0388_{16}, $038B_{16}$ - $038A_{16}$	Indeterminate
AD06 to AD07	$038D_{16}$ - $038C_{16}$, $038F_{16}$ - $038E_{16}$	Indeterminate

Function	RW
8 low-order bits in an A/D conversion result	RO
In 10-bit mode : 2 high-order bits in an A/D conversion result In 8-bit mode : When read, its contents is indeterminate.	RO
Nothing is assigned. When write, set to "0". When read, its content is indeterminate.	—

Figure 17.4 AD0CON2 Register, AD00 to AD07 Registers

A/D1 Control Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
AD1CON0	01D6₁₆	00₁₆

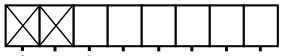
Bit Symbol	Bit Name	Function	RW
CH0	Analog Input Pin Select Bit(2, 3, 4, 5, 6)	b2 b1 b0 0 0 0 : ANi0 0 0 1 : ANi1 0 1 0 : ANi2 0 1 1 : ANi3 1 0 0 : ANi4 1 0 1 : ANi5 1 1 0 : ANi6 1 1 1 : ANi7 (i=0, 2, 15)	RW
CH1			RW
CH2			RW
MD0	A/D Operation Mode Select Bit 0(2)	b4 b3 0 0 : One-shot mode 0 1 : Repeat mode 1 0 : Single sweep mode 1 1 : Repeat sweep mode 0 or 1	RW
MD1			RW
TRG	Trigger Select Bit	0 : Software trigger 1 : External trigger, hardware trigger(7)	RW
ADST	A/D Conversion Start Flag	0 : A/D conversion stops 1 : A/D conversion starts(7)	RW
CKS0	Frequency Select Bit(8)	0 : Select from f_{AD}/3 or f_{AD}/4 1 : Select from f_{AD}/1 or f_{AD}/2	RW

NOTES:
1. When the AD1CON0 register is rewritten during the A/D conversion, the conversion result is indeterminate.
2. Set analog input pins again after changing A/D operation mode.
3. This bit is disabled in single sweep mode, repeat sweep mode 0 and repeat sweep mode 1.
4. The APS1 to APS0 bit in the AD1CON2 register select i=0, 2 or 15.
5. i=0 or 2 is available in single-chip mode only.
6. i=15 is available in the 144-pin package.
7. To set the TRG bit to "1", select the cause of trigger by setting the the TRG1 and TRG0 bits in the AD1CON2 register. Then set the ADST bit to "1" after the TRG bit is set to "1".
8. $\varnothing_{AD}$ frequency must be under 16 MHz when V_{CC}=5V.
   $\varnothing_{AD}$ frequency must be under 10 MHz when V_{CC}=3.3V.
   Combination of the CKS0 and CKS1 bits selects $\varnothing_{AD}$.

CKS0	CKS1	$\varnothing_{AD}$
0	0	f_{AD} divided by 4
0	1	f_{AD} divided by 3
1	0	f_{AD} divided by 2
1	1	f_{AD}

Figure 17.5 AD1CON0 Register

A/D1 Control Register 1(1)



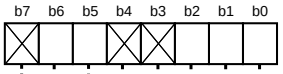
Symbol	Address	After Reset
AD1CON1	$01D7_{16}$	$XX00\ 0000_2$

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D Sweep Pin Select Bit(2, 3, 4)	b1 b0 0 0 : ANi0,ANi1 (ANi0) 0 1 : ANi0 to ANi3 (ANi0,ANi1) 1 0 : ANi0 to ANi5 (ANi0 to ANi2) 1 1 : ANi0 to ANi7 (ANi0 to ANi3) (i=0, 2, 15)	RW
SCAN1			RW
MD2	A/D Operation Mode Select Bit 1	0 : Any mode other than repeat sweep mode 1 1 : Repeat sweep mode 1	RW
BITS	8/10-bit Mode Select Bit	0 : 8-bit mode 1 : 10-bit mode	RW
CKS1	Frequency Select Bit(5)	0 : Select from $f_{AD}/2$ or $f_{AD}/4$ 1 : Select from $f_{AD}/1$ or $f_{AD}/3$	RW
VCUT	V_{REF} Connection Bit	0 : V_{REF} not connected(6) 1 : V_{REF} connected	RW
____ (b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

NOTES:
1. When the AD1CON1 register is rewritten during the A/D conversion, the conversion result is indeterminate.
2. This bit is disabled in one-shot mode and repeat mode. Pins in parentheses are those most commonly used for A/D conversions when the MD2 bit is set to "1" (repeat sweep mode 1).
3. The APS1 to APS0 bits in the AD1CON2 register select i=0, 2 or 15.
4. i=15 is available in the 144-pin package.
5. $\varnothing_{AD}$ frequency must be under 16 MHz when V_{CC}=5V. $\varnothing_{AD}$ frequency must be under 10 MHz when V_{CC}=3.3V. Combination of the CKS0 and CKS1 bits selects $\varnothing_{AD}$ (see the AD1CON0 register).
6. Do not set the VCUT bit to "0" during the A/D conversion. This is a reference voltage for the A/D1. It does not affect the D/A conversion.

Figure 17.6 AD1CON1 Register

A/D1 Control Register 2(1)

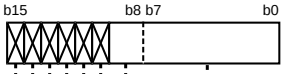


Symbol	Address	After Reset
AD1CON2	$01D4_{16}$	X00X X000$_2$

Bit Symbol	Bit Name	Bit name	RW
SMP	A/D Conversion Method Select Bit	0 : Without the sample and hold function 1 : With the sample and hold function	RW
APS0	Analog Input Port Select Bit	b2 b1 0 0 : $AN15_0$ to $AN15_7$(2) 0 1 : Do not set to this value 1 0 : $AN0_0$ to $AN0_7$(3) 1 1 : $AN2_0$ to $AN2_7$(3)	RW
APS1			RW
____ (b4 - b3)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
TRG0	External Trigger Request Cause Select Bit	b6 b5 0 0 : Selects $\overline{ADTRG}$ 0 1 : Selects a timer B2 interrupt request of the three-phase motor control timer functions (after the ICTB2 counter completes counting) 1 0 : Selects the Intelligent I/O group 3 channel 1 interrupt 1 1 : Do not set to this value	RW
TRG1			RW
____ (b7)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. When the AD1CON2 register is rewritten during the A/D conversion, the conversion result is indeterminate.
2. $AN15_0$ to $AN15_7$ are provided in the 144-pin package.
3. AN00 to AN07, AN20 to AN27 are available in single-chip mode only.

A/D1 Register j (j=0 to 7)



Symbol	Address	After Reset
AD10 to AD12	$01C1_{16}$ - $01C0_{16}$, $01C3_{16}$ - $01C2_{16}$, $01C5_{16}$ - $01C4_{16}$	Indeterminate
AD13 to AD15	$01C7_{16}$ - $01C6_{16}$, $01C9_{16}$ - $01C8_{16}$, $01CB_{16}$ - $01CA_{16}$	Indeterminate
AD16 to AD17	$01CD_{16}$ - $01CC_{16}$, $01CF_{16}$ - $01CE_{16}$	Indeterminate

Function	RW
8 low-order bits in an A/D conversion result	RO
In 10-bit mode : 2 high-order bits in an A/D conversion result In 8-bit mode : When read, its content is indeterminate.	RO
Nothing is assigned. When write, set to "0". When read, its content is indeterminate.	—

Figure 17.7 AD1CON2 Register, AD10 to AD17 Register

17.1 Mode Description

17.1.1 One-shot Mode

In one-shot mode, analog voltage applied to a selected pin is converted to a digital code once. Table 17.4 lists specifications of one-shot mode.

Table 17.4 One-shot Mode Specifications

Item	Specification
Function	Analog voltage, applied to a pin selected by the CH2 to CH0 bits in the ADiCON0 register (i=0, 1), is converted to a digital code once.
Start Condition	When the TRG bit in the ADiCON0 register is set to "0" (software trigger), • The ADST bit in the ADiCON0 register is set to "1" (A/D conversion starts) by program • The PST bit in the AD0CON2 register is set to "1" (A/D0 and A/D1 start a conversion simultaneously) by program When the TRG bit is set to "1" (external trigger, hardware trigger), • When a falling edge is applied to the $\overline{\text{ADTRG}}$ pin after the ADST bit is set to "1" by program • One of the following interrupt requests is generated after the ADST bit is set to "1" by program: The timer B2 interrupt request of three-phase motor control timer functions (after the ICTB2 counter completes counting) is generated The intelligent I/O interrupt request is generated Channel 1 in the group 2 (A/D0), channel 1 in the group 3 (A/D1)
Stop Condition	• A/D conversion is completed (the ADST bit is set to "0" when the internal trigger is selected) • The ADST bit is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	A/D conversion is completed
Analog Voltage Input Pins	Select one pin from AN_0 to AN_7, ANEX0, or ANEX1 Select one pin from ANj_0 to ANj_7, (j=0, 2, 15)
Reading of A/D Conversion Result	The ADik register (k=0 to 7) corresponding to selected pin

17.1.2 Repeat Mode

In repeat mode, analog voltage applied to a selected pin is repeatedly converted to a digital code. Table 17.5 lists specifications of repeat mode.

Table 17.5 Repeat Mode Specifications

Item	Specification
Function	Analog voltage, applied to a pin selected by the CH2 to CH0 bits in the ADiCON0 register (i=0, 1), is converted to a digital code once.
Start Condition	Same as one-shot mode
Stop Condition	The ADST bit in the ADiCON0 register is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	Not generated
Analog Voltage Input Pins	Select one pin from AN_0 to AN_7, ANEX0, or ANEX1 Select one pin from ANj_0 to ANj_7 (j=0, 2, 15)
Reading of A/D Conversion Result	The ADik register (k=0 to 7) corresponding to selected pins

17.1.3 Single Sweep Mode

In single sweep mode, analog voltage that is applied to selected pins is converted one-by-one to a digital code. Table 17.6 lists specifications of single sweep mode.

Table 17.6 Single Sweep Mode Specifications

Item	Specification
Function	Analog voltage, applied to pins selected by the SCAN1 to SCAN0 bits in the ADiCON0 register (i=0, 1), are converted one-by-one to a digital code
Start Condition	Same as one-shot mode
Stop Condition	• A/D conversion is completed (the ADST bit in the ADiCON0 register is set to "0" when the internal trigger is selected) • The ADST bit is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	Sweep operation is completed
Analog Voltage Input Pins	Select from AN0 to AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), or AN0 to AN7 (8 pins) Select from ANj0 (j=0, 2, 15) to ANj1 (2 pins), ANj0 to ANj3 (4 pins), ANj0 to ANj5 (6 pins), or ANj0 to ANj7 (8 pins)
Reading of A/D Conversion Result	The ADik register (k=0 to 7) corresponding to selected pins

17.1.4 Repeat Sweep Mode 0

In repeat sweep mode 0, analog voltage applied to selected pins is repeatedly converted to a digital code. Table 17.7 lists specifications of repeat sweep mode 0.

Table 17.7 Repeat Sweep Mode 0 Specifications

Item	Specification
Function	Analog voltage, applied to pins selected by the SCAN1 to SCAN0 bits in the ADiCON0 register (i=0, 1), are repeatedly converted to a digital code
Start Condition	Same as one-shot mode
Stop Condition	The ADST bit in the ADiCON0 register is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	Not generated
Analog Voltage Input Pins	Select from AN0 to AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), or AN0 to AN7 (8 pins) Select from ANj0 (j=0, 2, 15) to ANj1 (2 pins), ANj0 to ANj3 (4 pins), ANj0 to ANj5 (6 pins), or ANj0 to ANj7 (8 pins)
Reading of A/D Conversion Result	The ADik register (k=0 to 7) corresponding to selected pins

17.1.5 Repeat Sweep Mode 1

In repeat sweep mode 1, analog voltage selectively applied to eight pins is repeatedly converted to a digital code. Table 17.8 lists specifications of repeat sweep mode 1.

Table 17.8 Repeat Sweep Mode 1 Specifications

Item	Specification
Function	Analog voltage selectively applied to 8 pins selected by the SCAN1 to SCAN0 bits in the ADiCON1 register (i=0,1) is repeatedly converted to a digital code. e.g., When ANj0 is selected (j =none, 0, 2, 15), analog voltage is converted to a digital code in the following order: ANj0→ ANj1→ ANj0→ ANij2→ ANj0 →ANj3 ..... etc.
Start Condition	Same as one-shot mode
Stop Condition	The ADST bit in the ADiCON1 register is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	Not generated
Analog Voltage Input Pins	ANj0 to ANj7 (8 pins)
Prioritized Pins	Select from AN0, AN0 to AN1 (2 pins), AN0 to AN2 (3 pins), or AN0 to AN3 (4 pins) Select from ANj0 (j=0, 2, 15), ANj0 to ANj1 (2 pins), ANj0 to ANj2 (3 pins), or ANj0 to ANj3 (4 pins)
Reading of A/D Conversion Result	The ADik register (k=0 to 7) corresponding to selected pins

17.2 Function

17.2.1 Resolution Select Function

The BITS bit in the ADiCON1 (i=0, 1) register determines the resolution. When the BITS bit is set to "1" (10-bit precision), the A/D conversion result is stored into bits 0 to 9 in the ADij register (j = 0 to 7). When the BITS bit is set to "0" (8-bit precision), the A/D conversion result is stored into bits 0 to 7 in the ADij register.

17.2.2 Sample and Hold

When the SMP bit in the ADiCON2 register is set to "1" (with the sample and hold function), A/D conversion rate per pin increases to 28 ØAD cycles for 8-bit resolution and 33 ØAD cycles for 10-bit resolution. The sample and hold function is available in all operating modes. Start the A/D conversion after selecting whether the sample and hold circuit is to be used or not.

17.2.3 Trigger Select Function

The TRG bit in the ADiCON0 register and the TRG1 to TRG0 bits in the ADiCON2 register determine the trigger to start the A/D conversion. Table 17.9 lists settings of the trigger select function.

Table 17.9 Trigger Select Function Settings

Bit and Setting		Trigger
ADiCON0 Register	ADiCON2 Register	
TRG = 0	-	Software trigger The A/Di starts the A/D conversion when the ADST bit in the ADiCON0 register is set to "1"
	-	Two-circuit simultaneous start A/D0 and A/D1 start the A/D conversion simultaneously when the PST bit in the AD0CON2 register is set to "1" by program (Refer to 17.2.4 Two-Circuit Simultaneous Start)
TRG = 1(1)	TRG1 to TRG0 = 00_2	External trigger(2) Falling edge of a signal applied to $\overline{ADTRG}$
	TRG1 to TRG0 = 01_2	Hardware trigger(2) The timer B2 interrupt request of three-phase motor control timer functions (after the ICTB2 counter completes counting)
	TRG1 to TRG0 = 10_2	Hardware trigger(2) The intelligent I/O interrupt request is generated Channel 1 in the group 2 (A/D0), channel 1 in the group 3 (A/D1)

i= 0,1

NOTES:

1. The A/Di starts the A/D conversion when the ADST bit is set to "1" (A/D conversion started) and a trigger is generated.
2. The A/D conversion is restarted if an external trigger or a hardware trigger is inserted during an A/D conversion. (The A/D conversion in process is aborted.)

17.2.4 Two-Circuit Simultaneous Start (Software Trigger)

A/D0 and A/D1 start simultaneously when the PST bit in the AD0CON2 register is set to "1" (two-circuit simultaneous start).

Do not set the PST bit to "1" while either A/D0 or A/D1 is performing an A/D conversion, or if the TRG bit is set "1" (external trigger).

Do not set the ADST bit to "1" (A/D conversion started) when using the PST bit.

17.2.5 Pin Input Replacement Function

When the ADS bit in the AD0CON2 register is set to "1" (channel replacement enabled), channels of the A/D0 can be replaced with channels of the A/D1 and vice versa.

Voltage applied to the ANj (j = 0 to 7) pin is converted to digital code in the A/D1 and the conversion result is stored into the AD1j register. Voltage applied to the AN0j, AN2j or AN15j pin is converted to digital code in the A/D0 and the conversion results are stored into the AD0j register.

To set the ADS bit to "1", set the MD1 to MD0 bits in the AD0CON0 register to "00_2" (one-shot mode) or "01_2" (repeat mode). Single sweep, repeat sweep 0, and repeat sweep 1 modes cannot be used. Set the OPA1 to OPA0 bits in the AD0CON1 register to "00_2" (no ANEX0 and ANEX1 used). Set the same value to both AD0CON0 register and AD1CON0 register, and to both AD0CON1 register and AD1CON1 register.

17.2.6 Extended Analog Input Pins

In one-shot mode and repeat mode, the ANEX0 and ANEX1 pins can be used as analog input pins. The OPA1 to OPA0 bits in the AD0CON1 register select which pins to use as analog input pins. An A/D conversion result for the ANEX0 pin is stored into the AD00 register. The result for the ANEX1 pin is stored into the AD01 register.

17.2.7 External Operation Amplifier (Op-Amp) Connection Mode

In external op-amp connection mode, multiple analog voltage can be amplified by one external op-amp using extended analog input pins ANEX0 and ANEX1.

When the OPA1 to OPA0 bits in the AD0CON1 register are set to "11$_2$" (external op-amp connection), voltage applied to the AN$_0$ to AN$_7$ pins are output from ANEX0. Amplify this output signal by an external op-amp and apply it to ANEX1.

Analog voltage applied to ANEX1 is converted to a digital code and the A/D conversion result is stored into the corresponding ADij register (i=0, 1; j=0 to 7). A/D conversion rate varies depending on the response of the external op-amp. Do not connect the ANEX0 pin to the ANEX1 pin directly.

Figure 17.8 shows an example of an external op-amp connection.

Table 17.10 Extended Analog Input Pin Settings

AD0CON1 Register		ANEX0 Function	ANEX1 Function
OPA1	OPA0		
0	0	Not used	Not used
0	1	P9$_5$ as an analog input	Not used
1	0	Not used	P9$_6$ as an analog input
1	1	Output to an external op-amp	Input from an external op-amp

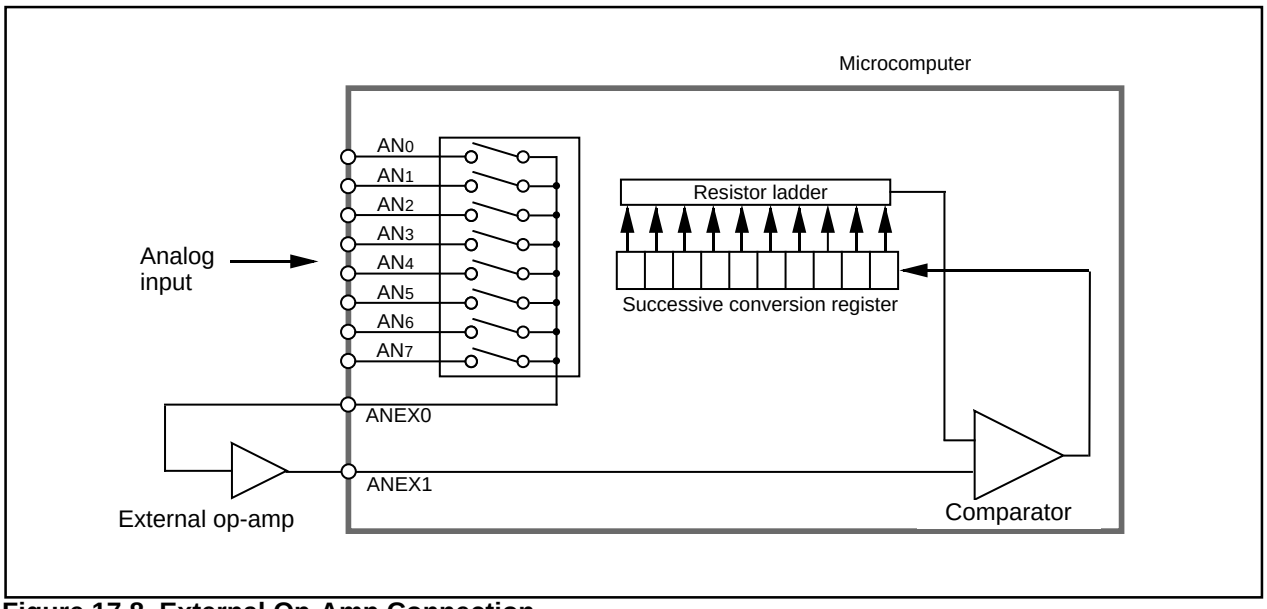


Figure 17.8 External Op-Amp Connection

17.2.8 Power Consumption Reducing Function

When the A/D converter is not used, the VCUT bit in the ADiCON1 register (i=0, 1) isolates the resistor ladder of the A/D converter from the reference voltage input pin (VREF). Power consumption is reduced by shutting off any current flow into the resistor ladder from the VREF pin.

When using the A/D converter, set the VCUT bit to "1" (VREF connection) before setting the ADST bit in the ADiCON0 register to "1" (A/D conversion started). Do not set the ADST bit and VCUT bit to "1" simultaneously, nor set the VCUT bit to "0" (no VREF connection) during the A/D conversion. The VCUT bit does not affect the VREF performance of the D/A converter.

17.2.9 Analog Input Pin and External Sensor Equivalent Circuit

Figure 17.9 shows an example of the analog input pin and external sensor equivalent circuit.

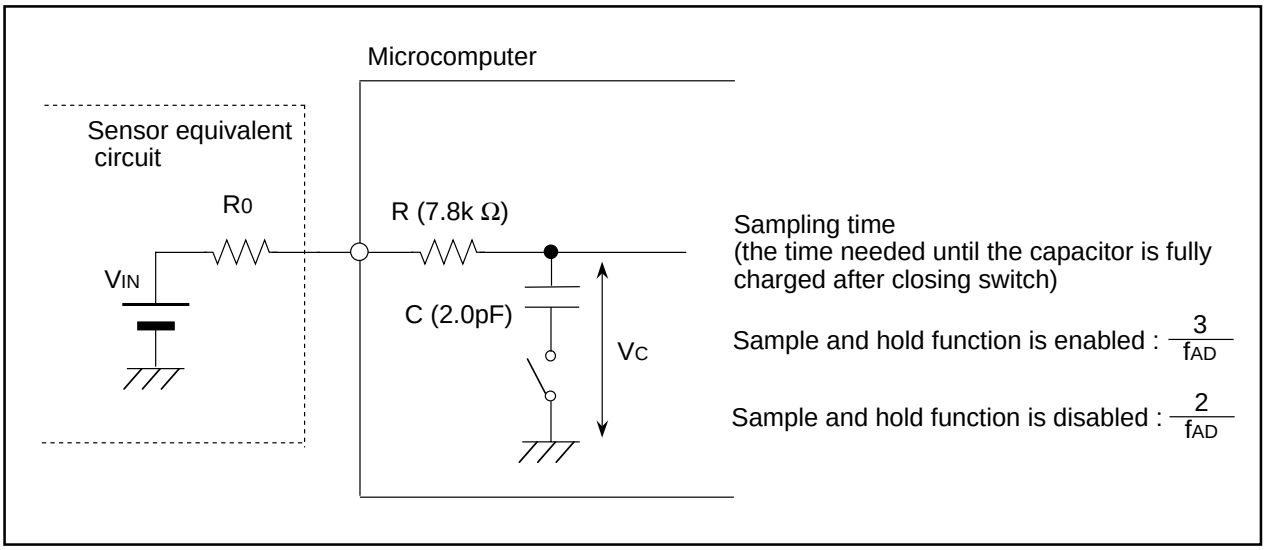


Figure 17.9 Analog Input Pin and External Sensor Equivalent Circuit

18. D/A Converter

The D/A converter consists of two separate 8-bit R-2R ladder D/A converters.
Digital code is converted to an analog voltage when a value is written to the corresponding DAi registers (i=0,1). The DAiE bit in the DACON register determines whether the D/A conversion result is output or not. Set the DAiE bit to "1" (output enabled) to disable a pull-up of a corresponding port.
Output analog voltage (V) is calculated from value n (n=decimal) set in the DAi register.

$$V = \frac{V_{REF} \times n}{256} \quad (n = 0 \text{ to } 255)$$

V_{REF} : reference voltage (not related to VCUT bit setting in the ADiCON1 register)

Table 18.1 lists specifications of the D/A converter. Table 18.2 lists pin settings of the DA0 and DA1 pins. Figure 18.1 shows a block diagram of the D/A converter. Figure 18.2 shows the D/A control register. Figure 18.3 shows a D/A converter equivalent circuit.
When the D/A converter is not used, set the DAi register to "00$_{16}$" and the DAiE bit to "0" (output disabled).

Table 18.1 D/A Converter Specifications

Item	Specification
D/A Conversion Method	R-2R
Resolution	8 bits
Analog Output Pin	2 channels

Table 18.2 Pin Settings

Port	Function	Bit and Setting		
		PD9 Register(1)	PS3 Register(1)	PSL3 Register
P9$_3$	DA$_0$ output	PD9_3=0	PS3_3=0	PSL3_3=1
P9$_4$	DA$_1$ output	PD9_4=0	PS3_4=0	PSL3_4=1

NOTES:
1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

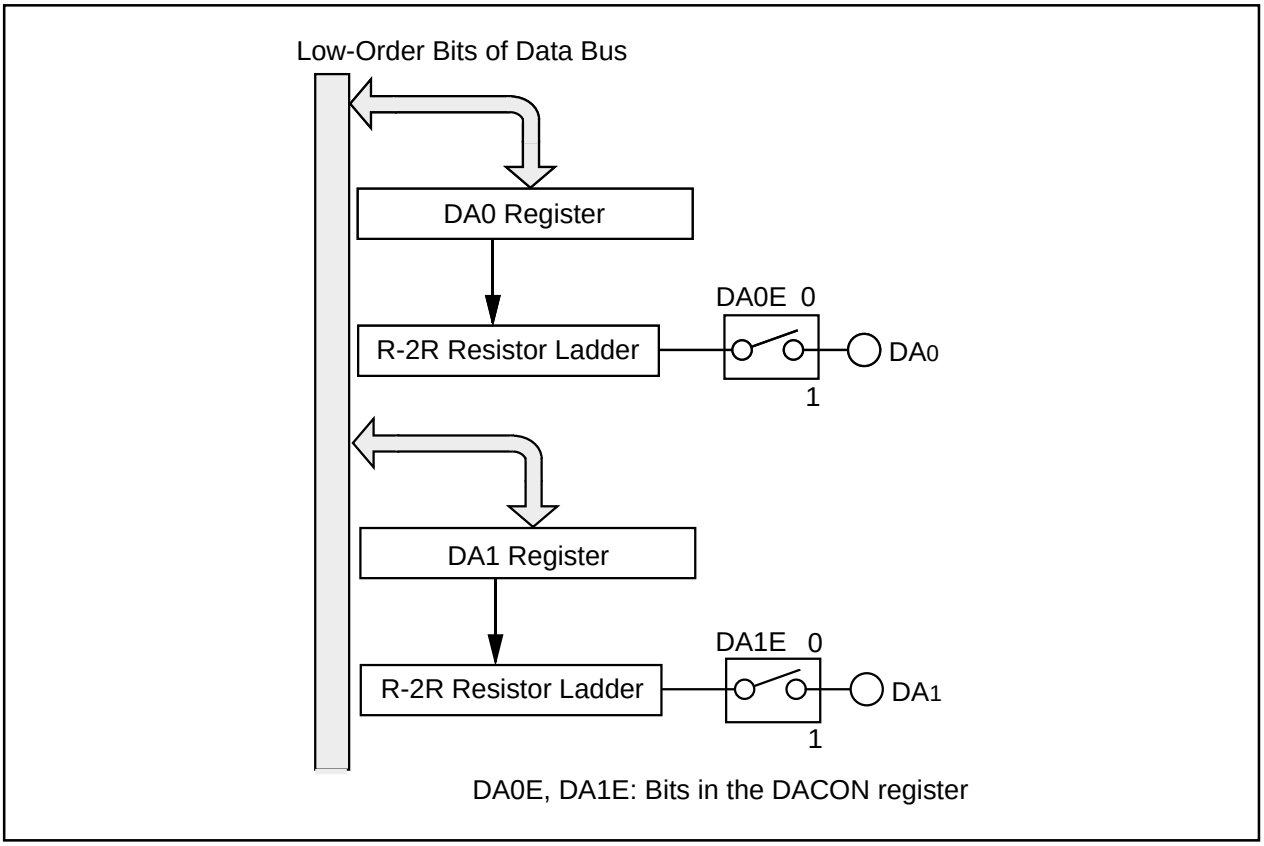


Figure 18.1 D/A Converter

D/A Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
DACON	$039C_{16}$	XXXX $XX00_2$

Bit Symbol	Bit Name	Function	RW
DA0E	D/A0 Output Enable Bit	0 : Disables an output 1 : Enables an output	RW
DA1E	D/A1 Output Enable Bit	0 : Disables an output 1 : Enables an output	RW
—— (b7 - b2)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

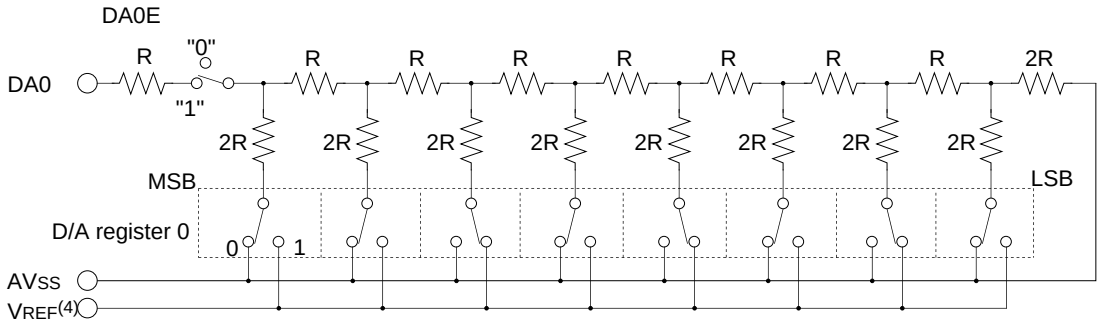
D/A Register i (i=0, 1)

b7 b0

Symbol	Address	After Reset
DA0, DA1	0398_{16}, $039A_{16}$	Indeterminate

Function	Setting Range	RW
Output value of D/A conversion	00_{16} to FF_{16}	RW

Figure 18.2 DACON Register, DA0 and DA1 Registers



NOTES:
1. The above applies when the DA0 register is set to "$2A_{16}$".
2. This circuitry is the same for D/A1.
3. To reduce power consumption when the D/A converter is not used, set the DAiE bit (i=0, 1) to "0" (output disabled) and the DAi register to "00_{16}" to stop current from flowing into the R-2R resistor.
4. This V_{REF} is not related to VCUT bit setting in the AD0CON1 and AD1CON1 registers.

Figure 18.3 D/A Converter Equivalent Circuit

19. CRC Calculation

The CRC (Cyclic Redundancy Check) calculation detects an error in data blocks. A generator polynomial of CRC_CCITT ($X^{16} + X^{12} + X^5 + 1$) generates CRC code.

The CRC code is a 16-bit code generated for a block of data of desired length. This block of data is in 8-bit units. The CRC code is set in the CRCD register every time one-byte data is transferred to the CRCIN register after a default value is written to the CRCD register. CRC code generation for one-byte data is completed in two cycles.

Figure 19.1 shows a block diagram of a CRC circuit. Figure 19.2 shows registers related to CRC. Figure 19.3 shows an example of the CRC calculation.

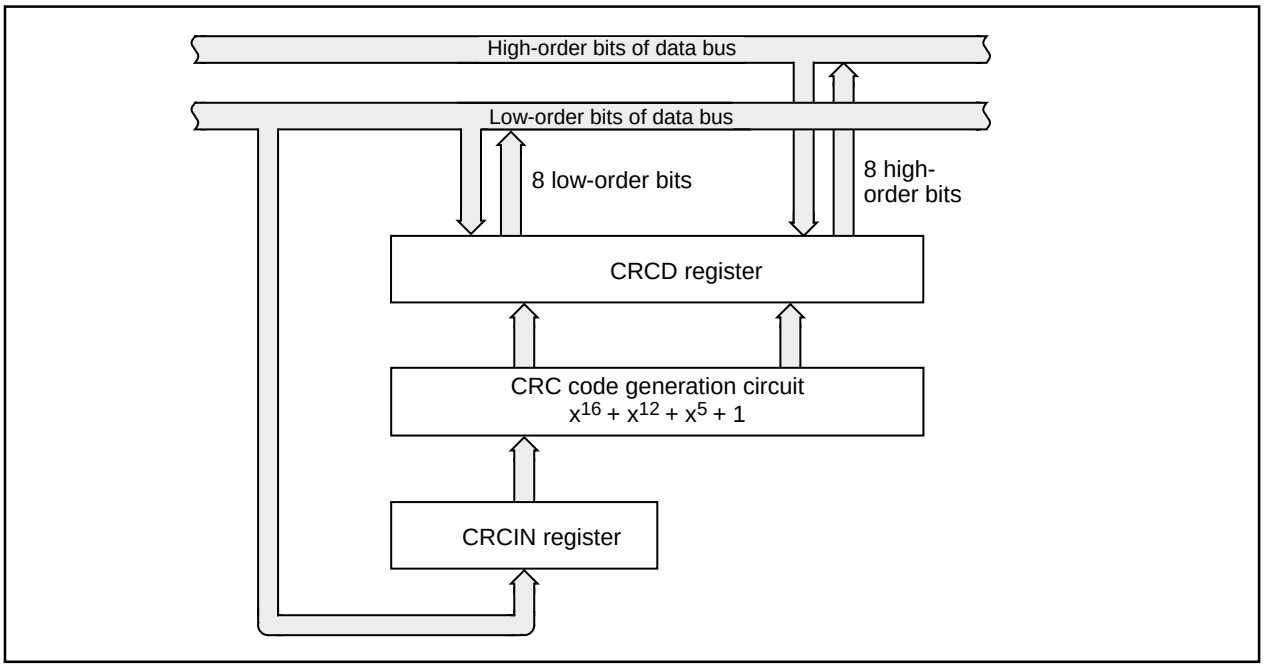


Figure 19.1 CRC Calculation Block Diagram

CRC Data Register

b15 b8 b7 b0

Symbol	Address	After Reset
CRCD	037D16- 037C16	Indeterminate

Function	Setting Range	RW
After default value is written to the CRCD register, the CRC code can be read from the CRCD register by writing data to the CRCIN register. Bit position of the default value is inversed. The inversed value is read as the CRC code.	000016 to FFFF16	RW

CRC Input Register

b7 b0

Symbol	Address	After Reset
CRCIN	037E16	Indeterminate

Function	Setting Range	RW
Data input. Inverse bit position of data.	0016 to FF16	RW

Figure 19.2 CRCD Register and CRCIN Register

CRC Calculation and Setup Procedure to Generate CRC Code for "80C4$_{16}$"

○ CRC Calculation for M32C

CRC Code : a remainder of a division, $\frac{\text{value of the CRCIN register with inversed bit position}}{\text{generation polynomial}}$

Generation Polynomial : $X^{16} + X^{12} + X^5 + 1$ (1 0001 0000 0010 0001$_2$)

○ Setting Steps

(1) Inverse a bit position of "80C4$_{16}$" per byte by program

"80$_{16}$" → "01$_{16}$", "C4$_{16}$" → "23$_{16}$"

(2) Set "0000$_{16}$" (default value) → b15 b0 CRCD register

(3) Set "01$_{16}$" → b7 b0 CRCIN register

Bit position of the CRC code for "80$_{16}$" (9188$_{16}$) is inversed to "1189$_{16}$", which is stored into the CRCD register in 3rd cycle.

b15 b0 1189$_{16}$ CRCD register

(4) Set "23$_{16}$" → b7 b0 CRCIN register

Bit position of the CRC code for "80C4$_{16}$" (8250$_{16}$) is inversed to "0A41$_{16}$", which is stored into the CRCD register in 3rd cycle.

b15 b0 0A41$_{16}$ CRCD register

○ Details of CRC Calculation

As shown in (3) above, bit position of "01$_{16}$" (00000001$_2$) written to the CRCIN register is inversed and becomes "10000000$_2$".
Add "1000 0000 0000 0000 0000 0000$_2$", as "10000000$_2$" plus 16 digits, to "0000$_{16}$" as the default value of the CRCD register to perform the modulo-2 division.

```
                                1000 1000
1 0001 0000 0010 0001 ) 1000 0000 0000 0000 0000 0000   ← data
                        1000 1000 0001 0000 1
                             1000 0001 0000 1000 0
                             1000 1000 0001 0000 1
                                  1001 0001 1000 1000
```

generation polynomial

CRC code

Modulo-2 Arithmetic is calculated on the law below.

0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0
- 1 = 1

"0001 0001 1000 1001$_2$ (1189$_{16}$)", the remainder "1001 0001 1000 1000$_2$ (9188$_{16}$)" with inversed bit position, can be read from the CRCD register.
When going on to (4) above, "23$_{16}$ (00100011$_2$)" written in the CRCIN register is inversed and becomes "11000100$_2$".
Add "1100 0100 0000 0000 0000 0000$_2$", as "11000100$_2$" plus 16 digits, to "1001 0001 1000 1000$_2$" as a remainder of (3) left in the CRCD register to perform the modulo-2 division.
"0000 1010 0100 0001$_2$ (0A41$_{16}$)", the remainder with inversed bit position, can be read from CRCD register.

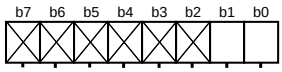
Figure 19.3 CRC Calculation

20. XY Conversion

The XY conversion rotates a 16 x 16 matrix data by 90 degrees and inverses high-order bits and low-order bits of a 16-bit data. Figure 20.1 shows the XYC register.

The 16-bit XiR register (i=0 to 15) and 16-bit YjR register (j=0 to 15) are allocated to the same address. The XiR register is a write-only register, while the YjR register is a read-only register. Access the XiR and YjR register from an even address in 16-bit units. Performance cannot be guaranteed if the XiR and YiR registers are accessed in 8-bit units.

XY Control Register



Symbol	Address	After Reset
XYC	$02E0_{16}$	XXXX $XX00_2$

Bit Symbol	Bit Name	Function	RW
XYC0	Read-Mode Set Bit	0 : Data conversion 1 : No data conversion	RW
XYC1	Write-Mode Set Bit	0 : No bit alignment conversion 1 : Bit alignment conversion	RW
—— (b7 - b2)	Noting is assigned. When write, set to "0". When read, its content is indeterminate.		—

Figure 20.1 XYC Register

The XYC0 bit in the XYC register determines how to read the YjR register.

By reading the YjR register when the XYC0 bit is set to "0" (data conversion), bit j in the X0R to X15R registers can be read simultaneously.

For example, bit 0 in the X0R register can be read if reading bit 0 in the Y0R register, bit 0 in the X1R register if reading bit 1 in the Y0R register..., bit 0 in the X14R register if reading bit 14 in the Y0R register and bit 0 in the X15R register if reading bit 15 in the Y0R register.

Figure 20.2 shows a conversion table when the XYC0 bit is set to "0". Figure 20.3 shows an example of the XY conversion.

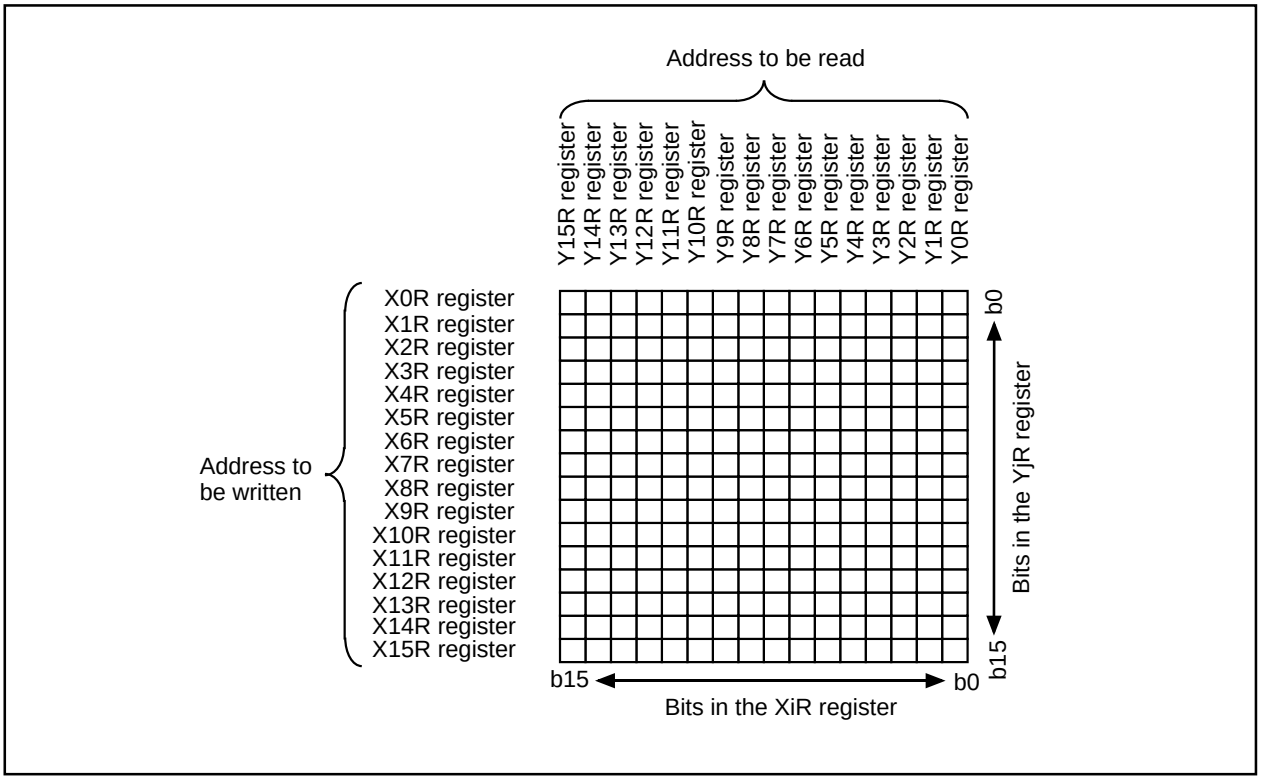


Figure 20.2 Conversion Table when Setting the XYC0 Bit to "0"

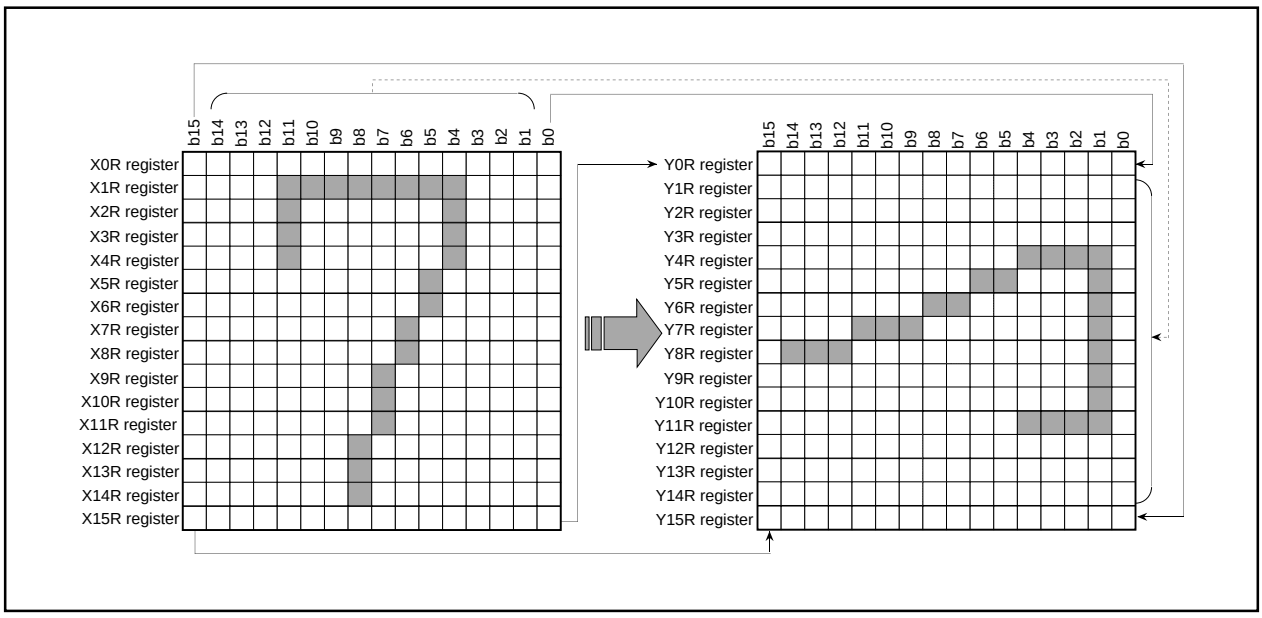


Figure 20.3 XY Conversion

By reading the YjR register when the XYC0 bit in the XYC register is set to "1" (no data conversion), the value written to the XiR register can be read directly. Figure 20.4 shows the conversion table when the XYC0 bit is set to "1."

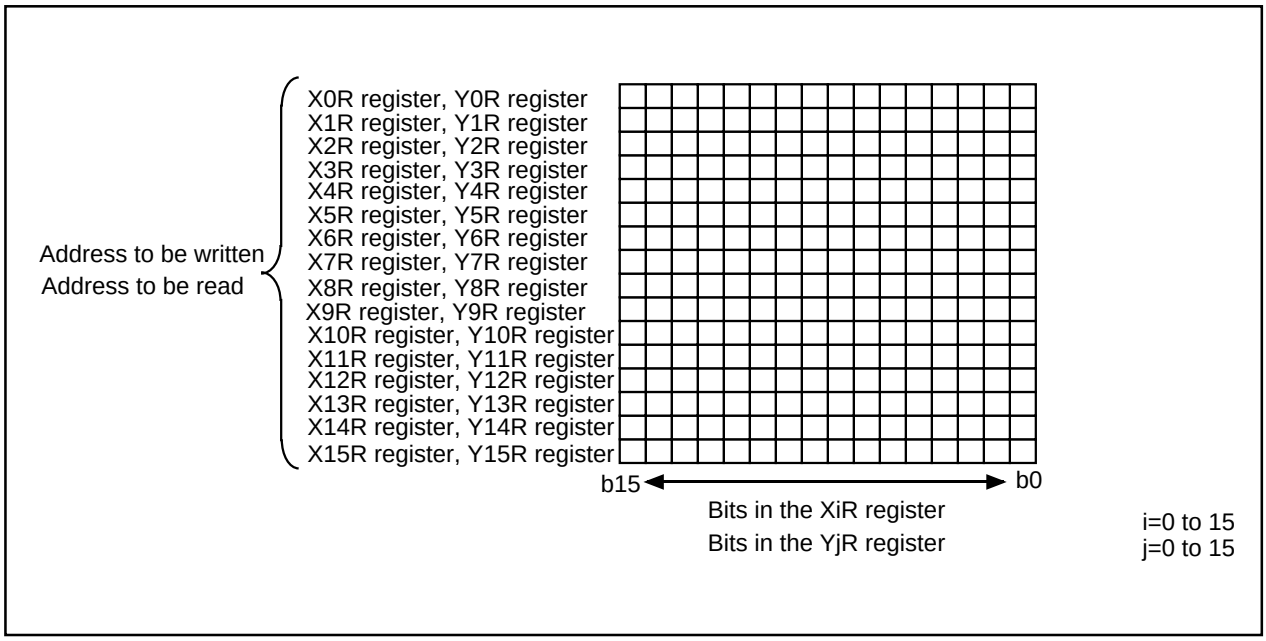


Figure 20.4 Conversion Table when Setting the XYC0 Bit to "1"

The XYC1 bit in the XYC register selects bit alignment of the value in the XiR register.
By writing to the XiR register while the XYC1 bit is set to "0" (no bit alignment conversion), bit alignment is written as is. By writing to the XiR register while the XYC1 bit is set to "1" (bit sequence replaced), bit alignment is written inversed.
Figure 20.5 shows a conversion table when the XYC1 bit is set to "1".

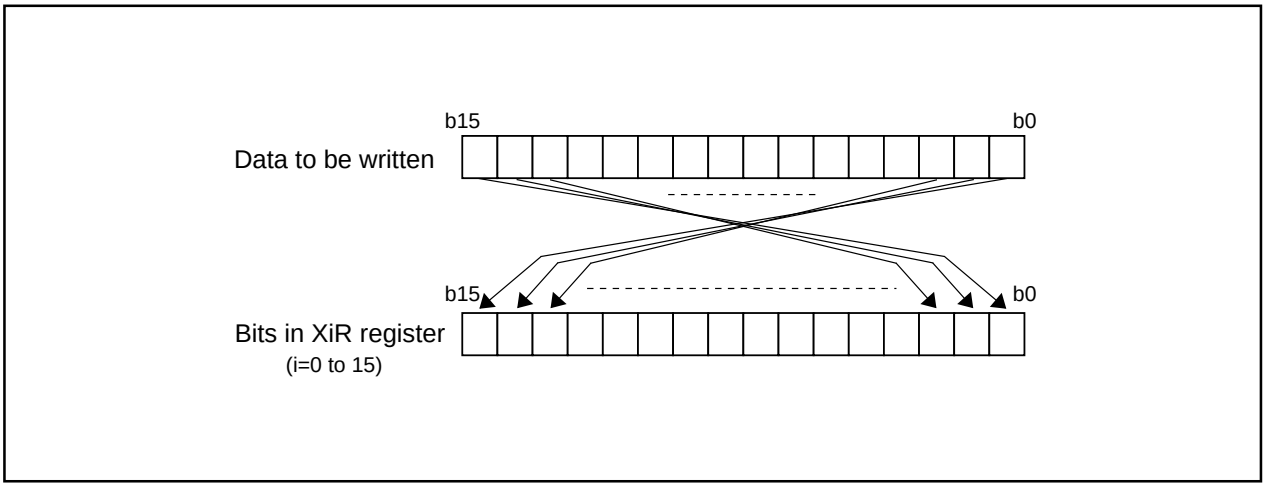


Figure 20.5 Conversion Table when Setting the XYC1 Bit to "1"

21. Intelligent I/O

The intelligent I/O is a multifunctional I/O port for time measurement, waveform generation, clock synchronous serial I/O, clock asynchronous serial I/O (UART), IEBus(1) communications, HDLC data processing and more.

The intelligent I/O consists of four groups. Each group has one 16-bit base timer for free-running operation, eight 16-bit registers for time measurement and waveform generation and two 8-bit shift registers (or one 16-bit shift register) for communications.

Table 21.1 lists functions and channels of the intelligent I/O.

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.

Table 21.1 Intelligent I/O Functions and Channels

Function		Group 0	Group 1	Group 2	Group 3	Group 0, 1 cascaded
Time Measurement(1)		8 channels (3 channels)(2)	4 channels (2 channels)	Not Available	Not Available	8 channels (3 channels)
	Digital Filter	8 channels (3 channels)	4 channels (2 channels)			8 channels (3 channels)
	Trigger Input Prescaler	2 channels	2 channels			2 channels
	Trigger Input Gate	2 channels	2 channels			2 channels
Waveform Generation		4 channels (2 channels)	8 channels (3 channels)	8 channels (3 channels)	8 channels (2 channels)	8 channels (3 channels)
	Single-phase Waveform Output	Available	Available	Available	Available	Available
	Phase-delayed Waveform Output					
	SR Waveform Output					
	Bit Modulation PWM Mode	Not Available	Not Available			Not Available
	RTP Mode					
	Parallel RTP Mode					
Communication		8 bits fixed		Variable	8 or 16 bits	Not Available
	Clock Synchronous Serial I/O Mode	Available		Available	Available	Not Available
	UART Mode			Not Available	Not Available	
	HDLC Data Processing Mode					
	IEBus Mode	Not Available		Available		

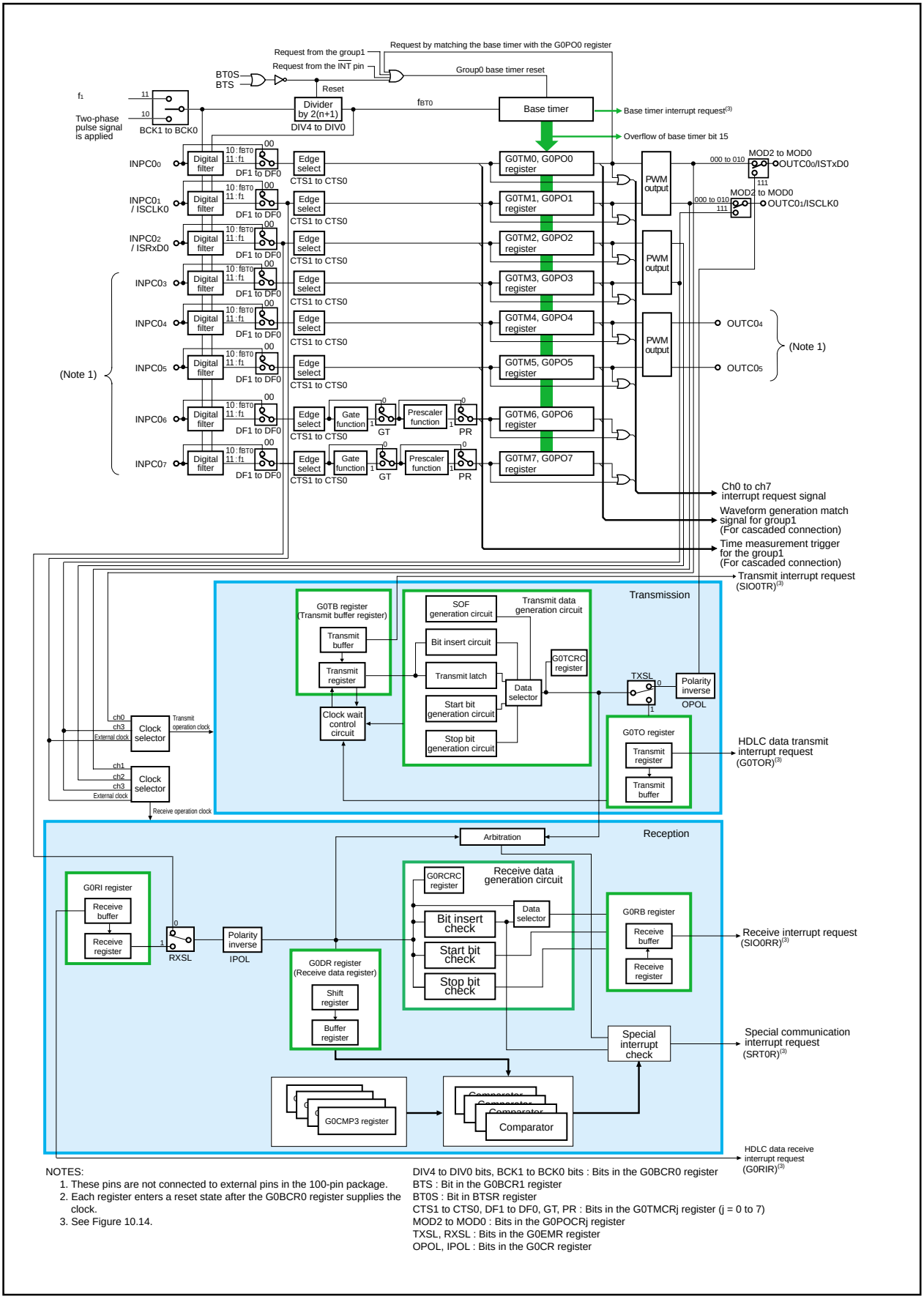
NOTES:

1. Time measurement function and waveform generation function share pins
2. The number of channels available in the 100-pin package are indicated in parentethese ( ).

The time measurement function and waveform generation function can be selected for each channel.

The communication function is available by a combination of multiple channels.

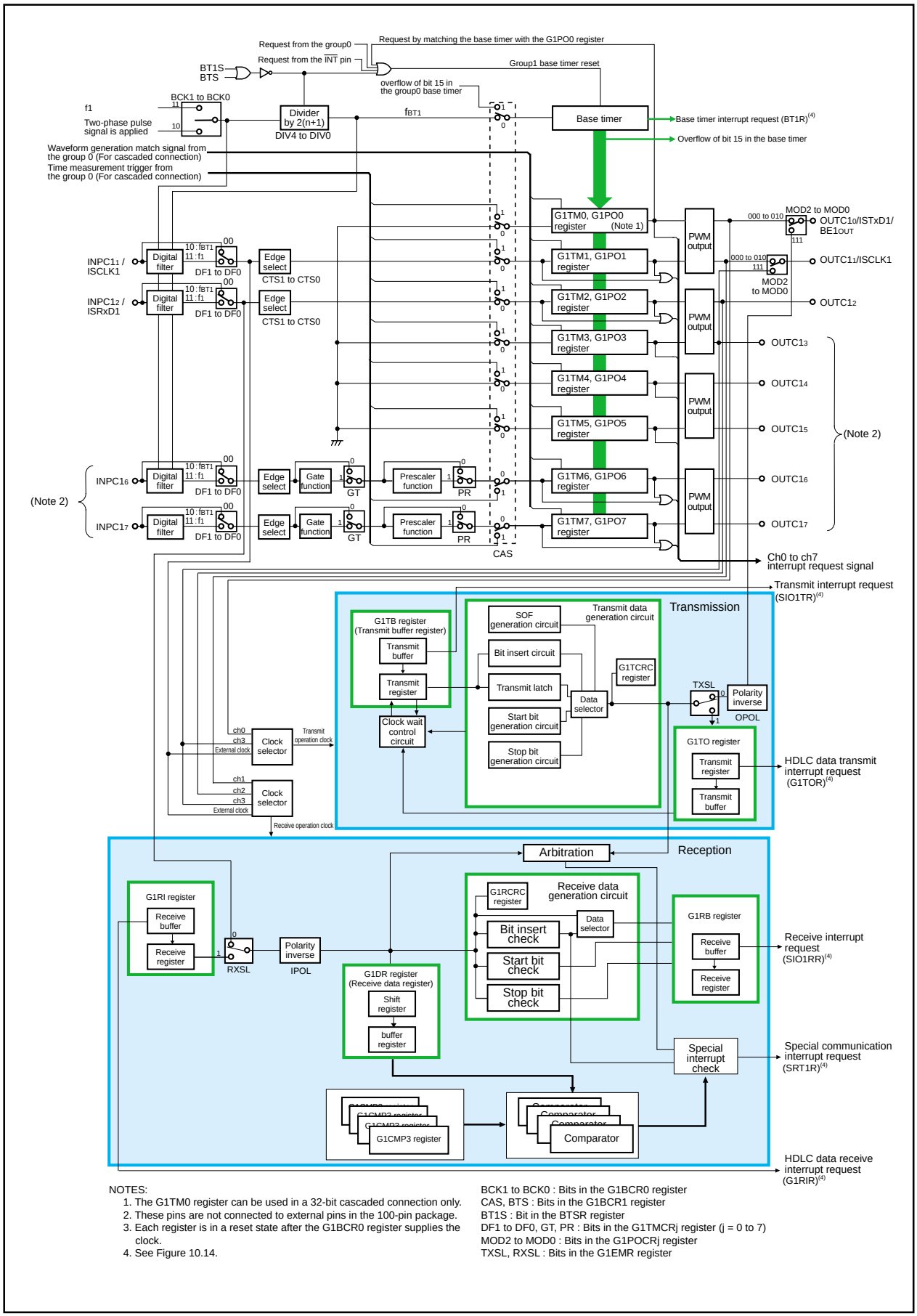
Figures 21.1 to 21.4 show block diagram of the intelligent I/O groups 0 to 3.



NOTES:
1. These pins are not connected to external pins in the 100-pin package.
2. Each register enters a reset state after the G0BCR0 register supplies the clock.
3. See Figure 10.14.

DIV4 to DIV0 bits, BCK1 to BCK0 bits : Bits in the G0BCR0 register
BTS : Bit in the G0BCR1 register
BT0S : Bit in BTSR register
CTS1 to CTS0, DF1 to DF0, GT, PR : Bits in the G0TMCRj register (j = 0 to 7)
MOD2 to MOD0 : Bits in the G0POCRj register
TXSL, RXSL : Bits in the G0EMR register
OPOL, IPOL : Bits in the G0CR register

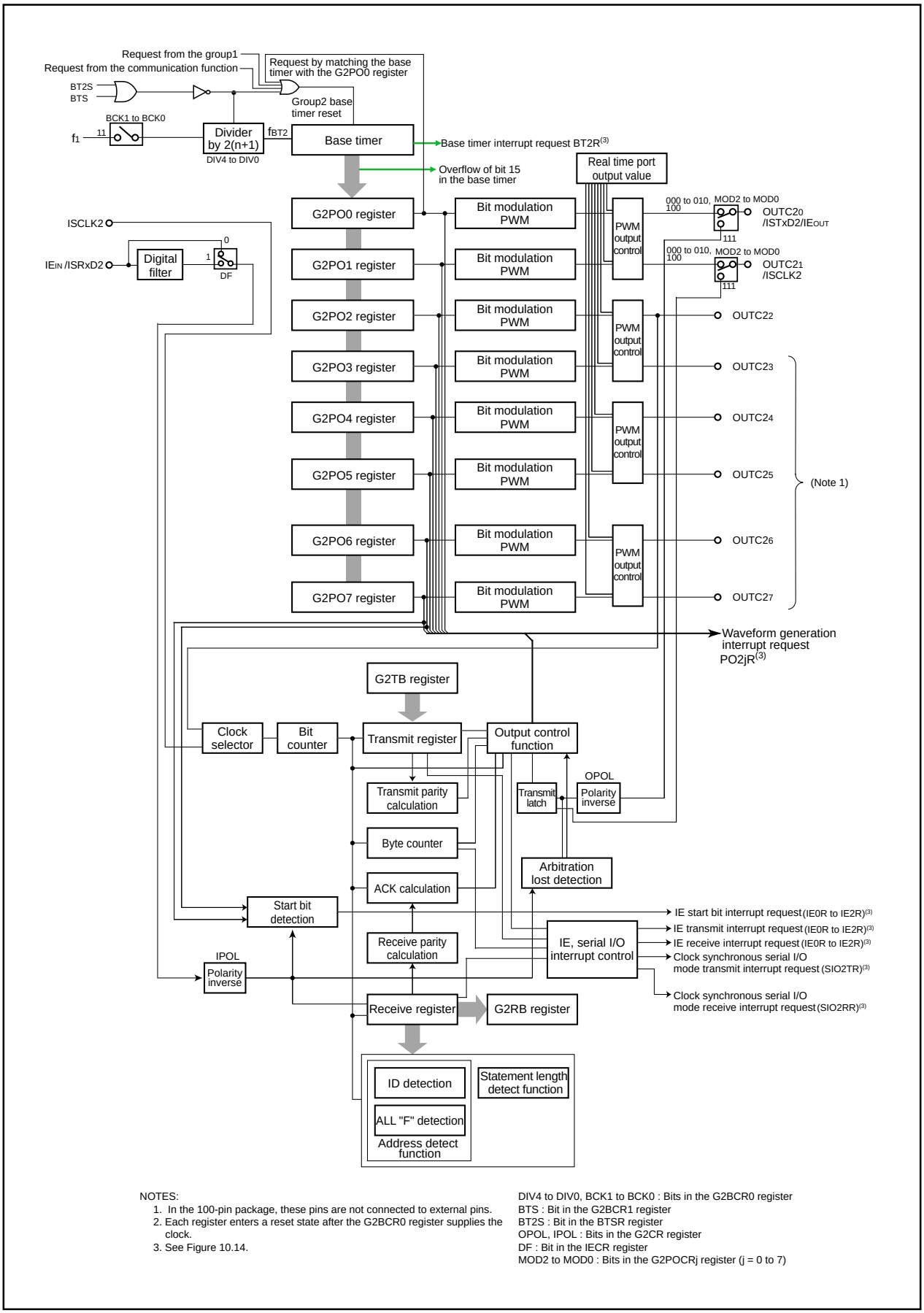
Figure 21.1 Intelligent I/O Group 0 Block Diagram



NOTES:
1. The G1TM0 register can be used in a 32-bit cascaded connection only.
2. These pins are not connected to external pins in the 100-pin package.
3. Each register is in a reset state after the G1BCR0 register supplies the clock.
4. See Figure 10.14.

BCK1 to BCK0 : Bits in the G1BCR0 register
CAS, BTS : Bits in the G1BCR1 register
BT1S : Bit in the BTSR register
DF1 to DF0, GT, PR : Bits in the G1TMCRj register (j = 0 to 7)
MOD2 to MOD0 : Bits in the G1POCRj register
TXSL, RXSL : Bits in the G1EMR register

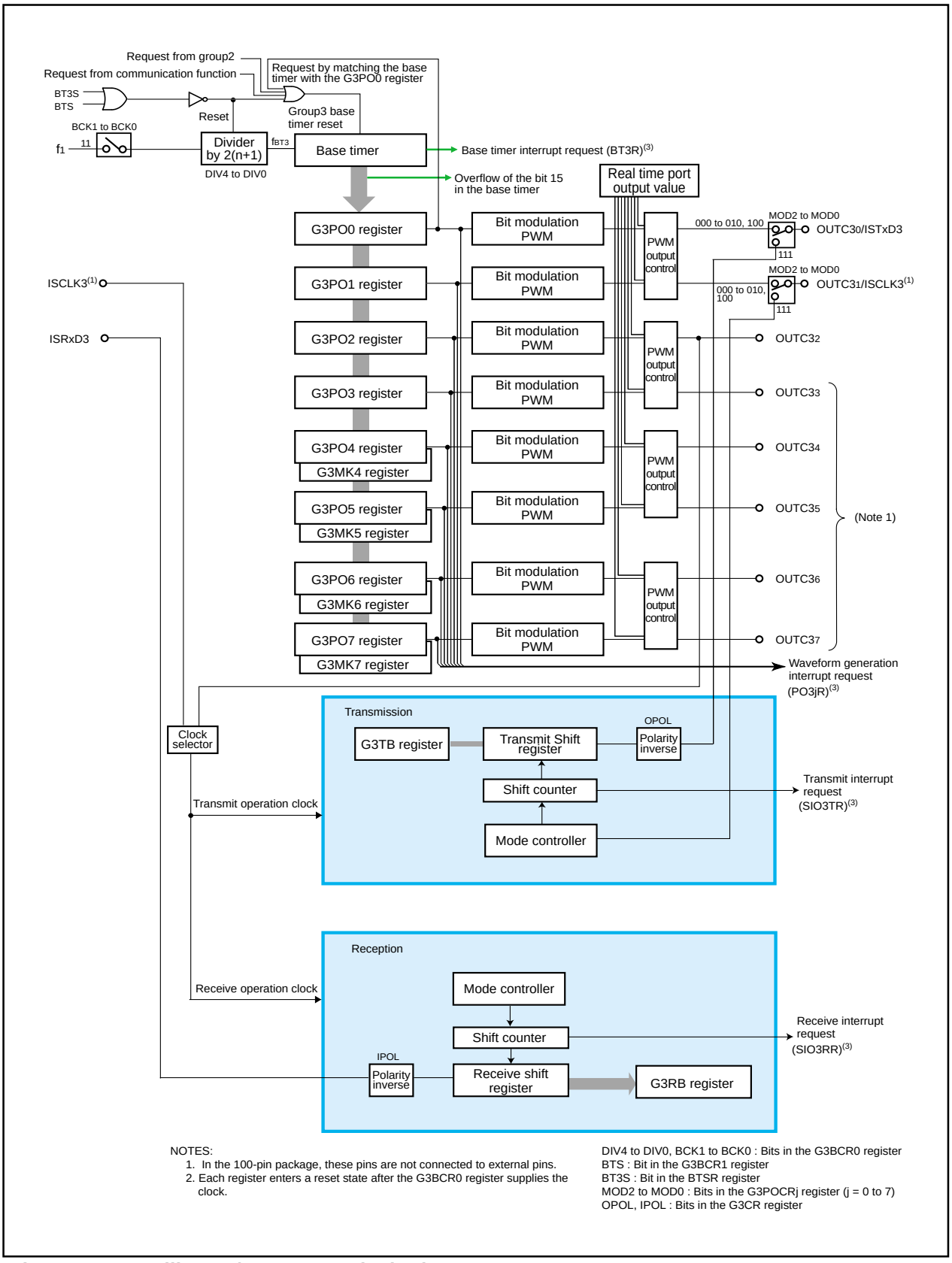
Figure 21.2 Intelligent I/O Group 1 Block Diagram



NOTES:
1. In the 100-pin package, these pins are not connected to external pins.
2. Each register enters a reset state after the G2BCR0 register supplies the clock.
3. See Figure 10.14.

DIV4 to DIV0, BCK1 to BCK0 : Bits in the G2BCR0 register
BTS : Bit in the G2BCR1 register
BT2S : Bit in the BTSR register
OPOL, IPOL : Bits in the G2CR register
DF : Bit in the IECR register
MOD2 to MOD0 : Bits in the G2POCRj register (j = 0 to 7)

Figure 21.3 Intelligent I/O Group 2 Block Diagram



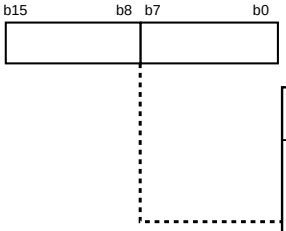
NOTES:
1. In the 100-pin package, these pins are not connected to external pins.
2. Each register enters a reset state after the G3BCR0 register supplies the clock.

DIV4 to DIV0, BCK1 to BCK0 : Bits in the G3BCR0 register
BTS : Bit in the G3BCR1 register
BT3S : Bit in the BTSR register
MOD2 to MOD0 : Bits in the G3POCRj register (j = 0 to 7)
OPOL, IPOL : Bits in the G3CR register

Figure 21.4 Intelligent I/O Group 3 Block Diagram

Figures 21.5 to 21.15 show registers associated with the intelligent I/O base timer, the time measurement function and waveform generation function. (For registers associated with the communication function, see Figures 21.32 to 21.38, Figures 21.42 to 21.45, Figures 21.47 to 21.49.)

Group i Base Timer Register (i=0 to 3)(2)

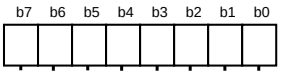


Symbol	Address	After Reset
G0BT,G1BT	$00E1_{16}$ - $00E0_{16}$, 0121_{16} - 0120_{16}	Indeterminate
G2BT,G3BT	0161_{16} - 0160_{16}, $01A1_{16}$ - $01A0_{16}$	Indeterminate

Function	Setting Range	RW
• When the base timer is counting: When read, the value of the counter can be read. When write, the counter starts counting from the value written. When the base timer is reset, the GiBT register is set to "0000_{16}"(1). • When the base timer is reset: The GiBT register is set to "0000_{16}" but the value is indeterminate. No value is written(1).	0000_{16} to $FFFF_{16}$	RW

NOTES:
1. Each base timer stops only when the BCK1 to BCK0 bits in the GiBCR0 register are set to "00_2" (clock stopped). The base timer counts when the BCK1 to BCK0 bits are set to a value other than "00_2". When the BTiS bit in the BTSR register and the BTS bit in the GiBCR1 register are set to "0", the base timer is reset continually, remaining set to "0000_{16}". This, in effect, places the base timer in a "no counting" state. When either BTiS bit or BTS bit is set to "1", this state is cleared and counting starts.
2. The GiBT register reflects the value of the base timer with a delay of one half f_{BTi} cycle.

Group i Base Timer Control Register 0 (i=0 to 3)(1)



Symbol	Address	After Reset
G0BCR0 to G3BCR0	$00E2_{16}$, 0122_{16}, 0162_{16}, $01A2_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
BCK0	Count Source Select Bit	b1b0 0 0: Clock stops 0 1: Do not set to this value 1 0: Two-phase pulse signal is applied(2) 1 1: f_1	RW
BCK1			RW
DIV0	Count Source Division Ratio Select Bit	If setting value is n (n = 0 to 31), count source is divided by 2(n + 1). No division if n=31. b6 b5 b4 b3 b2 (n=0) 0 0 0 0 0 : Divide-by-2 (n=1) 0 0 0 0 1 : Divide-by-4 (n=2) 0 0 0 1 0 : Divide-by-6 : (n=30) 1 1 1 1 0 : Divide-by-62 (n=31) 1 1 1 1 1 : No division	RW
DIV1			RW
DIV2			RW
DIV3			RW
DIV4			RW
IT	Base Timer Interrupt Select Bit	0 : Bit 15 overflows 1 : Bit 14 overflows	RW

NOTES:
1. When the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement, waveform generation function), set the G0BCR0 register and G1BCR0 register to the same value.
2. This setting can be used only when the UD1 to UD0 bits in the GjBCR1 register (j=0, 1) of group 0 or 1 are set to "10_2" (two-phase signal processing mode). Do not set the BCK1 to BCK0 bits to "10_2" in other modes or in group 2 or 3.

Figure 21.5 G0BT to G3BT Register and G0BCR0 to G3BCR0 Register

Group i Base Timer Control Register 1 (i=0,1)

b7	b6	b5	b4	b3	b2	b1	b0
				0			

Symbol	Address	After Reset
G0BCR1, G1BCR1	$00E3_{16}$, 0123_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
RST0	Base Timer Reset Cause Select Bit 0	0: The base timer is not reset by synchronizing with the base timer reset 1: The base timer is reset by synchronizing with the base timer reset(1)	RW
RST1	Base Timer Reset Cause Select Bit 1	0: The base timer is not reset by matching with the GiPO0 register 1: The base timer is reset by matching with the GiPO0 register(2)	RW
RST2	Base Timer Reset Cause Select Bit 2	0: The base timer is not reset by applying "L" to the $\overline{INTi}$ pin 1: The base timer is reset by applying "L" to the $\overline{INTi}$ pin(3)	RW
——— (b3)	Reserved Bit	Set to "0"	RW
BTS	Base Timer Start Bit(5, 6)	0: Base timer is reset 1: Base timer starts counting	RW
UD0	Counter Increment/ Decrement Control Bit	b6b5 0 0 : Counter increment mode 0 1 : Counter increment/decrement mode 1 0 : Two-phase pulse signal processing mode(7) 1 1 : Do not set to this value	RW
UD1			RW
CAS	Groups 0 and 1 Cascaded Connection Function Select Bit	0: 16-bit time measurement or waveform generation function 1: 32-bit time measurement or waveform generation function(4)	RW

NOTES:
1. In group 0, the base timer is reset by synchronizing with the group 1 base timer reset. In group 1, the base timer is reset by synchronizing with the group 0 base timer reset.
2. The base timer is reset two f_{BTi} clock cycles after the base timer matches the value set in the GiPO0 register. (See Figure 21.13 for details on the GiPO0 register.) When the RST1 bit is set to "1", the value of the GiPOj register (j=1 to7) for the waveform generation function and communication function must be set to a smaller value than that of the GiPO0 register.
3. In group 0, the base timer is reset when "L" is applied to the $\overline{INT0}$ pin. In group 1, the base timer is reset when "L" is applied to the $\overline{INT1}$ pin.
4. When the CAS bit is set to "1" (32-bit time measurement, waveform generation function), set the G0BCR1 register to "81_{16}" and the G1BCR1 register to "1000 0XX0$_2$".
5. When starting the group 0 or 1 base timer separately, set the BTS bit to "1" after the BTkS bit (k=0 to 1) in the BTSR register is set to "0".
6. When starting the base timers in multiple groups simultaneously, use the BTSR register. Set the BTS bit to "0".
7. In two-phase pulse signal processing mode, the base timer is not reset, even when the RST1 bit is set to "1", if the counter is decremented two clock cycles after the base timer matches the value set in the GiPO0 register

Figure 21.6 G0BCR1 and G1BCR1 Registers

Group 2 Base Timer Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
	0	0		0			

Symbol	Address	After Reset
G2BCR1	0163_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
RST0	Base Timer Reset Cause Select Bit 0	0 : The base timer is not reset by synchronizing with the group 1 base timer reset 1 : The base timer is reset by synchronizing with the group 1 base timer reset	RW
RST1	Base Timer Reset Cause Select Bit 1	0 : The base timer is not reset by matching with the G2PO0 register 1 : The base timer is reset by matching with the G2PO0 register(1)	RW
RST2	Base Timer Reset Cause Select Bit 2	0 : The base timer is not reset by a reset request from the communication function 1 : The base timer is reset by a reset request from the communication function	RW
——— (b3)	Reserved Bit	Set to "0"	RW
BTS	Base Timer Start Bit(3, 4)	0 : Base timer is reset 1 : Base timer starts counting	RW
——— (b6 - b5)	Reserved Bit	Set to "0"	RW
PRP	Parallel Real-Time Port Function Select Bit(2)	0 : RTP output mode 1 : Parallel RTP output mode	RW

NOTES:
1. The base timer is reset two f_{BT2} clock cycles after the base timer matches the value set in the G2PO0 register. (See Figure 21.13 for details on the G2PO0 register.) When the RST1 bit is set to "1", the value of the G2POi register (i=1 to7), for the waveform generation function and communication function, must be set to a smaller value than that of the G2PO0 register.
2. The PRP bit is valid when the RTP bit in the G2POCRi register is set to "1" (not used)
3. When starting the group 2 base timer, set the BTS bit to "1" after the BT2S bit in the BTSR register is set to "0".
4. When starting the base timers in multiple groups simultaneously, use the BTSR register. Set the BTS bit to "0".

Figure 21.7 G2BCR1 Register

Group 3 Base Timer Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
	0	0		0			

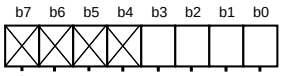
Symbol	Address	After Reset
G3BCR1	$01A3_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
RST0	Base Timer Reset Cause Select Bit 0	0 : The base timer is not reset by synchronizing with the group 2 base timer reset 1 : The base timer is reset by synchronizing with the group 2 base timer reset	RW
RST1	Base Timer Reset Cause Select Bit 1	0 : The base timer is not reset by matching with the G3PO0 register 1 : The base timer is reset by matching with the G3PO0 register(1)	RW
RST2	Base Timer Reset Cause Select Bit 2	0 : The base timer is not reset by a reset request from the communication function 1 : The base timer is reset by a reset request from the communication function	RW
—— (b3)	Reserved Bit	Set to "0"	RW
BTS	Base Timer Start Bit(3, 4)	0 : Base timer is reset 1 : Base timer starts counting	RW
—— (b6 - b5)	Reserved Bit	Set to "0"	RW
PRP	Parallel Real-Time Port Function Select Bit(2)	0 : RTP output mode 1 : Parallel RTP output mode	RW

NOTES:
1. The base timer is reset after two f_{BT3} clock cycles after the base timer matches the value set in the G3PO0 register. (See Figure 21.13 for details on the G3PO0 register.) When the RST1 bit is set to "1", the value of the G3POi register (i=1 to7), for the waveform generation function and communication function, must be set to a smaller value than that of the G2PO0 register.
2. The PRP bit is valid when the RTP bit in the G3POCRi register is set to "1" (not used)
3. When starting the group 3 base timer, set the BTS bit to "1" after the BT3S bit in the BTSR register is set to "0".
4. When starting the base timers in multiple groups simultaneously, use the BTSR register. Set the BTS bit to "0".

Figure 21.8 G3BCR1 Register

Base Timer Start Register(1, 2)



Symbol	Address	After Reset
BTSR	0164_{16}	$XXXX\ 0000_2$

Bit Symbol	Bit Name	Function	RW
BT0S	Group 0 Base Timer Start Bit	0 : Base timer reset 1 : Base timer starts counting	RW
BT1S	Group 1 Base Timer Start Bit	0 : Base timer reset 1 : Base timer starts counting	RW
BT2S	Group 2 Base Timer Start Bit	0 : Base timer reset 1 : Base timer starts counting	RW
BT3S	Group 3 Base Timer Start Bit	0 : Base timer reset 1 : Base timer starts counting	RW
—— (b7 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

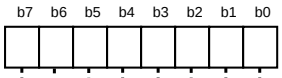
NOTES:

1. Set registers as follows before using the intelligent I/O:
   (1) Set the G2BCR0 register to supply the clock to the group 2 base timer
   (2) Set all BT0S to BT3S bits in the BTSR register to "0" (base timer reset)
   (3) Set other registers associated with the intelligent I/O

   The BTiS bit (i=0 to 3) allows the base timers in multiple groups to start counting simultaneously. When starting the base timers separately, set the BTiS bit to "0" before setting the BTS bit in the GiBCR1 register.
2. Use the following procedure to start base timers in multiple groups simultaneously (including groups 1 and 2 cascaded connections). This procedure is not required when starting the base timers individually.
   • Set the BCK1 to BCK0 bits and DIV4 to DIV0 bits in the GiBCR0 register (i=0 to 3) of the groups to be started simultaneously, to the same value.
   • After the BCK1 to BCK0 bits or DIV4 to DIV0 bits are changed, use the following procedure to start the base timer twice.
   (1) Set the BTiS bit in the BTSR register to "1" (base timer starts counting).
   (2) Set the BTiS bit to "0" (base timer stops counting) after one f_{BTi} clock cycle.
   (3) After waiting at least one additional f_{BTi} clock cycle, set the BTiS bit to "1" (base timer starts counting).

Figure 21.9 BTSR Register

Group i Time Measurement Control Register j (i=0,1; j=0 to 7)(1)

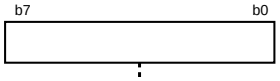


Symbol	Address	After Reset
G0TMCR0 to G0TMCR3	00D8$_{16}$, 00D9$_{16}$, 00DA$_{16}$, 00DB$_{16}$	00$_{16}$
G0TMCR4 to G0TMCR7	00DC$_{16}$, 00DD$_{16}$, 00DE$_{16}$, 00DF$_{16}$	00$_{16}$
G1TMCR0 to G1TMCR3	0118$_{16}$, 0119$_{16}$, 011A$_{16}$, 011B$_{16}$	00$_{16}$
G1TMCR4 to G1TMCR7	011C$_{16}$, 011D$_{16}$, 011E$_{16}$, 011F$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
CTS0	Time Measurement Trigger Select Bit	b1 b0 0 0 : No time measurement 0 1 : Rising edge 1 0 : Falling edge 1 1 : Both edges	RW
CTS1			RW
DF0	Digital Filter Function Select Bit	b3 b2 0 0 : No digital filter 0 1 : Do not set to this value 1 0 : f_{BTi} 1 1 : f_1	RW
DF1			RW
GT	Gate Function Select Bit(2, 4)	0 : Gate function is not used 1 : Gate function is used	RW
GOC	Gate Function Clear Select Bit(2, 3, 5)	0 : Not cleared 1 : The gate is cleared when the base timer matches the GiPOk register	RW
GSC	Gate Function Clear Bit(2, 3)	The gate is cleared by setting the GSC bit to "1"	RW
PR	Prescaler Function Select Bit(2)	0 : Not used 1 : Used	RW

NOTES:
1. If the CAS bit in the GiBCR1 register is set to "0" (16-bit time measurement function), the G1TMCR0 and G1TMCR3 to G1TMCR5 registers cannot be used. When write, set these registers to "00$_{16}$". If the CAS bit is set to "1" (32-bit time measurement function), set the same values in the G0TMCRj and G1TMCRj registers.
2. These bits are in the GiTMCR6 and GiTMCR7 registers. Set all bits 4 to 7 in the GiTMCR0 to GiTMCR5 registers to "0".
3. These bits are enabled only when the GT bit is set to "1"
4. If the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement function), set the GT bit to "0". The gate function cannot be used.
5. The GOC bit is set to "0" after the gate function is cleared. See Figure 18.13 for details on the GiPOk register (k=4 when j=6; k=5 when j=7).

Group i Time Measurement Prescale Register j (i=0,1; j=6,7)



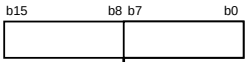
Symbol	Address	After Reset
G0TPR6 to G0TPR7	00E4$_{16}$, 00E5$_{16}$	00$_{16}$
G1TPR6 to G1TPR7	0124$_{16}$, 0125$_{16}$	00$_{16}$

Function	Setting Range	RW
If the setting value is n, the value of the base timer is stored into GiTMj register whenever a trigger input is counted by n+1(1)	00$_{16}$ to FF$_{16}$	RW

NOTES:
1. The first prescaler, after the PR bit in the GiTMCRj register is changed from "0" (prescaler function used) to "1" (prescaler function not used), may be divided by n rather than n+1. The subsequent prescaler is divided by n+1.

Figure 21.10 G0TMCR0 to G0TMCR7, G1TMCR0 to G1TMCR7, G0TPR6, G0TPR7, G1TPR6, and G1TPR7 Registers

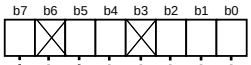
Group i Time Measurement Register j (i=0,1; j=0 to 7)



Symbol	Address	After Reset
G0TM0 to G0TM2	$00C1_{16}$ - $00C0_{16}$, $00C3_{16}$ - $00C2_{16}$, $00C5_{16}$ - $00C4_{16}$	Indeterminate
G0TM3 to G0TM5	$00C7_{16}$ - $00C6_{16}$, $00C9_{16}$ - $00C8_{16}$, $00CB_{16}$ - $00CA_{16}$	Indeterminate
G0TM6 to G0TM7	$00CD_{16}$ - $00CC_{16}$, $00CF_{16}$ - $00CE_{16}$	Indeterminate
G1TM0 to G1TM2	0101_{16} - 0100_{16}, 0103_{16} - 0102_{16}, 0105_{16} - 0104_{16}	Indeterminate
G1TM3 to G1TM5	0107_{16} - 0106_{16}, 0109_{16} - 0108_{16}, $010B_{16}$ - $010A_{16}$	Indeterminate
G1TM6 to G1TM7	$010D_{16}$ - $010C_{16}$, $010F_{16}$ - $010E_{16}$	Indeterminate

Function	Setting Range	RW
The value of the base timer is stored every trigger input. When the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement), 16 low-order bits are stored into the G0TMj register and 16 high-order bits are into stored the G1TMj register.	———	RO

Group i Waveform Generation Control Register j (i=0 to 1; j=0 to 7)(1)



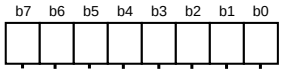
Symbol	Address	After reset
G0POCR0 to G0POCR3	$00D0_{16}$, $00D1_{16}$, $00D2_{16}$, $00D3_{16}$	0X00 X000$_2$
G0POCR4 to G0POCR7	$00D4_{16}$, $00D5_{16}$, $00D6_{16}$, $00D7_{16}$	0X00 X000$_2$
G1POCR0 to G1POCR3	0110_{16}, 0111_{16}, 0112_{16}, 0113_{16}	0X00 X000$_2$
G1POCR4 to G1POCR7	0114_{16}, 0115_{16}, 0116_{16}, 0117_{16}	0X00 X000$_2$

Bit Symbol	Bit Name	Function	RW
MOD0	Operation Mode Select Bit	b2b1b0 0 0 0: Single waveform output mode 0 0 1: SR waveform output mode(2) 0 1 0: Phase-delayed waveform output mode 0 1 1: Do not set to this value 1 0 0: Do not set to this value 1 0 1: Do not set to this value 1 1 0: Do not set to this value(3) 1 1 1: Use a communication function output(4)	RW
MOD1			RW
MOD2			RW
——— (b3)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
IVL	Output Initial Value Select Bit	0: Outputs "L" as an initial value 1: Outputs "H" as an initial value	RW
RLD	GiPOj Register Value Reload Timing Select Bit	0: Reloads the GiPOj register when value is written 1: Reloads the GiPOj register when the base timer is reset	RW
——— (b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
INV	Inverse Output Function Select Bit(5)	0: Output is not inversed 1: Output is inversed	RW

NOTES:
1. Groups 0 and 1 have 16-bit and 32-bit waveform generation functions.
   If the CAS bit in the GiBCR1 register is set to "0" (16-bit waveform generation function), the G0POCR2 to G0POCR3 and G0POCR 6 to G0POCR7 registers cannot be used. When write, set these registers to "00_{16}".
   If the CAS bit is set to "1" (32-bit waveform generation function), set the same values in the G0POCRj and G1POCRj registers.
2. This setting is valid only for even channels. In SR waveform output mode, values written to the corresponding odd channel (next channel after an even channel) are ignored. Even channels output waveforms. Odd channels output no waveforms.
3. To receive data in UART mode of group 0 and 1, set the GiPOCR2 register to "0000 0110$_2$".
4. This setting is valid only for channels 0 and 1. To use ISTxDi, set the MOD2 to MOD0 bits in the GiPOCR0 register to "111$_2$". To use ISCLKi for an output, set the MOD2 to MOD0 bits in the GiPOCR1 register to"111$_2$". Do not set the MOD2 to MOD0 bits to "111$_2$" except in the channels 0 and 1 and for the communication function.
5. The inverse output function is the final step in the waveform generation process. If the INV bit is set to "1" (output inversed), the output signal is "H" when the IVL bit is set to "0" (outputs "L" as an initial value) and "L" when the IVL bit is set to "1" (outputs "H" as an initial value).

Figure 21.11 G0TM0 to G0TM7, G1TM0 to G1TM7, Registers and G0POCR0 to G0POCR7, G1POCR0 to G1POCR7 Registers

Group i Waveform Generation Control Register j (i=2 to 3; j=0 to 7)



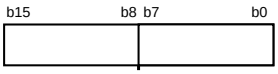
Symbol	Address	After Reset
G2POCR0 to G2POCR3	0150_{16}, 0151_{16}, 0152_{16}, 0153_{16}	00_{16}
G2POCR4 to G2POCR7	0154_{16}, 0155_{16}, 0156_{16}, 0157_{16}	00_{16}
G3POCR0 to G3POCR3	0190_{16}, 0191_{16}, 0192_{16}, 0193_{16}	00_{16}
G3POCR4 to G2POCR7	0194_{16}, 0195_{16}, 0196_{16}, 0197_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
MOD0	Operation Mode Select Bit(5)	b2b1b0 0 0 0: Single waveform output mode 0 0 1: SR waveform output mode(1) 0 1 0: Inverse waveform output mode 0 1 1: Do not set to this value 1 0 0: Bit-modulation PWM mode 1 0 1: Do not set to this value 1 1 0: Do not set to this value 1 1 1: Use a communication function output(2)	RW
MOD1			RW
MOD2			RW
PRT	Parallel Real-time Port Output Trigger Select Bit(4)	0: Not triggered by matching the base timer with the GiPO0 to GiPO7 registers 1: Triggered by matching the base timer with the GiPO0 to GiPO7 registers	RW
IVL	Output Initial Value Select Bit	0: Outputs "L" as the initial value 1: Outputs "H" as the initial value	RW
RLD	GiPOj Register Value Reload Timing Select Bit	0: Reloads the GiPOj register when counter is written to 1: Reloads the GiPOj register when the base timer is reset	RW
RTP	Real-time Port Function Select Bit	0: Not used 1: Used (RTP output mode or parallel RTP output mode)	RW
INV	Inverse Output Function Select Bit(3)	0: Output is not inversed 1: Output is inversed	RW

NOTES:
1. This setting is valid only for even channels. In SR waveform output mode, values written to the corresponding odd channel (next channel after an even channel) are ignored. Even channels output waveforms. Odd channels output no waveforms.
2. This setting is valid only for channels 0 and 1 in the groups 2 and 3. To use ISTxD2 or IEOUT, set the MOD2 to MOD0 bits in the G2POCR0 register to "111_2". To use ISCLK2 for an output, set the MOD2 to MOD0 bits in the G2POCR1 register to "111_2". Do not set the MOD2 to MOD0 bits to "111_2" except in the channels 0 and 1.
   To use ISTxD3, set the MOD2 to MOD0 bits in the G3POCR0 register to "111_2". To use ISCLK3 for an output, set the MOD2 to MOD0 bits in the G3POCR1 register to"111_2". Do not set the MOD2 to MOD0 bits to "111_2" except in the channels 0 and 1.
3. The inverse output function is the final step in the waveform generation process. If the INV bit is set to "1" (output inversed), the output signal is "H" when the IVL bit is set to "0" (outputs "L" as an initial value) and "L" when the IVL bit is set to "1" (outputs "H" as an initial value).
4. The PRT bit is valid when the RTP bit is set to "1" (real-time port function used) and the PRP bit in the GiBCR1 register is set to "1" (parallel RTP output mode).
5. When the RTP bit is set to "1", the value written to the MOD2 to MOD0 bits is ignored.

Figure 21.12 G2POCR0 to G2POCR7 and G3POCR0 to G3POCR7 Registers

Group i Waveform Generation Register j (i=0 to 3; j=0 to 7)



Symbol	Address	After Reset
G0PO0 to G0PO2	$00C1_{16}$-$00C0_{16}$, $00C3_{16}$-$00C2_{16}$, $00C5_{16}$-$00C4_{16}$	Indeterminate
G0PO3 to G0PO5	$00C7_{16}$-$00C6_{16}$, $00C9_{16}$-$00C8_{16}$, $00CB_{16}$-$00CA_{16}$	Indeterminate
G0PO6 to G0PO7	$00CD_{16}$-$00CC_{16}$, $00CF_{16}$-$00CE_{16}$	Indeterminate
G1PO0 to G1PO2	0101_{16}-0100_{16}, 0103_{16}-0102_{16}, 0105_{16}-0104_{16}	Indeterminate
G1PO3 to G1PO5	0107_{16}-0106_{16}, 0109_{16}-0108_{16}, $010B_{16}$-$010A_{16}$	Indeterminate
G1PO6 to G1PO7	$010D_{16}$-$010C_{16}$, $010F_{16}$-$010E_{16}$	Indeterminate
G2PO0 to G2PO2	0141_{16}-0140_{16}, 0143_{16}-0142_{16}, 0145_{16}-0144_{16}	Indeterminate
G2PO3 to G2PO5	0147_{16}-0146_{16}, 0149_{16}-0148_{16}, $014B_{16}$-$014A_{16}$	Indeterminate
G2PO6 to G2PO7	$014D_{16}$-$014C_{16}$, $014F_{16}$-$014E_{16}$	Indeterminate
G3PO0 to G3PO2	0181_{16}-0180_{16}, 0183_{16}-0182_{16}, 0185_{16}-0184_{16}	Indeterminate
G3PO3 to G3PO5	0187_{16}-0186_{16}, 0189_{16}-0188_{16}, $018B_{16}$-$018A_{16}$	Indeterminate
G3PO6 to G3PO7	$018D_{16}$-$018C_{16}$, $018F_{16}$-$018E_{16}$	Indeterminate

Function	Setting Range	RW
• When the RLD bit in the GiPOCRj register is set to "0", value written is immediately reloaded into the GiPOj register to output, for example, a waveform reflecting the value • When the RLD bit is set to "1", the value is reloaded when the base timer is reset. The value written can be read until reload.	0000_{16} to $FFFF_{16}$	RW

Group 3 Waveform Generation Mask Register j (j=4 to 7)

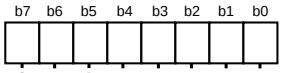
Symbol	Address	After Reset
G3MK4, G3MK5	0199_{16}-0198_{16}, $019B_{16}$-$019A_{16}$	Indeterminate
G3MK6, G3MK7	$019D_{16}$-$019C_{16}$, $019F_{16}$-$019E_{16}$	Indeterminate

Function	Setting Range	RW
When one or more bit k (k=0 to 15) in this register is set to "1", the bit k in the group 3 base timer is masked. The masked value is compared to the G3POj register(1).	0000_{16} to $FFFF_{16}$	RW

NOTES:
1. This function is enabled in single-phase waveform output mode or phase-delayed waveform output mode. Set the G3MKi register to "0000_{16}" in other modes.

Figure 21.13 G0PO0 to G0PO7, G1PO0 to G1PO7, G2PO0 to G2PO7, G3PO0 to G3PO7 Registers and G3MK4 to G3MK7 Registers

Group i Function Select Register (i=0, 1)

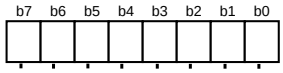


Symbol	Address	After Reset
G0FS, G1FS	$00E7_{16}$, 0127_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
FSC0	Channel 0 Time Measurement/ Waveform Generation Function Select Bit	0 : Selects the waveform generation function 1 : Selects the time measurement function	RW
FSC1	Channel 1 Time Measurement/ Waveform Generation Function Select Bit		RW
FSC2	Channel 2 Time Measurement/ Waveform Generation Function Select Bit		RW
FSC3	Channel 3 Time Measurement/ Waveform Generation Function Select Bit		RW
FSC4	Channel 4 Time Measurement/ Waveform Generation Function Select Bit		RW
FSC5	Channel 5 Time Measurement/ Waveform Generation Function Select Bit		RW
FSC6	Channel 6 Time Measurement/ Waveform Generation Function Select Bit		RW
FSC7	Channel 7 Time Measurement/ Waveform Generation Function Select Bit		RW

NOTES:
1. No 16-bit waveform generation function is provided for channels 2, 3, 6 and 7 of the group 0. No 16-bit time measurement function is provided for channels 0, 3, 4 and 5 of the group 1. When the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement or waveform generation function), set the same values in the G0FS and G1FS registers.

Group i Function Enable Register (i=0 to 3)

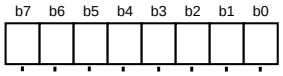


Symbol	Address	After Reset
G0FE to G3FE	$00E6_{16}$, 0126_{16}, 0166_{16}, $01A6_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
IFE0	Channel 0 Function Enable Bit	0 : Disables functions for channel j 1 : Enables functions for channel j (j=0 to 7)	RW
IFE1	Channel 1 Function Enable Bit		RW
IFE2	Channel 2 Function Enable Bit		RW
IFE3	Channel 3 Function Enable Bit		RW
IFE4	Channel 4 Function Enable Bit		RW
IFE5	Channel 5 Function Enable Bit		RW
IFE6	Channel 6 Function Enable Bit		RW
IFE7	Channel 7 Function Enable Bit		RW

Figure 21.14 G0FS and G1FS Registers and G0FE to G3FE Registers

Group i RTP Output Buffer Register (i=2, 3)



Symbol	Address	After Reset
G2RTP, G3RTP	0167_{16}, $01A7_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
RTP0	Channel 0 RTP Output Buffer	0 : Outputs "L" 1 : Outputs "H"	RW
RTP1	Channel 1 RTP Output Buffer		RW
RTP2	Channel 2 RTP Output Buffer		RW
RTP3	Channel 3 RTP Output Buffer		RW
RTP4	Channel 4 RTP Output Buffer		RW
RTP5	Channel 5 RTP Output Buffer		RW
RTP6	Channel 6 RTP Output Buffer		RW
RTP7	Channel 7 RTP Output Buffer		RW

Figure 21.15 G2RTP AND G3RTP Registers

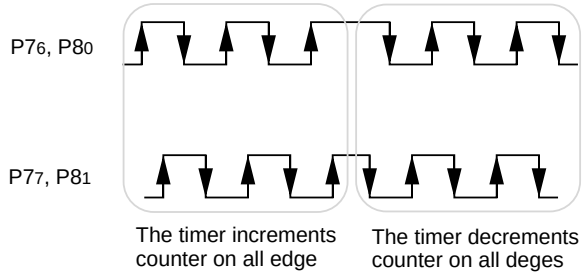
21.1 Base Timer

The base timer is a free-running counter that counts an internally generated count source.
Table 21.2 lists specifications of the base timer. Figures 21.5 to 21.9 show registers associated with the base timer. Figure 21.16 shows a block diagram of the base timer. Figure 21.17 shows an example of a cascaded connection. Figure 21.18 shows an example of the base timer in counter increment mode. Figure 21.19 shows an example of the base timer in counter increment/decrement mode. Figure 21.20 shows an example of two-phase pulse signal processing mode.

Table 21.2 Base Timer Specifications

Item	Specification
Count Source (f_{BTi}) (i=0 to 3)	f_1 divided by $2(n+1)$ (Group 0 to 3), two-phase pulse input divided by $2(n+1)$ (Group 0 and 1) n: determined by the DIV4 to DIV0 bits in the GiBCR0 register n=0 to 31; however no division when n=31
Counting Operation	The base timer increments the counter The base timer increments/decrements the counter Two-phase pulse signal processing
Counter Start Condition	• When starting the base timer of each group separately, set the BTS bit in the GiBCR1 register to "1" (base timer starts counting) • When starting the base timer of multiple groups simultaneously, set the BTiS bit in the BTSR register to "1" (base timer starts counting)
Counter Stop Condition	Set the BTiS bit in the BTSR register to "0" (base timer reset) and the BTS bit in the GiBCR1 register to "0" (base timer reset)
Base Timer Reset Condition	• Synchronized with the base timer reset in different groups: Group0 : synchronized with group 1 base timer reset Group1 : synchronized with group 0 base timer reset Group2 : synchronized with group 1 base timer reset Group3 : synchronized with group 2 base timer reset • Matching values in the base timer and GiPO0 register • "L" signal applied to the external interrupt pin Group 0 : $\overline{INT0}$ pin Group 1 : $\overline{INT1}$ pin • Reset request from communication function (Group 2 and 3)
Value when the Base Timer is Reset	"0000_{16}"
Interrupt Request	The BTiR bit in the interrupt request register is set to "1" (interrupt requested) when bit 14 or bit 15 in the base timer overflows (See Figure 10.14.)
Read from Base Timer	• The GiBT register indicates counter value while the base timer is running • The GiBT register is indeterminate when the base timer is reset
Write to Base Timer	When a value is written while the base timer is running, the counter immediately starts counting from this value. No value can be written while the base timer is reset.
Selectable Function	• Cascaded connection (Group 0 and 1) Group 1 base timer is incremented every time bit 15 in the group 0 base timer overflows (See Figure 21.17) • Counter increment/decrement mode (Group 0 and 1) The base timer starts when the BTS bit or the BTiS bit is set to "1". After incrementing to "$FFFF_{16}$", the counter is then decremented back to "0000_{16}". If the RST1 bit in the GiBCR1 register is set to "1" (the base timer is reset by matching with the GiPO0 register), the counter decrements after the base timer matches the GiPO0 register. The base timer increments the counter again when the counter becomes "0000_{16}." (See Figure 21.19.)

Table 21.2 Base Timer Specifications (Continued)

Item	Specification
Selectable Function	• Two-phase pulse processing mode (Group 0 and 1) Two-phase pulse signals from P7$_6$ and P7$_7$ pins in group 0, and P8$_0$ and P8$_1$ pins in group 1 are counted (See Figure 21.20) 

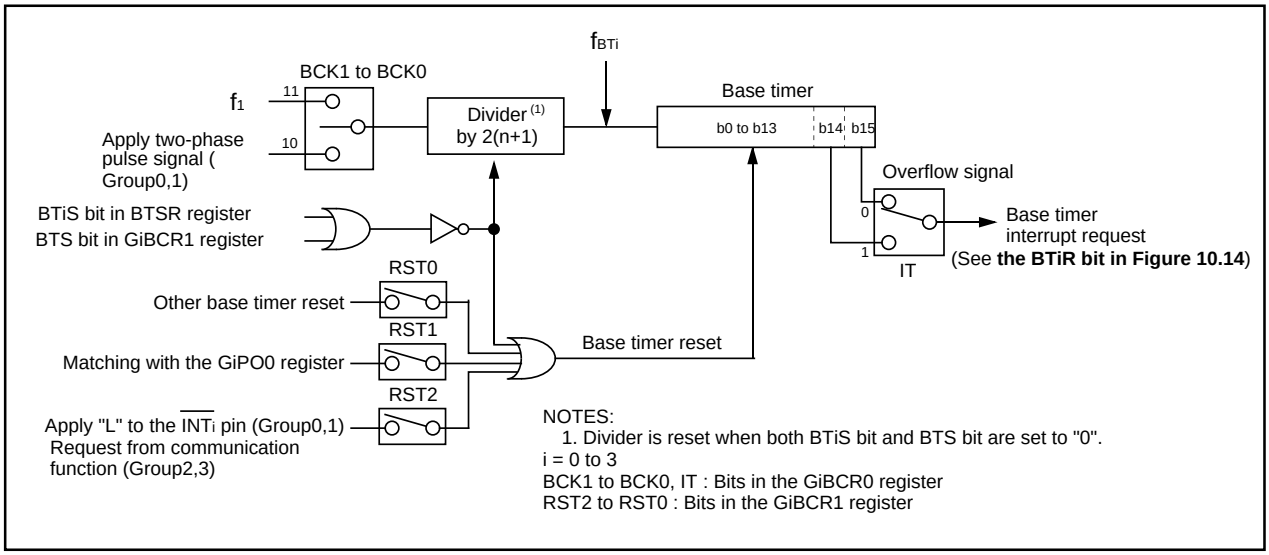


Figure 2116 Base Timer Block Diagram

Table 21.3 Base Timer Associated Register Settings
(for Time Measurement Function, Waveform Generation Function, and Communication Function)

Register	Bit	Function
G2BCR0	-	Supplies operation clock to the BTSR register. Set to "0111 1111$_2$".
BTSR	-	Set to "0000 0000$_2$"
GiBCR0	BCK1 to BCK0	Select count source
	DIV4 to DIV0	Select divide ratio of count source
	IT	Selects the base timer interrupt
GiBCR1	RST2 to RST1	Select factors for a base timer reset
	BTS	Used to start the base timer independently
	UD1 to UD0	Select how to count (Group 0 and 1)
	CAS	Selects cascaded connection (Group 0 and 1)
GiBT	-	Read or write base timer value

Set the following registers to set the RST1 bit to "1" (base timer reset by matching the base timer with the G1PO0 register).

GiPOCR0	MOD2 to MOD0	Set to "000$_2$" (single-phase waveform output mode)
GiPO0	-	Set reset cycle
GiFS	FSC0	Set to "0" (waveform generation function)
GiFE	IFE0	Set to "1" (channel operation start)

i : Bit configurations and functions vary with each group

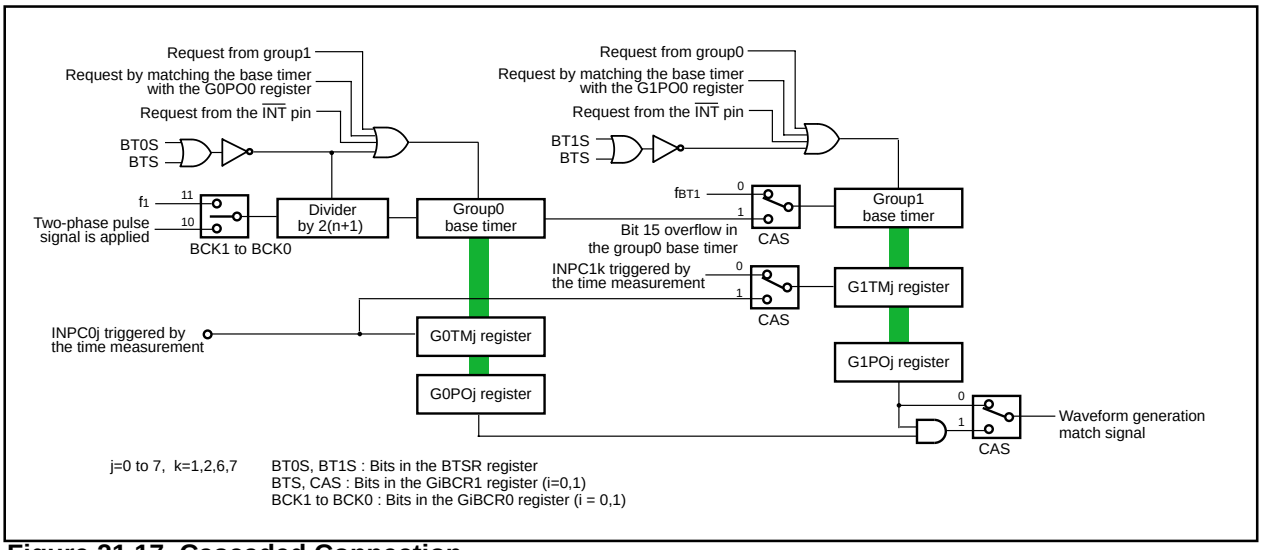
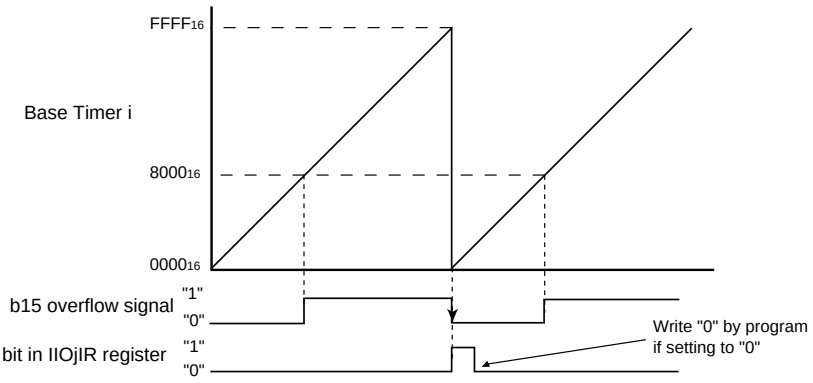


Figure 21.17 Cascaded Connection

(1) The IT in the GiBCR0 register (i=0,1) is set to "0" (bit 15 in the base timer overflows)

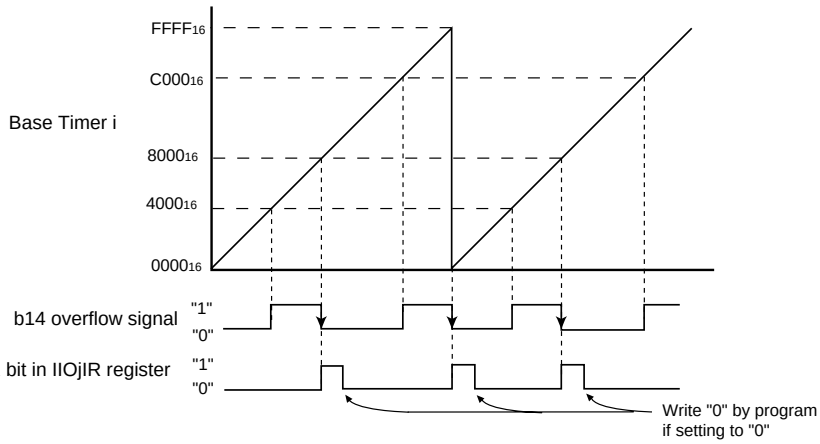


j=4,7,8,11 k=0 to 3

The above applies under the following conditions:

- The RST1 bit in the GiBCR1 register is set to "0" (the base timer is not reset by matching the base timer with the GiPO0 register)
- The UD1 to UD0 bits in the GiBCR1 register are set to "00$_2$" (counter increment mode)

(2) The IT in the GiBCR0 register (i=0,1) is set to "1" (bit 14 in the base timer overflows)



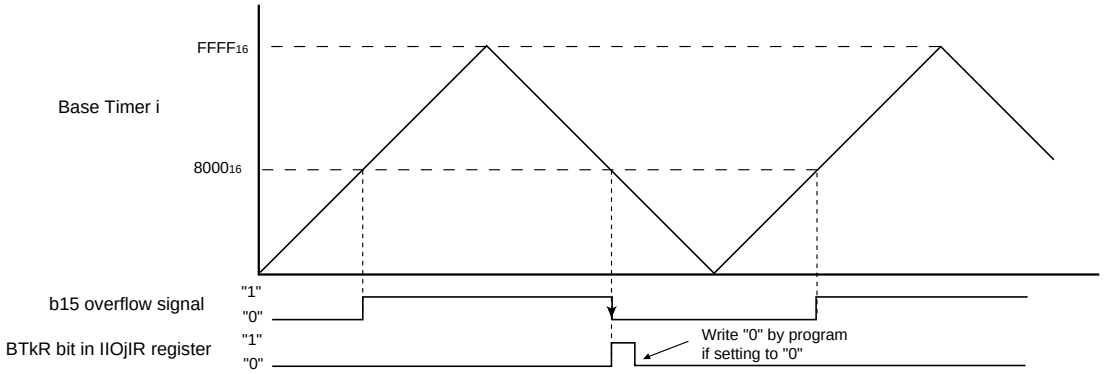
j=4,7,8,11 k=0 to 3

The above applies under the following conditions:

- The RST1 bit in the GiBCR1 register is set to "0" (the base timer is not reset by matching the base timer with the GiPO0 register)
- The UD1 to UD0 bits in the GiBCR1 register are set to "00$_2$" (counter increment mode)

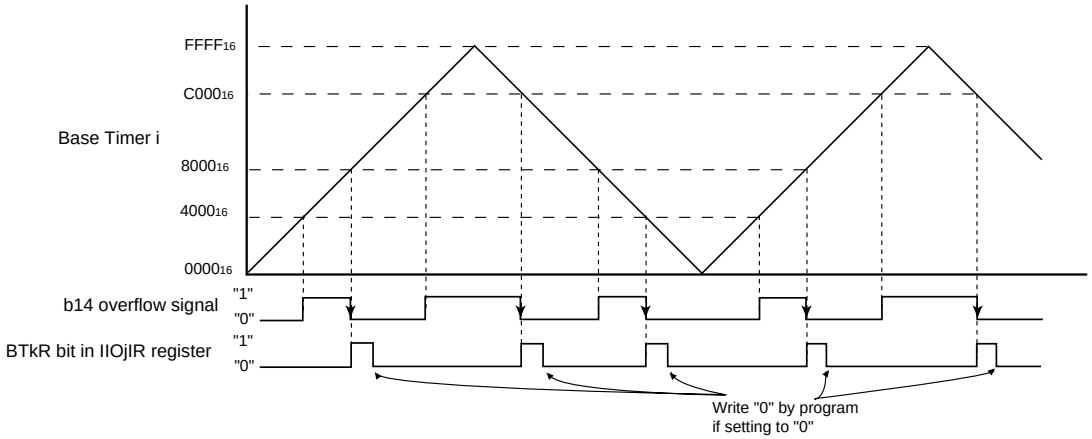
Figure 21.18 Counter Increment Mode (Group 0 and 1)

(1) When the IT bit in the GiBCR0 register (i= 0 to 1) is set to "0" (bit 15 in the base timer overflows)



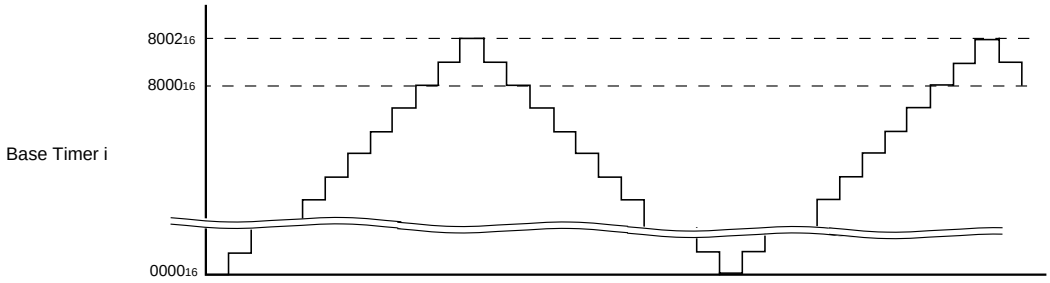
j=4, 7, 8, 11; k=0 to 3
The above applies under the following conditions:
• The RST1 in the GiBCR1 register is set to "0" (the base timer is not reset by matching the GiPO0 register).
• The UD1 to UD0 bits in the GiBCR1 register are set to "012" (counter increment/decrement mode).

(2) When the IT bit in the GiBCR0 register (i= 0 to 1) is set to "1" (bit 14 in the base timer overflows)



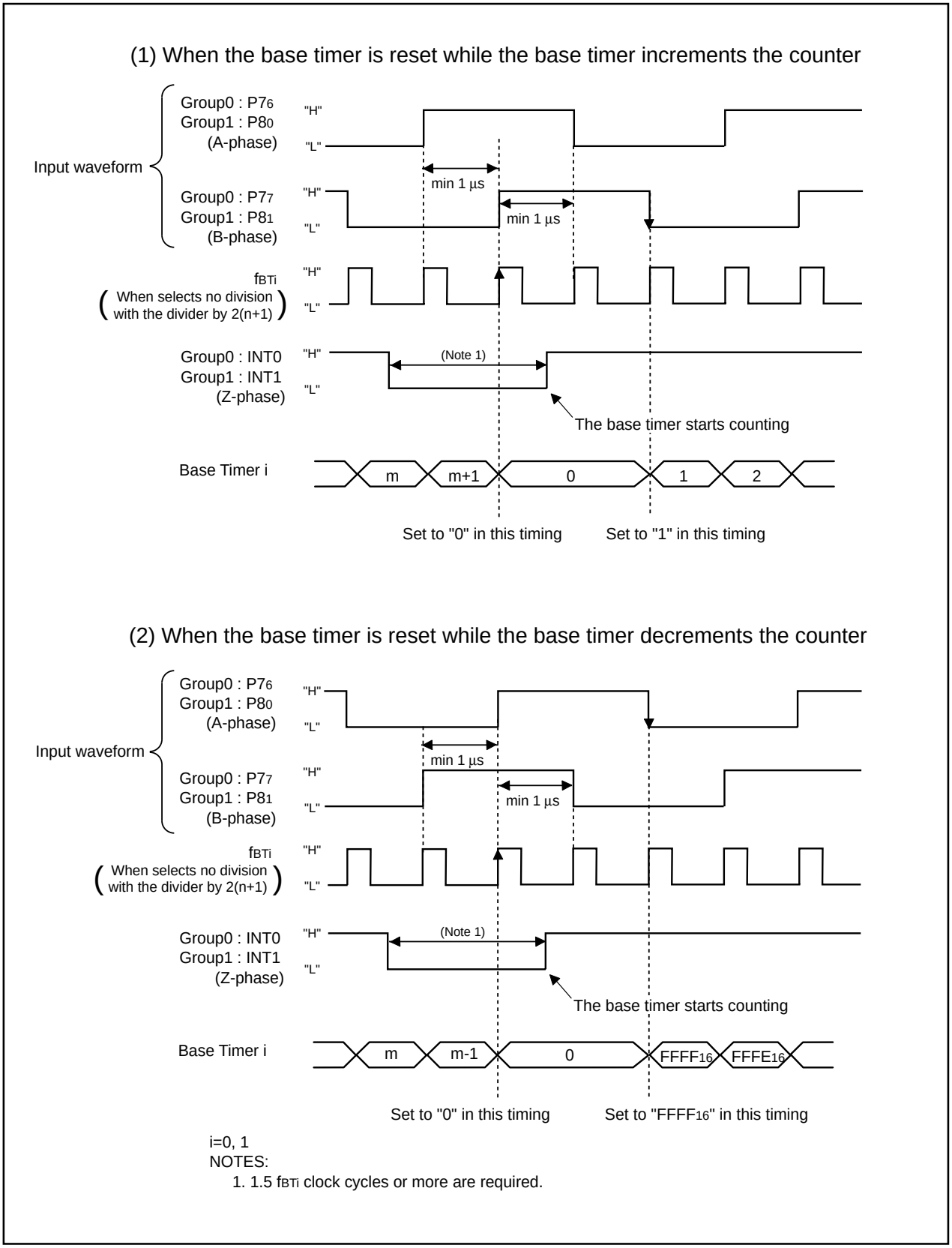
j=4, 7, 8, 11; k=0 to 3
The above applies under the following conditions:
• The RST1 in the GiBCR1 register is set to "0" (the base timer is not reset by matching the GiPO0 register).
• The UD1 to UD0 bits in the GiBCR1 register are set to "012" (counter increment/decrement mode).

(3) When the RST1 bit in the GiBCR1 register (i= 0 to 1) is set to "1" (the base timer is reset by matching with the GiPO0 register)



j=4, 7, 8, 11; k=0 to 3
The above applies under the following conditions:
• Value of GiPO0 register: "800016"
• The UD1 to UD0 bits in the GiBCR1 register are set to "012" (counter increment/decrement mode).

Figure 21.19 Counter Increment/ Decrement Mode (Group 0 and 1)



i=0, 1

NOTES:

1. 1.5 f_{BTi} clock cycles or more are required.

Figure 21.20 Base Timer Operation in Two-phase Pulse Signal Proccessing Mode (Group 0 and 1)

21.2 Time Measurement Function (Group 0 and 1)

When external trigger is applied, the value of the base timer is stored into the GiTMj register (i=0 to 1; j=0 to 7). Table 21.4 shows specifications of the time measurement function. Table 21.5 lists pin settings of the time measurement function. Table 21.6 lists settings of time measurement function associated registers. Figures 21.21 and 21.22 show operating examples of the time measurement function. Figure 21.23 shows an operating example of the prescaler function and gate function.

Table 21.4 Time Measurement Function Specifications

Item	Specification
Measurement Channel	Group 0: Channel 0 to 7 Group 1: Channel 1, 2, 6, 7
Trigger Input Polarity	Rising edge, falling edge or both edges of the INPCij pin(1)
Measurement Start Condition	The IFEj bit in the GiFE register is set to "1" (channel j function enabled) when the FSCj bit (i=0 to1; j=0 to 7) in the GiFS register is set to "1" (time measurement function selected)
Measurement Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Time Measurement Timing	• No prescaler : every time a trigger signal is applied • Prescaler (for channel 6 and channel 7): every *GiTPRk register (k=6, 7) +1* times a trigger signal is applied
Interrupt Request Generation Timing	The TMijR bit in the interrupt request register (See Figure 10.14) is set to "1" (interrupt requested) at time measurement timing
INPCij Pin Function(1)	Trigger input pin
Selectable Function	• Digital filter function The digital filter samples a trigger input signal level every f_1 or f_{BTi} cycles and passes pulse signals that match trigger input signal level three times • Cascaded connection function Group 0 and group 1 are connected to operate as a 32-bit base timer • Prescaler function (for channel 6 and channel 7) Time measurement is executed every *GiTPRk register value +1* times a trigger signal is applied • Gate function (for channel 6 and channel 7) After time measurement by the first trigger input, trigger input cannot be received. However, trigger input can be received again by matching the base timer with the GiPOp register, or by setting the GSC bit in the GiTMCRK register to "1", when the GOC bit in the GiTMCRk register is set to "1" (gate cleared by matching the base timer with the GiPOp register (p=4 when k=6, p=5 when k=7))

NOTES:

1. $INPC0_0$ to $INPC0_7$, $INPC1_1$ to $INPC1_2$, $INPC1_6$ to $INPC1_7$ pins ($INPC0_0$ to $INPC0_7$ pins during cascaded connection)

Table 21.5 Pin Settings for Time Measurement Function

Pin(2)	Bit and Setting		
	PS1, PS2, PS5, PS8, PS9 Registers	PD7, PD8, PD11, PD14, PD15 Registers	IPS Register
P74/INPC11	PS1_4 = 0	PD7_4 = 0	IPS1 = 0
P75/INPC12	PS1_5 = 0	PD7_5 = 0	
P76/INPC00	PS1_6 = 0	PD7_6 = 0	IPS0 = 0
P77/INPC01	PS1_7 = 0	PD7_7 = 0	
P80/INPC02	PS2_0 = 0	PD8_0 = 0	
P111/INPC11(1)	PS5_1 = 0	PD11_1 = 0	IPS1 =1
P112/INPC12(1)	PS5_2 = 0	PD11_2 = 0	
P142/INPC16(1)	PS8_2 = 0	PD14_2 = 0	—
P143/INPC17(1)	PS8_3 = 0	PD14_3 = 0	
P150/INPC00(1)	PS9_0 = 0	PD15_0 = 0	IPS0 = 1, IPS2 = 0
P151/INPC01(1)	PS9_1 = 0	PD15_1 = 0	
P152/INPC02(1)	—	PD15_2 = 0	
P153/INPC03(1)	—	PD15_3 = 0	IPS2 = 0
P154/INPC04(1)	PS9_4 = 0	PD15_4 = 0	
P155/INPC05(1)	PS9_5 = 0	PD15_5 = 0	
P156/INPC06(1)	—	PD15_6 = 0	
P157/INPC07(1)	—	PD15_7 = 0	

NOTES:

1. This port is provided in the 144-pin package only.
2. Apply trigger to INPC0j pin (j=0 to 7) when the CAS bit in the GiBCR register is set to "1" (32-bit time measurement function). Trigger input to INPC1k pin (k=1, 2, 6, 7) is invalid.

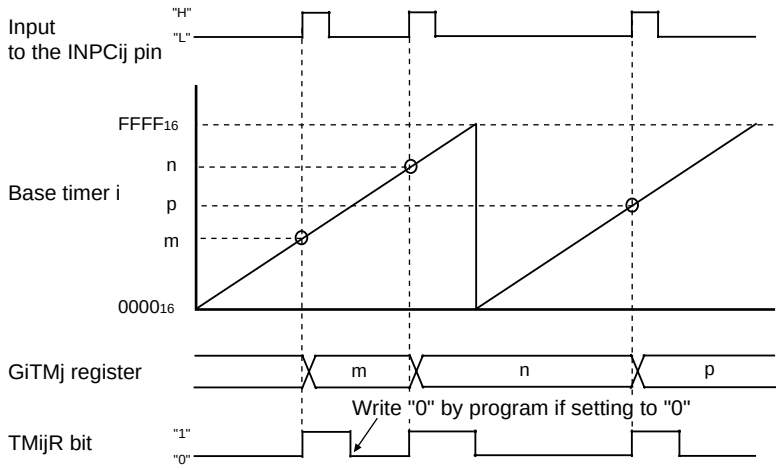
Table 21.6 Time Measurement Function Associated Register Settings

Register	Bit	Function
GiTMCRj	CTS1 to CTS0	Select a time measurement trigger
	DF1 to DF0	Select the digital filter function
	GT, GOC, GSC	Select the gate function
	PR	Select the prescaler function
GiTPRk	-	Setting value of the prescaler
GiFS	FSCj	Set to "1" (time measurement function)
GiFE	IFEj	Set to "1" (channel j function enabled)

i = 0 to 1; j = 0 to 7; k = 6, 7

Bit configurations and functions vary with channels and groups used.

Set registers associated with the time measurement function after setting registers associated with the base timer.



i=0,1 j=0 to 7 (except j=1, 2, 6, 7 when i=1)
TMijR bit : Bits in the IIO0IIR to IIO8IR and IIO10IR to IIO11IR registers

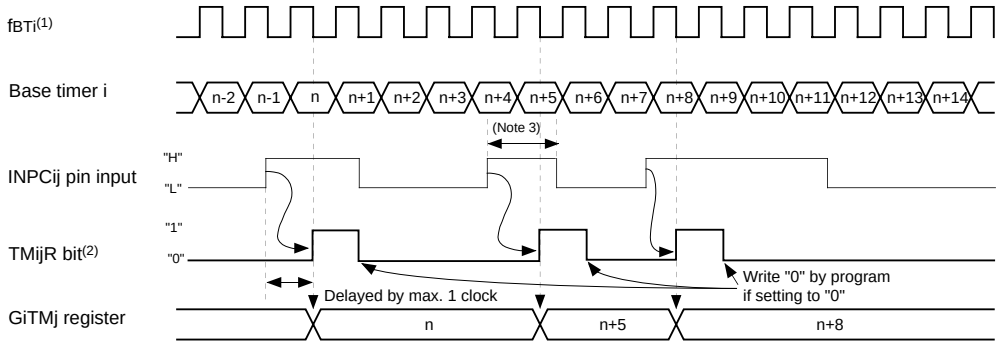
The above applies under the following conditions:

- The CTS1 to CTS0 bits in the GiTMCRj register are set to "01$_2$" (rising edge). The PR bit is set to "0" (no prescaler used) and the GT bit is set to"0" (no gate function used).
- The RTS2 to RTS0 bits in the GiBCR1 register are set to "000$_2$" (no base timer reset). The UD1 to UD0 bits are set to "00$_2$" (counter increment mode) and the CAS bit is set to "0" (16-bit time measurement or waveform generation function).

To set the base timer to "0000$_{16}$" (setting the RST1 bit to "1" and the RST0 and RST2 bits to "0") when the base timer matches the GiPO0 register, the base timer is set to "0000$_{16}$" after it reaches *the value set in the GiPO0 register + 2*.

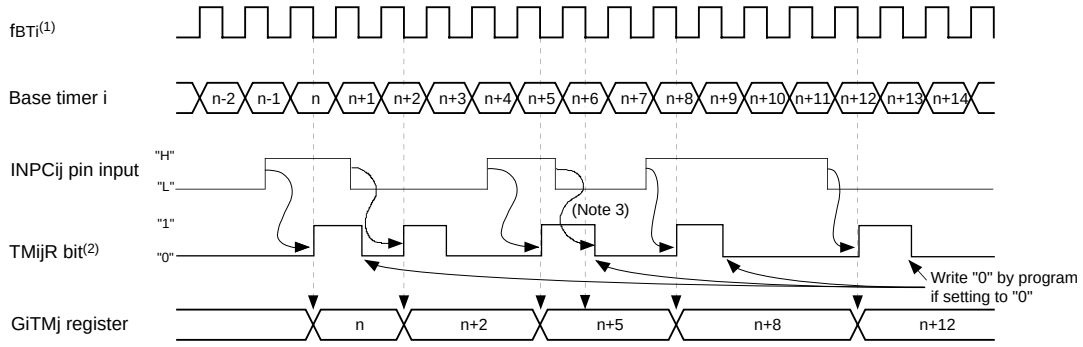
Figure 21.21 Time Measurement Function (1)

(1) When selecting the rising edge as a time measurement trigger
(The CTS1 to CTS0 bits in the GiTMCR register (i=0,1, j=0 to 7)=01$_2$)



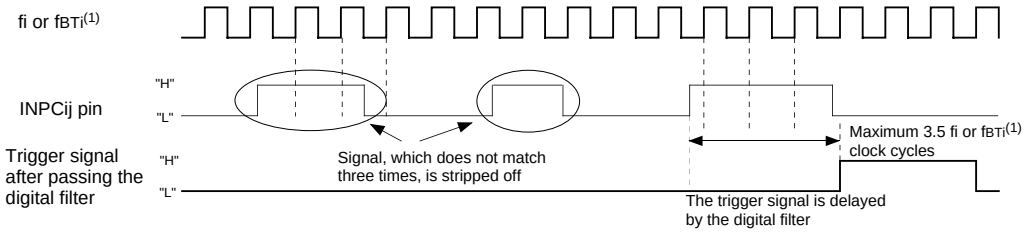
NOTES:
1. If the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement), the group 1 base timer increments counter every time the group 0 base timer overflows.
2. Bits in the IIO0IR to IIO8IR, IIO10IR to IIO11R registers. The TM0jR bit if the CAS bit is set to "1".
3. Input pulses applied to the INPCij pin require 1.5 fBTi clock cycles or more.

(2) When selecting both edges as a time measurement trigger
(The CTS1 to CTS0 bits=11$_2$)



NOTES:
1. If the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement), the group 1 base timer increments the counter whenever the group 0 base timer overflows.
2. Bits in the IIO0IR to IIO8IR, IIO10IR to IIO11R registers. The TM0jR register if the CAS bit is set to "1".
3. No interrupt is generated if the microcomputer receives a trigger signal when the TMijR bit is set to "1". Howver, the value of the GiTMj register changes.

(3) Trigger signal when using the digital filter
(The DF1 to DF0 bits in the GiTMCR register =10$_2$ or 11$_2$)

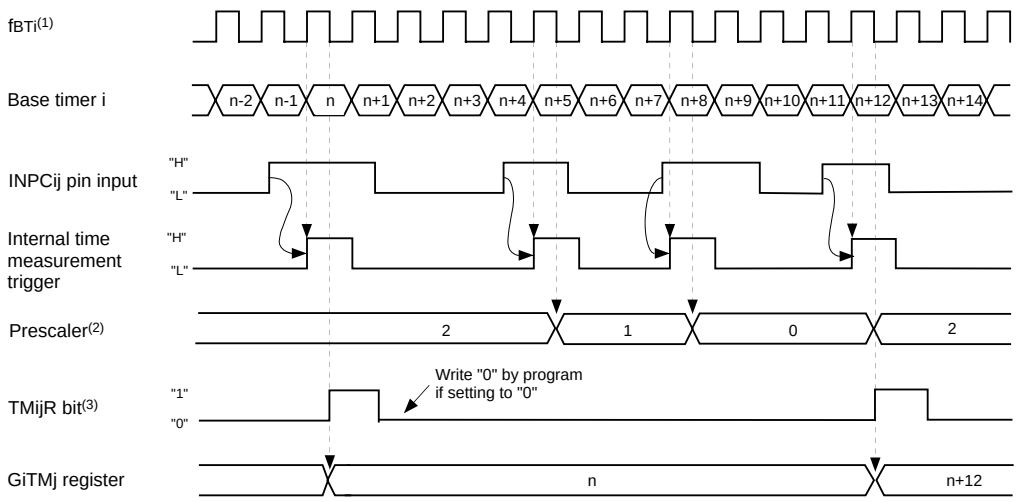


NOTES:
1. fBTi when the DF1 to DF0 bits are set to "10$_2$", and f1 when to "11$_2$".

Figure 21.22 Time Measurement Function (2)

(1) With the prescaler function

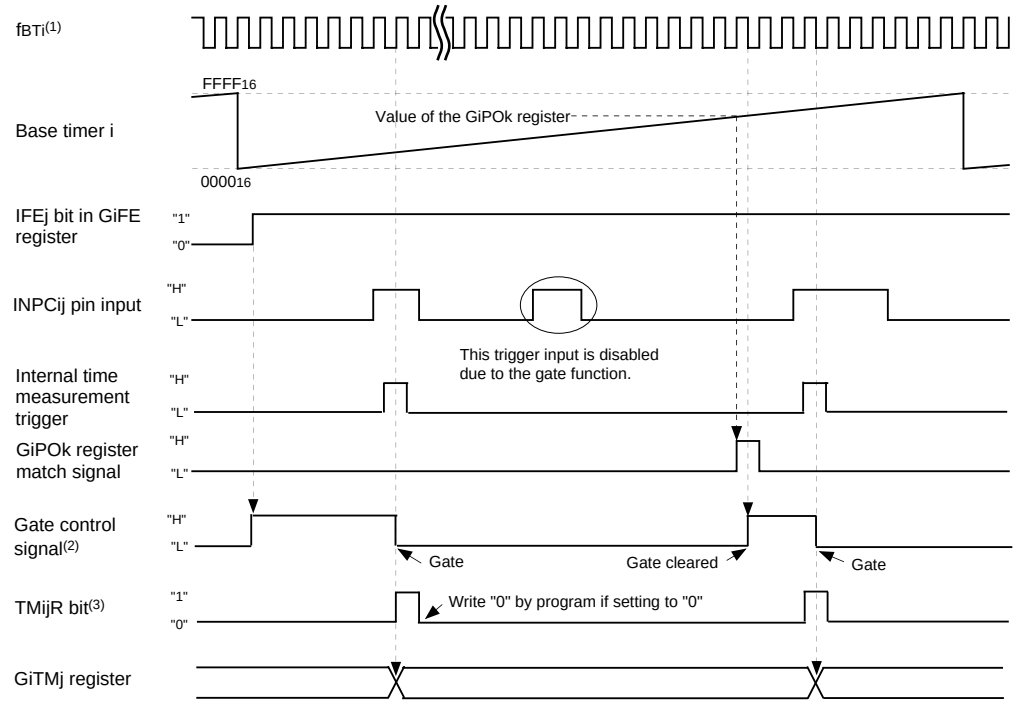
(When the GiTPRj register (i=0, 1, j=6, 7) =02$_{16}$, the PR bit in the GiTMCR register=1)



NOTES:
1. If the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement), the group 1 base timer increments the counter every time the group 0 base timer overflows.
2. This applies to the second or later prescaler cycles after the PR bit in the GiTMCRj register is set to "1".
3. Bits in the IIO0IR to IIO8IR, IIO10IR to IIO11IR registers. The TM0jR register if the CAS bit is set to "1".

(2) With the gate function

(The gate function is cleared by matching the base timer with the GiPOk register.
the GT bit in the GiTMCRj register=1, the GOC bit=1)



NOTES:
1. If the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement), the group 1 base timer increments the counter every time the group 0 base timer overflows.
2. Bits in the IIO0IR to IIO8IR, IIO10IR to IIO11IR registers. The TM0jR register if the CAS bit is set to "1".

Figure 21.23 Prescaler Function and Gate Function

21.3 Waveform Generation Function

Waveforms are generated when the value of the base timer matches the GiPOj register (i=0 to 3; j=0 to 7).
The waveform generation function has the following six modes :

- Single-phase waveform output mode (group 0 to 3)
- Phase-delayed waveform output mode (group 0 to 3)
- Set/Reset waveform output (SR waveform output) mode (group 0 to 3)
- Bit modulation PWM output mode (group 2 and 3)
- Real-time port output (RTP output) mode (group 2 and 3)
- Parallel real-time port output (parallel RTP output) mode (group 2 and 3)

Table 21.7 lists pin settings of the waveform generation function. Table 21.8 lists registers associated with the waveform generation function.

Table 21.7 Pin Settings for Waveform Generation Function (1/2)

Pin	Bit and Setting		
	PS0 to PS2, PS5 to PS9 Registers	PSL0, PSL1, PSL2 Registers	PSC Register
P64/OUTC21	PS0_4 = 1	PSL0_4 = 1	-
P70/OUTC20	PS1_0 = 1	PSL1_0 = 0	PSC_0 = 1
P71/OUTC22	PS1_1 = 1	PSL1_1 = 0	PSC_1 = 1
P73/OUTC10(2)	PS1_3 = 1	PSL1_3 = 0	PSC_3 = 1
P74/OUTC11(2)	PS1_4 = 1	PSL1_4 = 0	PSC_4 = 1
P75/OUTC12(2)	PS1_5 = 1	PSL1_5 = 1	-
P76/OUTC00(2)	PS1_6 = 1	PSL1_6 = 0	PSC_6 = 0
P77/OUTC01(2)	PS1_7 = 1	-	-
P81/OUTC30	PS2_1 = 1	PSL2_1 = 1	-
P82/OUTC32	PS2_2 = 1	PSL2_2 = 0	-
P92/OUTC20	PS3_2 = 1	PSL3_2 = 1	-
P110/OUTC10(1,2)	PS5_0 = 1	-	-
P111/OUTC11(1,2)	PS5_1 = 1		
P112/OUTC12(1,2)	PS5_2 = 1		
P113/OUTC13(1,2)	PS5_3 = 1		
P120/OUTC30(1)	PS6_0 = 1	-	-
P121/OUTC31(1)	PS6_1 = 1		
P122/OUTC32(1)	PS6_2 = 1		
P123/OUTC33(1)	PS6_3 = 1		
P124/OUTC34(1)	PS6_4 = 1		
P125/OUTC35(1)	PS6_5 = 1		
P126/OUTC36(1)	PS6_6 = 1		
P127/OUTC37(1)	PS6_7 = 1		
P130/OUTC24(1)	PS7_0 = 1	-	-
P131/OUTC25(1)	PS7_1 = 1		

NOTES:
1. This port is provided in the 144-pin package only.
2. When the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement function), the OUTC1j pin (j=0 to 7) outputs a waveform and the OUTC0k pin (k=0, 1, 4, 5), set as above, outputs a 16-bit low-order waveform.

Table 21.7 Pin Settings for Waveform Generation Function (2/2)

Pin	Bit and Setting		
	PS0 to PS2, PS5 to PS9 Registers	PSL0, PSL1, PSL2 Registers	PSC Register
P13$_2$/OUTC2$_6$(1)	PS7_2 = 1	-	-
P13$_3$/OUTC2$_3$(1)	PS7_3 = 1		
P13$_4$/OUTC2$_0$(1)	PS7_4 = 1		
P13$_5$/OUTC2$_2$(1)	PS7_5 = 1		
P13$_6$/OUTC2$_1$(1)	PS7_6 = 1		
P13$_7$/OUTC2$_7$(1)	PS7_7 = 1		
P14$_0$/OUTC1$_4$(1,2)	PS8_0 = 1	-	-
P14$_1$/OUTC1$_5$(1,2)	PS8_1 = 1		
P14$_2$/OUTC1$_6$(1,2)	PS8_2 = 1		
P14$_3$/OUTC1$_7$(1,2)	PS8_3 = 1		
P15$_0$/OUTC0$_0$(1,2)	PS9_0 = 1	-	-
P15$_1$/OUTC0$_1$(1,2)	PS9_1 = 1		
P15$_4$/OUTC0$_4$(1,2)	PS9_4 = 1		
P15$_5$/OUTC0$_5$(1,2)	PS9_5= 1		

NOTES:
1. This port is provided in the 144-pin package only.
2. When the CAS bit in the GiBCR1 register is set to "1" (32-bit time measurement function), the OUTC1j pin (j=0 to 7) outputs a waveform and the OUTC0k pin (k=0, 1, 4, 5), set as above, outputs a 16-bit low-order waveform.

Table 21.8 Waveform Generation Function Associated Register Settings

Register	Bit	Function
GiPOCRj	MOD2 to MOD0	Select waveform output mode
	PRT(1)	Set to "1" when using the parallel RTP output mode
	IVL	Select default value
	RLD	Select reload timing of GiPOj register value
	RTP(1)	Set to "1" when using the RTP output or the parallel RTP output mode MOD2 to MOD0 bits are invalid when the RTP bit is set to "1"
	INV	Select inversed output
G2BCR1 G3BCR1	PRP	Set to "1" when using the parallel RTP output mode
GiPOj	-	Select output waveform inverse timing
G3MK4 to G3MK7	-	Set masked values of the base timer and G3PO4 to G3PO7 registers (group 3 only)
GiFS	FSCj	Set to "0" (waveform generation function) (group 0 and 1 only)
GiFE	IFEj	Set to "1" (enables channel j function)
G2RTP G3RTP	RTP0 to RTP7	Set RTP output value in RTP output or parallel RTP output mode

i = 0 to 3; j = 0 to 7

Bit configurations and functions vary with channels and groups used.

Set registers associated with the waveform generation function after setting registers associated with the base timer.

NOTES:
1. This bit is in the G2POCRj and G3POCRj registers only.

21.3.1 Single-Phase Waveform Output Mode (Group 0 to 3)

Output signal level of the OUTCij pin (i=0 to 3; j=0 to 7) becomes "H" when the value of the base timer matches that of the GiPOj register . The "H" signal switches to an "L" signal when the base timer reaches "0000_{16}". If the IVL bit in the GiPOCRj register is set to "1" (outputs "H" as initial value), an "H" signal is output when waveform output starts. If the INV bit is set to "1" (output is inversed), the level of the waveform being output is inversed. See Figure 21.24 for details on single-phase waveform mode operation. Table 21.9 lists specifications of single-phase waveform mode.

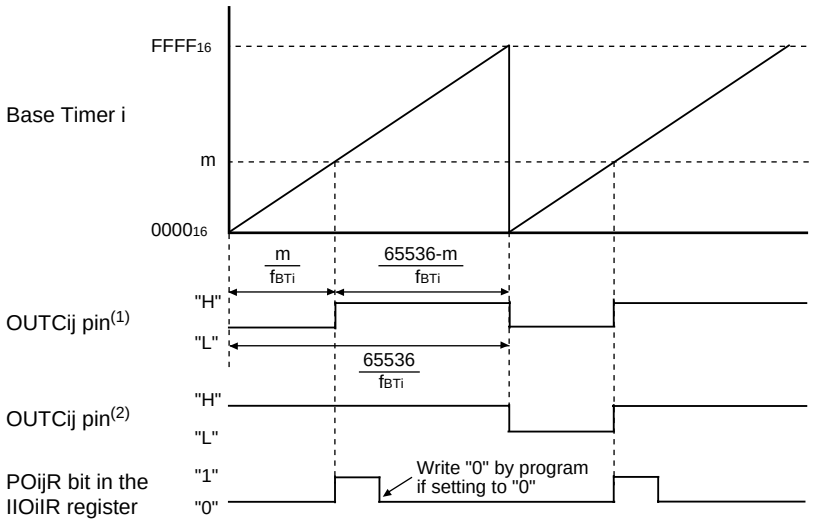
Table 21.9 Single-phase Waveform Output Mode Specifications

Item	Specification
Output Waveform(3)	• Free-running operation (the RST2 to RST0 bits in the GiBCR1 (i=0 to 3) register are set to "000_2") Cycle : $\frac{65536}{f_{BTi}}$ "L" width : $\frac{m}{f_{BTi}}$ "H" width : $\frac{65536-m}{f_{BTi}}$ m : setting value of the GiPOj register (j=0 to 7), 0000_{16} to $FFFF_{16}$ • The base timer is reset by matching the base timer with the GiPO0 register (the RST1 bit is set to "1", and the RST0 and the RST2 bit are set to "0") Cycle : $\frac{n+2}{f_{BTi}}$ "L" width : $\frac{m}{f_{BTi}}$ "H" width : $\frac{n+2-m}{f_{BTi}}$ m : setting value of the GiPOj register (j=1 to 7), 0000_{16} to $FFFF_{16}$ n : setting value of the GiPO0 register, 0001_{16} to $FFFD_{16}$ If m ≥ n+2, the output level is fixed to "L"
Waveform Output Start Condition(1)	The IFEj bit in the GiFE register is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the GiPOj register. (See Figure 10.14)
OUTCij Pin(2)	Pulse signal output pin
Selectable Function	• Default value set function : Set starting waveform output level • Inversed output function : Waveform output level is inversed and output from the OUTCij pin • Cascaded connection function: Connect group 0 and group 1 to operate as a 32-bit base timer

NOTES:

1. Set the FSCj bit in the GiFS register to "0" (waveform generation function selected) when using channels shared by both time measurement function and waveform generation function
2. $OUTC0_0$, $OUTC0_1$, $OUTC0_4$, $OUTC0_5$, $OUTC1_0$ to $OUTC1_7$, $OUTC2_0$ to $OUTC2_7$, and $OUTC3_0$ to $OUTC3_7$ pins ($OUTC1_0$ to $OUTC1_7$ pins when using group 0 and group 1 cascaded connection)
3. When the INV bit in the GiPOCRj register is set to "1" (output inversed), the "L" width and "H" width are inversed

(1) Free-Running Operation
(The RST2 to RST0 bits in the GiBCR1 register are set to "000$_2$")

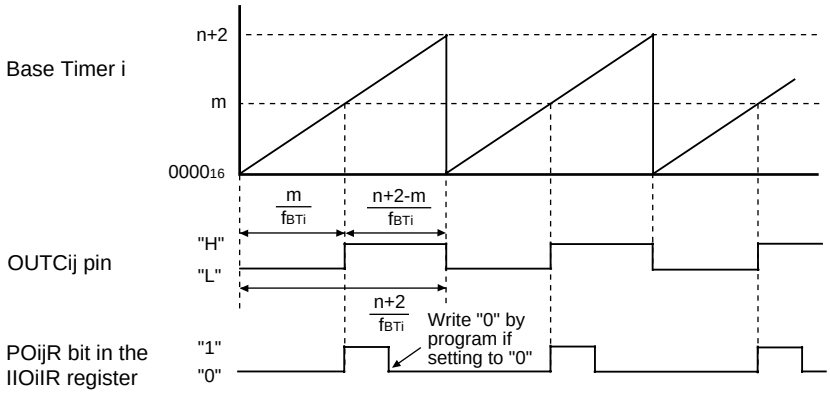


i=0 to 3; j=0 to 7 (however, i=0 when j=0, 1, 4, 5)
m : Setting value of the GiPOj register (0000$_{16}$ to FFFF$_{16}$)
POijR bit: Bits in the IIO0IR to IIO11IR register

NOTES:
1. Waveform output when the INV bit in the GiPOCRj register is set to "0" (not inversed) and the IVL bit is set to "0" (output "L" as initial value).
2. Waveform output when the INV bit is set to "0" (not inversed) and the IVL bit is set to "1" (output "H" as initial value).

The above applies applies under the following conditions:
- The RST2 to RST0 bits in the GiBCR1 register are set to "000$_2$" (no base timer reset), the UD1 to UD0 bits to "00$_2$" (counter increment mode), and CAS bit to "0" (16-bit waveform generation function)

(2) The Base Timer is Reset when the Base Timer Matches the GiPO0 Register
(The RST1 bit is set to "1", and the RST0 and RST2 bits are set to "0")



i=0 to 3; j=1 to 7 (however, i=0 when j=1, 4, 5)
m : Setting value of the GiPOj register (0000$_{16}$ to FFFF$_{16}$)
n : Setting value of the GiPO0 register (0001$_{16}$ to FFFD$_{16}$)
POijR bit: Bits in the IIO0IR to IIO11IR register

The above diagram applies under the following conditions:
- The IVL bit in the GiPOCRj register is set to "0" (outputs "L" as initial value). The INV bit is set to "0" (not inverse).
- The UD1 to UD0 bits in the GiBCR1 register are set to "00$_2$" (counter increment mode), and the CAS bit to "0" (16-bit waveform generation function)
- m < n+2

Figure 21.24 Single-Phase Waveform Output Mode

21.3.2 Phase-Delayed Waveform Output Mode (Group 0 to 3)

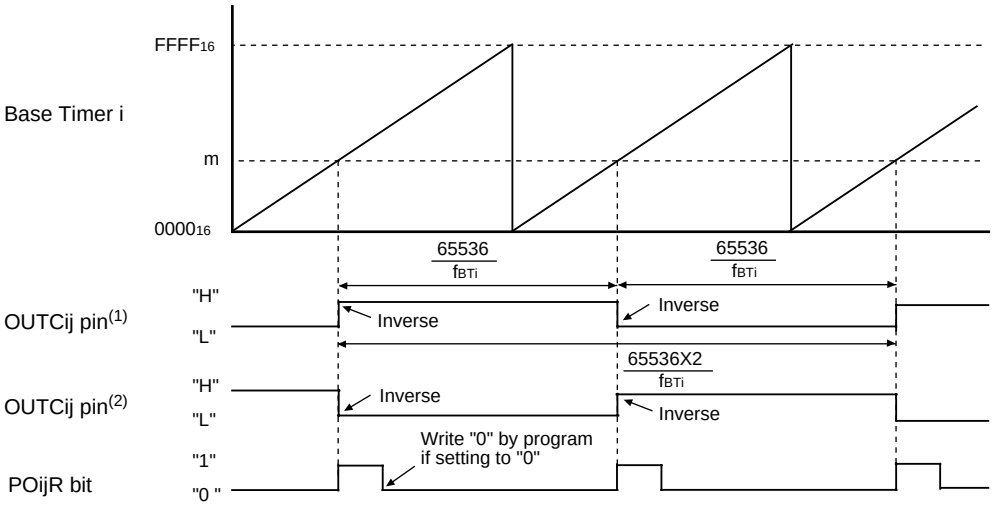
Output signal level of the OUTCij pin (i=0 to 3; j=0 to 7) is inversed every time the value of the base timer matches that of the GiPOj register. Table 21.10 lists specifications of phase-delayed waveform mode. Figure 21.25 shows an example of phase-delayed waveform mode operation.

Table 21.10 Phase-delayed Waveform Output Mode Specifications

Item	Specification
Output Waveform	• Free-running operation (the RST2 to RST0 bits in the GiBCR1 register (i=0 to 3) are set to "000$_2$") Cycle : $\frac{65536 \times 2}{f_{BTi}}$ "H" and "L" width : $\frac{65536}{f_{BTi}}$ Setting value of the GiPOj (j=0 to 7) register is 0000$_{16}$ to FFFF$_{16}$ • The base timer is reset by matching the base timer with the GiPO0 register (the RST1 bit is set to "1", and the RST0 and RST2 bit are set to "0") Cycle : $\frac{2(n+2)}{f_{BTi}}$ "H" and "L" width : $\frac{n+2}{f_{BTi}}$ n : setting value of the GiPO0 register, 0001$_{16}$ to FFFD$_{16}$ Setting value of the GiPOj (j=1 to 7) register is 0000$_{16}$ to FFFF$_{16}$ If GiPOj register ≥ n+2, the output level is not inversed
Waveform Output Start Condition(1)	The IFEj bit (j=0 to 7) in the GiFE register is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the GiPOj register. (See Figure 10.14)
OUTC1j Pin	Pulse signal output pin
Selectable Function	• Default value set function : Set starting waveform output level • Inversed output function : Waveform output level is inversed and output from the OUTCij pin • Cascaded connection function: Connect group 0 and group 1 to operate as a 32-bit base timer

NOTES:
1. Set the FSCj bit in the GiFS register to "0" (waveform generation function selected) when using channels shared by both time measurement function and waveform generation function
2. OUTC0$_0$, OUTC0$_1$, OUTC0$_4$, OUTC0$_5$, OUTC1$_0$ to OUTC1$_7$, OUTC2$_0$ to OUTC2$_7$, and OUTC3$_0$ to OUTC3$_7$ pins (OUTC1$_0$ to OUTC1$_7$ pins when using group 0 and group 1 cascaded connection)

(1) Free-Running Operation
(The RST2 to RST0 bits in the GiBCR1 register are set to "000$_2$")

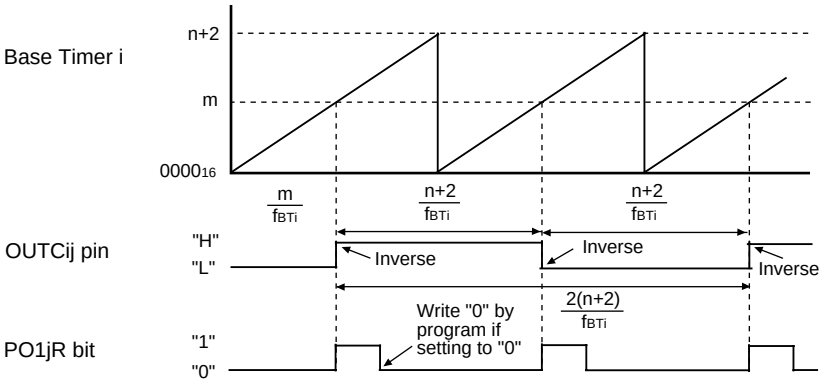


i=0 to 3; j=0 to 7 (however, i=0 when j= 0, 1, 4, 5)
m : Setting value of the GiPOj register (0000$_{16}$ to FFFF$_{16}$)
POijR bit: Bits in the IIO0IR to IIO11IR registers

NOTES:
1. Waveform output when the INV bit in the GiPOCRj register is set to "0" (not inversed) and the IVL bit is set to "0" (output "L" as initial value).
2. Waveform output when the INV bit is set to "0" (not inversed) and the IVL bit is set to "1" (output "H" as initial value).

The above diagram applies under the following condition:
- The RST2 to RST0 bits in the GiBCR1 register are set to "000$_2$" (no base timer reset), the UD1 to UD0 bits to "00$_2$" (counter increment mode), and the CAS bit to "0" (16-bit waveform generation function).

(2) The Base Timer is Reset when the Base Timer Matches the GiPO0 Register
(The RST1 bit is set to "1", and the RST0 and RST2 bits are set to "0")



i=0 to 3; j=0 to 7 (however, i=0 when j=1, 4, 5)
m : Setting value of the GiPOj register (0000$_{16}$ to FFFF$_{16}$)
n : Setting value of the GiPO0 register (0001$_{16}$ to FFFD$_{16}$)
POijR bit: Bits in the IIO0IR to IIO11IR registers

The above diagram applies under the following conditions:
- The IVL bit in the GiPOCRj register is set to "0" (outputs "L" as initial value). The INV bit is set to "0" (not inversed).
- The UD1 to UD0 bits in the G1BCR1 register are set to "00$_2$" (counter increment mode) and the CAS bit to "0" (16-bit waveform generation function).
- m < n+2

Figure 21.25 Phase-delayed Waveform Output Mode

21.3.3 Set/Reset Waveform Output (SR Waveform Output) Mode (Group 0 to 3)

Output signal level of the OUTCij pin (i=0 to 3; j=0, 2, 4, 6) becomes "H" when the value of the base timer matches that of the GiPOj register. The "H" signal switches to an "L" signal when the value of the base timer matches that of the GiPOk register (k=j+1) or when the base timer is set to "0000_{16}". If the IVL bit in the GiPOCRj register (j=0 to 7) is set to "1" (outputs "H" as initial value), an "H" signal is output when waveform output starts. If the INV bit is set to "1" (output is inversed), the level of the waveform being output is inversed. Table 21.11 lists specifications of SR waveform mode. Figure 21.26 shows an example of a SR waveform mode operation.

Table 21.11 SR Waveform Output Mode Specifications (1/2)

Item	Specification
Output Waveform(2)	• Free-running operation (the RST2 to RST0 bits in the GiBCR1 register are set to "000_2") (1) m < n "H" width : $\frac{n - m}{f_{BTi}}$ "L" width : $\frac{m^{(3)}}{f_{BTi}} + \frac{65536 - n^{(4)}}{f_{BTi}}$ (2) m ≥ n "H" width : $\frac{65536 - m}{f_{BTi}}$ "L" width : $\frac{m}{f_{BTi}}$ m : setting value of the GiPOj register (j=0, 2, 4, 6) n : setting value of the GiPOk register (k=j+1) m, n=0000_{16} to $FFFF_{16}$ • The base timer is reset by matching the base timer with the GiPO0 register(1) (the RST1 bit is set to "1", and the RST0 and RST2 bits are set to "0") (1) m < n < p+2 "H" width : $\frac{n-m}{f_{BTi}}$ "L" width : $\frac{m^{(3)}}{f_{BTi}} + \frac{p + 2 - n^{(4)}}{f_{BTi}}$ (2) m < p+2 ≤ n "H" width : $\frac{p + 2 - n}{f_{BTi}}$ "L" width : $\frac{m}{f_{BTi}}$ (3) If m ≥ p+2, the output level is fixed to "L" m : setting value of the GiPOj register (j=2, 4, 6) n : setting value of the GiPOk register (k=j+1) p : setting value of the GiPO0 register m, n=0000_{16} to $FFFF_{16}$ p=0001_{16} to $FFFD_{16}$

NOTES:
1. When the GiPO0 register resets the base timer, the channel 0 and 1 SR waveform generation functions are not available.
2. When the INV bit in the GiPOCRj register is set to "1" (output inversed), the "L" width and "H" width are inversed.
3. Waveform from base timer reset until when output level becomes "H".
4. Waveform from when output level becomes "L" until base timer reset.

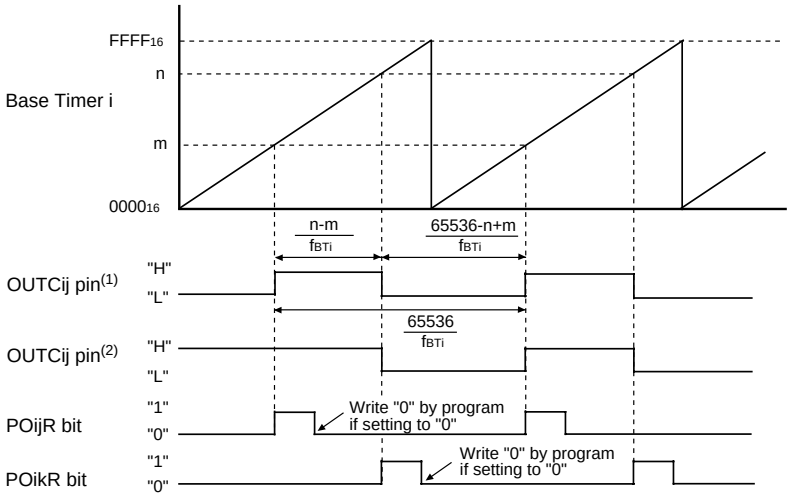
Table 21.11 SR Waveform Output Mode Specifications (2/2)

Item	Specification
Waveform Output Start Condition(5)	The IFEq bit (q=0 to 7) in the GiFE register is set to "1" (channel q function enabled)
Waveform Output Stop Condition	The IFEq bit is set to "0" (channel q function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the GiPOj register. The POikR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the GiPOk register. (See Figure 10.14)
OUTCij Pin(6)	Pulse signal output pin
Selectable Function	• Default value set function : Set starting waveform output level • Inversed output function : Waveform output level is inversed and output from the OUTCij pin • Cascaded connection function: Connect group 0 and group 1 to operate as a 32-bit base timer

NOTES:

5. Set the FSCj bit in the GiFS register to "0" (waveform generation function selected) when using channels shared by both time measurement function and waveform generation function
6. $OUTC0_0$, $OUTC0_4$, $OUTC1_0$, $OUTC1_2$, $OUTC1_4$, $OUTC1_6$, $OUTC2_0$, $OUTC2_2$, $OUTC2_4$, $OUTC2_6$, $OUTC3_0$, $OUTC3_2$, $OUTC3_4$, and $OUTC3_6$ pins
   ($OUTC1_0$, $OUTC1_2$, $OUTC1_4$, and $OUTC1_6$ pins when using group 0 and group 1 cascaded connection)

(1) Free-Running Operation
(The RST2 to RST0 bits in the GiBCR1 register are set to "000$_2$")

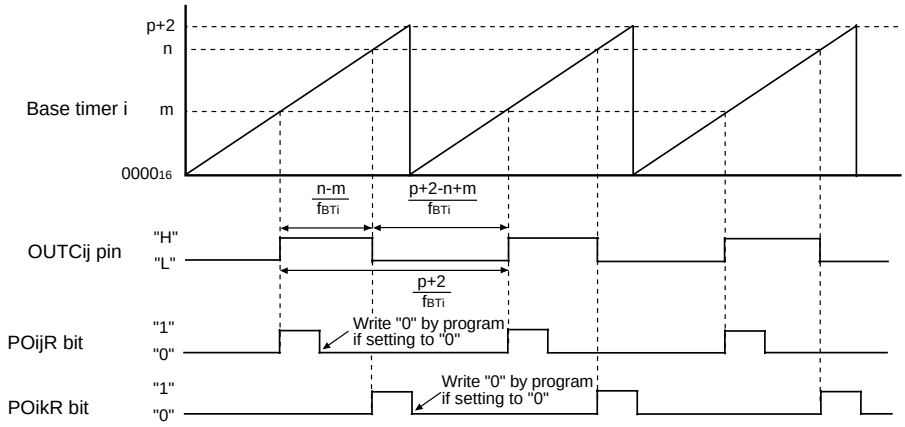


i=0, 3; j=0, 2, 4, 6 (however, i=0 when j=0, 4); k=j+1
m : Setting value of the GiPOj register (0000_{16} to $FFFF_{16}$)
n : Setting value of the GiPOk register (0000_{16} to $FFFF_{16}$)
POijR, POikR bits: Bits in the IIO0IR to IIO11IR registers

NOTES:
1. Waveform output when the INV bit in the GiPOCRj register is set to "0" (not inversed) and the IVL bit is set to "0" (output "L" as initial value).
2. Waveform output when the INV bit is set to "0" (not inversed) and the IVL bit is set to "1" (output "H" as initial value).

The diagram above applies under the following condition:
- The RST2 to RST0 bits in the GiBCR1 register are set to "000$_2$" (no base timer reset), the UD1 to UD0 bits to "00$_2$" (counter increment mode), and the CAS bit to "0" (16-bit waveform generation function).
- m < n

(2) The Base Timer is Reset when the Base Timer Matches the GiPO0 Register
(The RST1 bit is set to "1", and the RST0 and RST2 bits are set to "0")



i=0 to 3; j=2, 4, 6 (however, i=0 when j=4); k=j+1
m : Setting value of the GiPOj register (0000_{16} to $FFFF_{16}$)
n: Setting value of the GiPOk register (0000_{16} to $FFFF_{16}$)
p: Setting value of the GiPO0 register (0001_{16} to $FFFD_{16}$)
POijR, POikR bits: Bits in the IIO0IR to IIO11IR registers

The diagram above applies under the following conditions:
- The IVL bit in the GiPOCRk register is set to "0" (outputs "0" as an initial value). The INV bit is set to "0" (not inversed).
- The UD1 to UD0 bits in the GiBCR1 register are set to "00$_2$" (counter increment mode) and the CAS bit to "0" (16-bit waveform generation function).
- m < n < p+2

Figure 21.26 SR Waveform Output Mode

21.3.4 Bit Modulation PWM Output Mode (Group 2 and 3)

In bit modulation PWM output mode, PWM output has a 16-bit resolution. Pulses are output in repetitive cycles, each cycle consisting of span t repeated 1024 times. Span t, itself, has a cycle of $\frac{64}{f_{BTi}}$. The six high-order bits in the GiPOj register (i=2 to 3; j=0 to 7) determine the "L" base width. The 10 low-order bits determine the number of span t, within a cycle, in which "L" width is extended by the minimum resolution bit width (1 clock cycle). If the INV bit is set to "1" (output is inversed), the level of the waveform being output is inversed.

Table 21.12 lists specifications of bit modulation PWM output mode. Table 21.13 lists the number of modulated span and minimum resolution bit width altered span t. Figure 21.27 shows an example of bit modulation PWM mode operation.

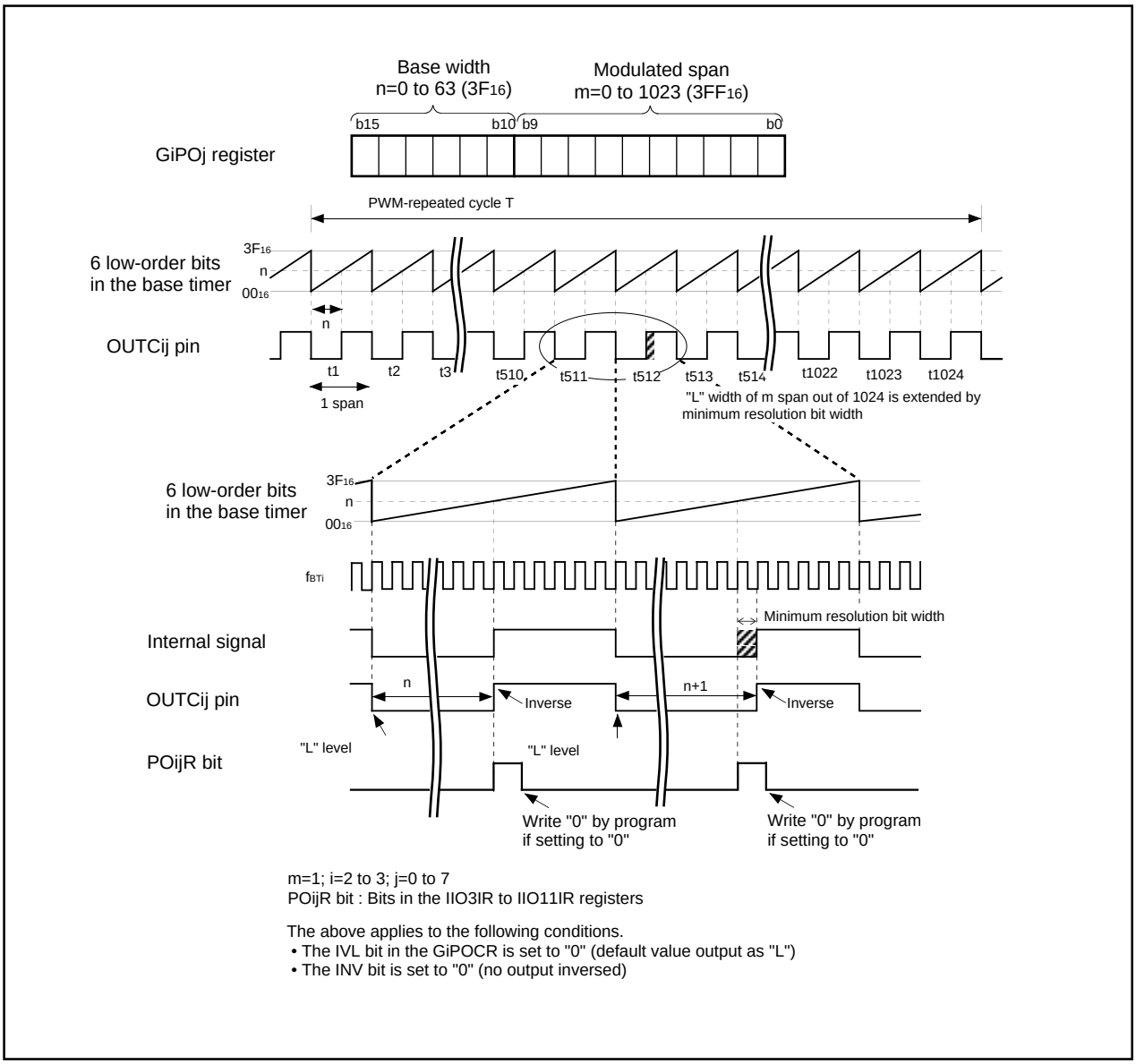
Table 21.12 Bit Modulation PWM Output Mode Specifications

Item	Specification
Output Waveform(1,2)	PWM-repeated cycle T: $\frac{65536}{f_{BTi}}$ (= $\frac{64}{f_{BTi}}$ X1024) Cycle of span t: $\frac{64}{f_{BTi}}$ "L" width: of m spans $\frac{n+1}{f_{BTi}}$ $\frac{n}{f_{BTi}}$ of (1024-m) spans Average "L" output width: $\frac{1}{f_{BTi}}$ X (n+ $\frac{m}{1024}$) n: Setting values (six high-order bits) of the GiPOj register (i=2 to 3; j=0 to 7) 00_{16} to $3F_{16}$ m: Setting values (ten low-order bits) of the GiPOj register 00_{16} to $3FF_{16}$
Waveform Output Start Condition	The IFEj bit in the GiFE register is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" when the value of the six low-order bits of the base timer matches those set in the six high-order bits of the GiPOj register (see Figure 10.14).
OUTCij Pin	Pulse signal output pin
Selectable Function	• Default value set function : Set starting waveform output level • Inversed output function : Waveform output level is inversed and output from the OUTCij pin

NOTES:
1. Set the RST2 to RST0 bits in the GiBCR1 register to "000_2" when using the bit modulation PWM mode.
2. When the INV bit in the GiPOCRj register is set to "1" (output inversed), the "L" width and "H" width are inversed.

Table 21.13. Number of Modulated Spans and Minimum Resolution Bit Width Extended Span t

Number of Modulated Spans	Minimum Resolution Bit Width Extended Span t
00 0000 0000_2	none
00 0000 0001_2	t512
00 0000 0010_2	t256, t768
00 0000 0100_2	t128, t384, t640, t896
00 0000 1000_2	t64, t192, t320, t448, t576, t704, t832, t960
⋮	⋮
10 0000 0000_2	t1, t3, t5, t7, ••• t1019, t1021, t1023



m=1; i=2 to 3; j=0 to 7
POijR bit : Bits in the IIO3IR to IIO11IR registers

The above applies to the following conditions.
- The IVL bit in the GiPOCR is set to "0" (default value output as "L")
- The INV bit is set to "0" (no output inversed)

Figure 21.27 Bit Modulation PWM Mode

21.3.5 Real-Time Port (RTP) Output Mode (Group 2 and 3)

The OUTCij pin outputs the value set in the GiRTP register in one-byte units by matching the value of the base timer with that of the GiPOj register (i=2 to 3, j=0 to 7). Table 21.14 lists specifications of RTP output mode. Figure 21.28 shows a block diagram of the RTP output function. Figure 21.29 shows an example of RTP output mode operation.

Table 21.14 RTP Output Mode Specifications

Item	Specification
Waveform Output Start Condition	The IFEj bit in the GiFE register (i=2 to 3, j=0 to 7) is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" when the value of the base timer matches that of the GiPOj register (0000_{16} to $FFFF_{16}$(1)). (See Figure 10.14.)
OUTCij Pin	RTP output pin
Selectable Function	• Default value set function : Set starting waveform output level • Inversed output function : Waveform output level is inversed and output from the OUTCij pin

NOTES:

1. Set the GiPO0 register to 0001_{16} to $FFFD_{16}$ when setting the base timer to "0000_{16}" (the RST1 bit in the GiBCR1 register is set to "1", and the RST0 and RST2 bits are set to "0") while the values in the base timer and the GiPO0 register match

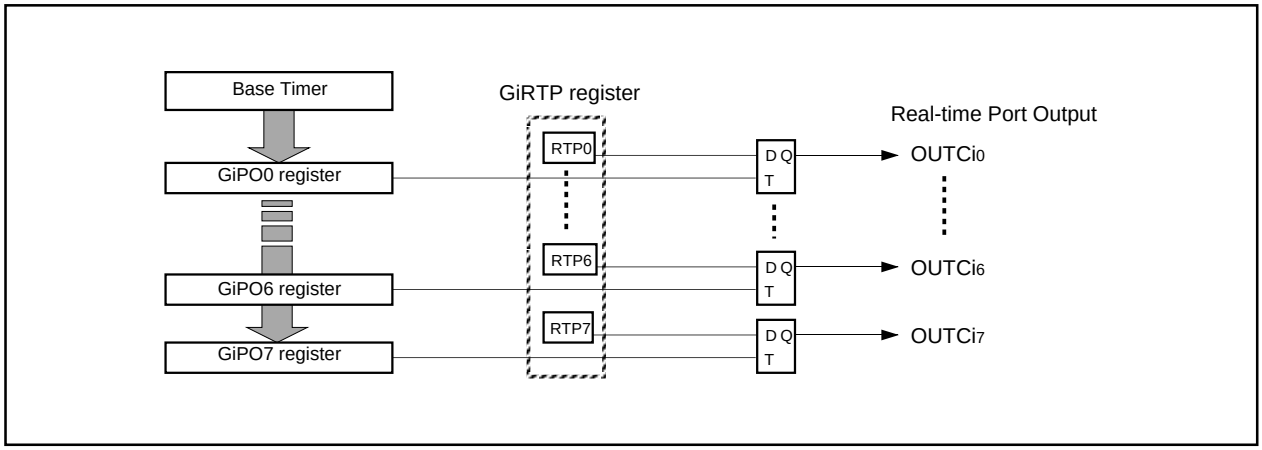
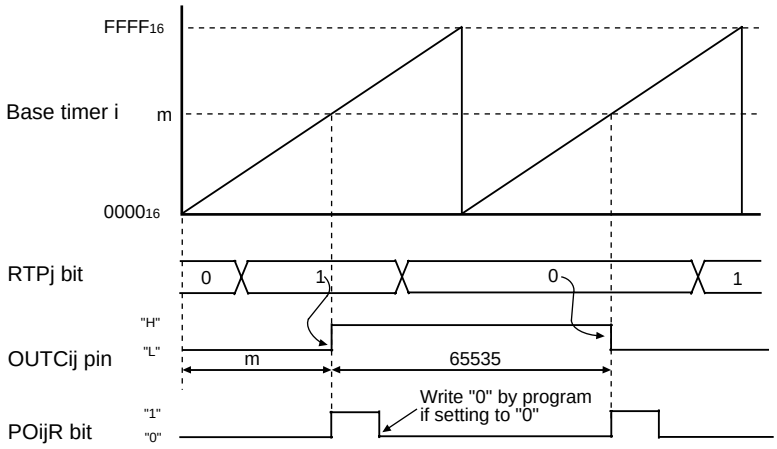


Figure 21.28 Real-time Port Output Function Block Diagram

(1) Free-running operation
(RST2 to RST0 bits in the GiBCR1 register are set to "000$_2$")

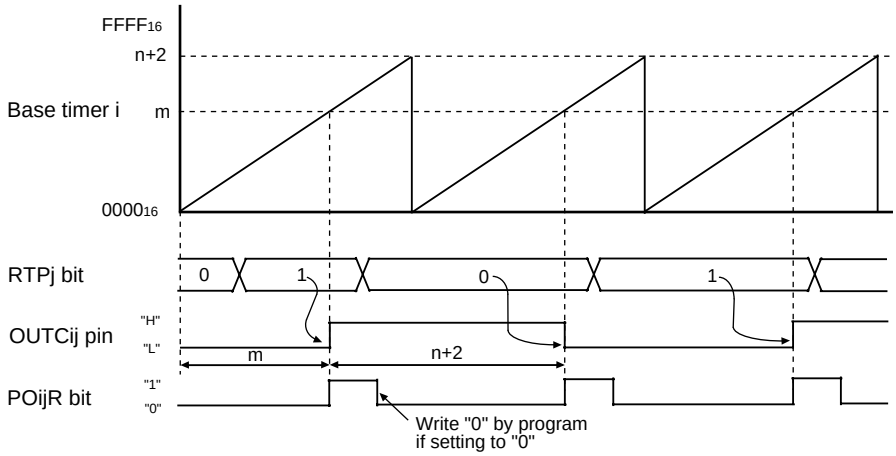


i=2 to 3, j=0 to 7
m : Setting value of the GiPOj register (0000$_{16}$ to FFFF$_{16}$)
POijR bit : Bits in the IIO3IR to IIO11IR registers

The above applies to the following conditions.

- The IVL bit in the GiPOCRj register is set to "0" (output "L" as an initial value). The INV bit is set to "0" (no output inversed).
- RST2 to RST0 bits in the GiBCR1 register are set to "000$_2$" (no base timer reset).

(2) The base timer is reset when the base timer matches the GiPO0 register
(The RST1 bit is set to "1" and both RST0 and RST2 bits are set to "0")



i=2 to 3, j=1 to 7
m : Setting value of the GiPOj register (0000$_{16}$ to FFFF$_{16}$)
n: Setting value of the GiPO0 register (0001$_{16}$ to FFFD$_{16}$)
POijR bit : Bits in the IIO0IR to IIO11IR registers

The above applies to the following condition.

- The IVL bit in the GiPOCRj register is set to "0" (output "L" as an initial value). The INV bit is set to "0" (no output inversed).
- m < n+2

Figure 21.29 Real-time Port Output Mode

21.3.6 Parallel Real-Time Port Output Mode (Group 2 and 3)

The OUTCij pin outputs the value set by the GiRTP register in one-byte units when the value of the base timer matches that of the GiPOj register (i=2 to 3, j=0 to 7). Table 21.15 lists specifications of the parallel RTP output mode. Figure 21.30 shows a block diagram of the parallel RTP output function. Figure 21.31 shows an example of the parallel RTP output mode operation. (See Figure 21.7 for the G2BCR1 register and Figure 21.8 for the G3BCR1 register.)

Table 21.15 Parallel RTP Output Mode Specifications

Item	Specification
Waveform Output Start Condition	The IFEj bit in the GiFE register (i=2 to 3, j=0 to 7) is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The POijR bit in the interrupt request register is set to "1" when value of the base timer matches that of the GiPOj register (0000_{16} to $FFFF_{16}$(1)). (See Figure 10.14.)
OUTCij Pin	RTP output
Selectable Function	• Default value set function: Set starting waveform output level • Inverse output function: Waveform output level is inversed and output from the OUTCij pin

NOTES:

1. Set the GiPO0 register to 0001_{16} to $FFFD_{16}$ when setting the base timer to "0000_{16}" (the RST1 bit in the GiBCR1 register is set to "1", and the RST0 and RST2 bits are set to "0") while the values in the base timer and the GiPO0 register match

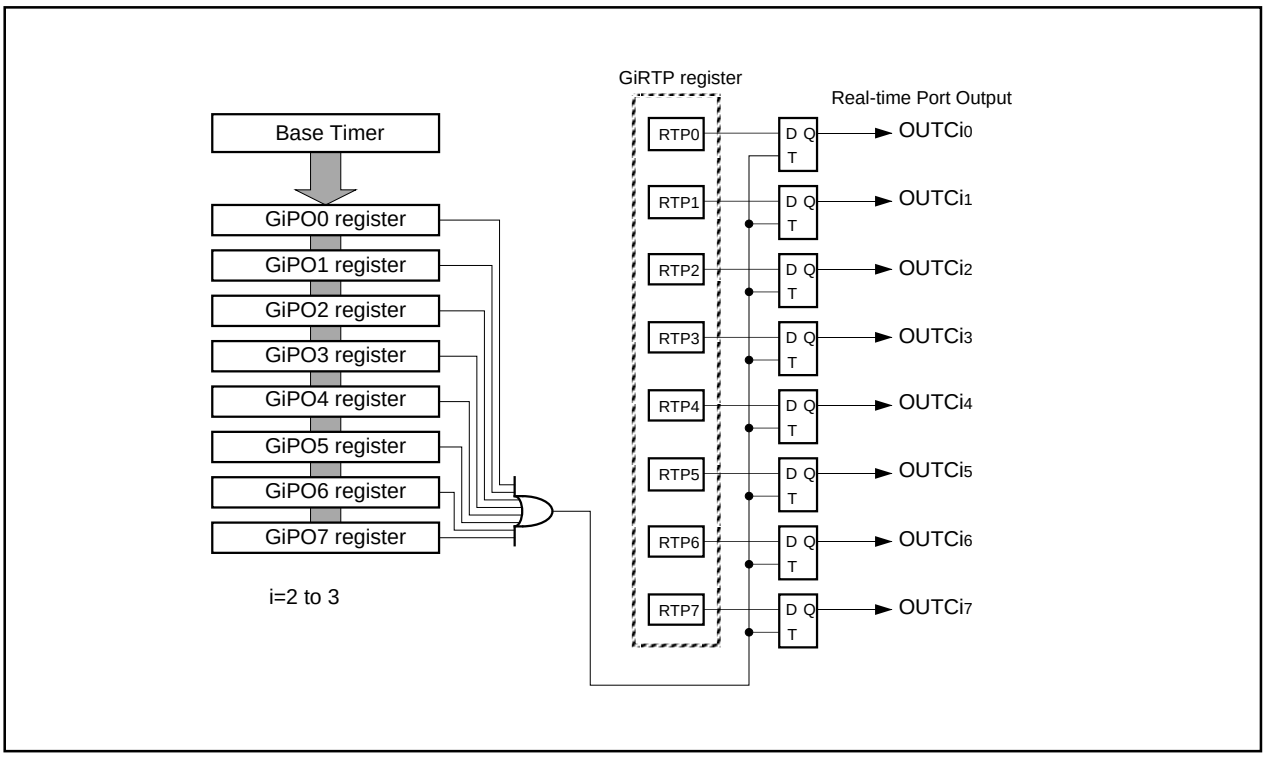
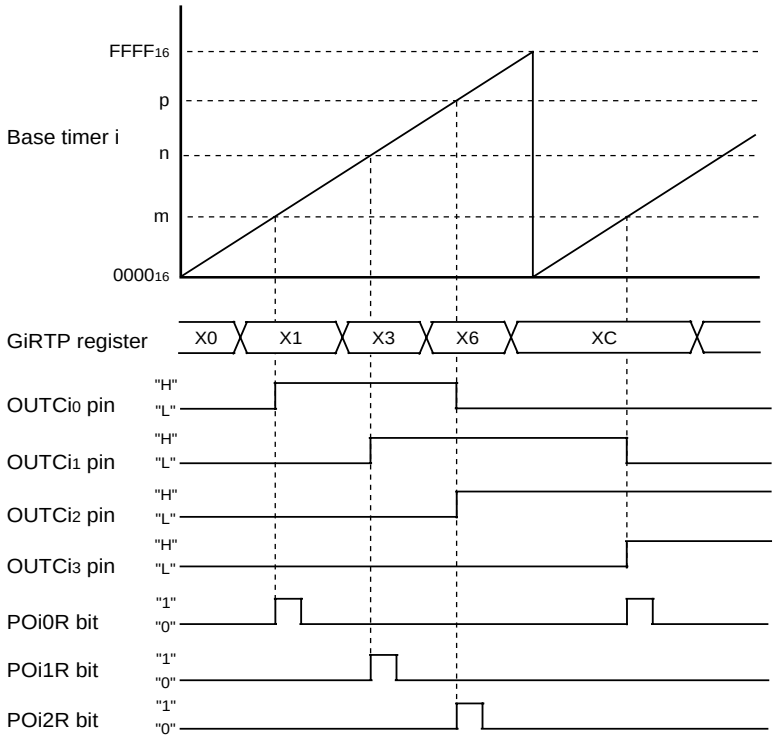


Figure 21.30 Parallel RTP Output Function Block Diagram

(1) Free-Running Operation



i=2,3

m : Setting value of the GiPO0 register (0000_{16} to $FFFF_{16}$)
n : Setting value of the GiPO1 register (0000_{16} to $FFFF_{16}$)
p : Setting value of the GiPO2 register (0000_{16} to $FFFF_{16}$)

- POi0R, POi1R, POi2R bit : Bits in the IIO3IR to IIO11IR registers

The above applies under the following conditions.

- The IVL in the of GiPOCRj register is set to "0" (output "L" as an initial value).
- The INV bit is set to "0" (no output inversed).
  RST2 to RST0 bits in the GiBCR1 register are set to "000_2" (no base timer reset).
  m < n < p

Figure 21.31 Parallel RTP Output Mode

21.4 Communication Unit 0 and 1 Communication Function

The communication function is available when two 8-bit shift registers are used with either timer measurement function or waveform generation function.

In the intelligent I/O groups 0 and 1, 8-bit clock synchronous serial I/O, 8-bit clock asynchronous serial I/O (UART) and HDLC data processing are available.

Figures 21.32 to 21.38 show registers associated with the communication function.

Group i Receive Input Register (i=0,1)

b7 b0

Symbol	Address	After Reset
G0RI,G1RI	$00EC_{16}$, $012C_{16}$	Indeterminate

Function	Setting Range	RW
Set data to be transmitted to a received data generation circuit	00_{16} to FF_{16}	WO

Group i Transmit Output Register (i=0,1)

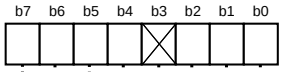
b7 b0

Symbol	Address	After Reset
G0TO, G1TO	$00EE_{16}$, $012E_{16}$	Indeterminate

Function	RW
Can read data transmitted by a transmitted data generation circuit	RO

Figure 21.32 G0RI to G1RI Registers and G0TO to G1TO Registers

Group i SI/O Communication Control Register (i=0,1)



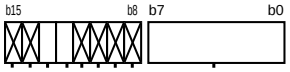
Symbol	Address	After Reset
G0CR, G1CR	$00EF_{16}$, $012F_{16}$	$0000\ X000_2$

Bit Symbol	Bit Name	Function	RW
TI	Transmit Buffer Empty Flag	0 : Data in the GiTB register 1 : No data in the GiTB register	RO
TXEPT	Transmit Register Empty Flag	0 : Data in the transmit register (during transmission) 1 : No data in the transmit register (transmit completed)	RO
RI	Receive Complete Flag	0 : No data in the GiRB register 1 : Data in the GiRB register	RO
____ (b3)	Nothing is assigned. When write, set to "0". When read, its contents is indeterminate.		–
TE	Transmit Enable Bit	0 : Transmit disable 1 : Transmit enable	RW
RE	Receive Enable Bit	0 : Receive disable 1 : Receive enable	RW
IPOL	ISRxD Input Polarity Switch Bit	0 : No inverse 1 : Inverse(1)	RW
OPOL	ISTxD Output Polarity Switch Bit	0 : No inverse 1 : Inverse(1)	RW

NOTES:
1. Set to "1" when using UART mode

Figure 21.33 G0CR to G1CR Registers

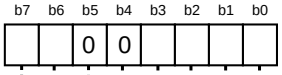
Group i SI/O Receive Buffer Register (i=0,1)



Symbol	Address	After Reset
G0RB, G1RB	$00E9_{16}$-$00E8_{16}$, 0129_{16}-0128_{16}	XX00 XXXX XXXX XXX_2

Bit Symbol	Bit Name	Function	RW
____ (b7 - b0)	————	Received data	RW
____ (b11 - b8)	Nothing is assigned. When read, its content is indeterminate.		—
OER	Overrun Error Flag	0 : No overrun error 1 : Overrun error found	RO
FER	Framing Error Flag	0 : No framing error 1 : Framing error found	RO
____ (b15 - b14)	Nothing is assigned. When read, its content is indeterminate.		—

Group i SI/O Communication Mode Register (i=0,1)



Symbol	Address	After Reset
G0MR,G1MR	$00ED_{16}$, $012D_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
GMD0	Communication Mode Select Bit	b1 b0 0 0 : UART mode 0 1 : Clock synchronous serial I/O mode 1 0 : Special communication mode(1) 1 1 : HDLC data processing mode	RW
GMD1			RW
CKDIR	Internal/External Clock Select Bit	0 : Internal clock 1 : External clock	RW
STPS	Stop Bit Length Select Bit	0 : 1 stop bit 1 : 2 stop bits	RW
____ (b5 - b4)	Reserved Bit	Set to "0"	RW
UFORM	Transfer Direction Select Bit	0 : LSB first 1 : MSB first	RW
IRS	Transmit Interrupt Cause Select Bit	0 : No data in the transmit buffer (TI=1) 1 : Transmission is completed (TXEPT=1)	RW

NOTES:
1. Do not set except when using in motor vehicles

Figure 21.34 G0RB to G1RB Registers and G0MR to G1MR Registers

Group i SI/O Expansion Mode Register (i=0,1)(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
G0EMR,G1EMR	00FC16, 013C16	0016

Bit Symbol	Bit Name	Function	RW
SMODE	Synchronous Mode Select Bit	0 : No re-synchronous mode used 1 : Re-synchronous mode	RW
CRCV	CRC Default Value Select Bit	0 : Set to "000016" 1 : Set to "FFFF16"	RW
ACRC	CRC Reset Select Bit	0 : Not reset 1 : Reset(2)	RW
BSINT	Bit Stuffing Error Interrupt Select Bit	0 : Not used 1 : Used	RW
RXSL	Receive Source Switch Bit	0 : ISRxDi pin 1 : GiRI register	RW
TXSL	Transmit Source Switch Bit	0 : ISTxDi pin 1 : GiTO register	RW
CRC0	CRC Generation Polynomial Select Bit	b7 b6 0 0 : X^8+X^4+X+1 0 1 : Do not set to this value 1 0 : $X^{16}+X^{15}+X^2+1$ 1 1 : $X^{16}+X^{12}+X^5+1$	RW
CRC1			RW

NOTES:
1. The GiEMR register is used in special communication mode or HDLC data processing mode. Do not use in clock synchronous serial I/O mode or UART mode.
2. The CRC is reset when a data in the GiCMP3 register matches a received data.

Group i SI/O Expansion Transmit Control Register (i=0,1)(1)

b7 b6 b5 b4 b3 b2 b1 b0

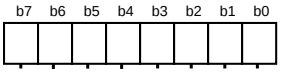
Symbol	Address	After Reset
G0ETC,G1ETC	00FF16, 013F16	0000 0XXX2

Bit Symbol	Bit Name	Function	RW
——— (b2 - b0)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
SOF	SOF Transmit Request Bit	0 : No request to transmit SOF 1 : Request to transmit SOF	RW
TCRCE	Transmit CRC Enable Bit	0 : Not used 1 : Used	RW
ABTE	Arbitration Enable Bit	0 : Not used 1 : Used	RW
TBSF0	Transmit Bit Stuffing "1" Insert Select Bit	0 : "1" is not inserted 1 : "1" is inserted	RW
TBSF1	Transmit Bit Stuffing "0" Insert Select Bit	0 : "0" is not inserted 1 : "0" is inserted	RW

NOTES:
1. The GiETC register is used in special communication mode or HDLC data processing mode. Do not use in clock synchronous serial I/O mode or UART mode.

Figure 21.35 G0EMR to G1EMR Registers and G0ETC to G1ETC Registers

Group i SI/O Expansion Receive Control Register (i=0,1)(1)



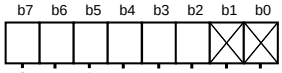
Symbol	Address	After Reset
G0ERC,G1ERC	$00FD_{16}$, $013D_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
CMP0E	Data Compare Function 0 Select Bit	0 : The GiDR register (transmit data register) is not compared with the GiCMP0 register 1 : The GiDR register is comparedwith the GiCMP0 register	RW
CMP1E	Data Compare Function 1 Select Bit	0 : The GiDR register (transmit data register) is not compared with the GiCMP1 register 1 : The GiDR register is compared with the GiCMP1 register	RW
CMP2E	Data Compare Function 2 Select Bit	0 : The GiDR register (transmit data register) is not compared with the GiCMP2 register 1 : The GiDR register is compared with the GiCMP2 register	RW
CMP3E	Data Compare Function 3 Select Bit	0 : The GiDR register (transmit data register) is not compared with the GiCMP3 register 1 : The GiDR register is compared with the GiCMP3 register(2)	RW
RCRCE	Receive CRC Enable Bit	0 : Not used 1 : Used	RW
RSHTE	Receive Shift Operation Enable Bit	0 : Disables receive shift operation 1 : Enables receive shift operation	RW
RBSF0	Receive Bit Stuffing "1" Delete Select Bit	0 : "1" is not deleted 1 : "1" is deleted	RW
RBSF1	Receive Bit Stuffing "0" Delete Select Bit	0 : "0" is not deleted 1 : "0" is deleted	RW

NOTES:
1. The GiERC register is used in special communication mode or HDLC data processing mode. Set to "$0010\ 0000_2$" in clock synchronous serial I/O mode. Do not use in UART mode.
2. When the ACRC bit in the GiEMR register is set to "1" (CRC reset function used), set the CMP3E bit to "1".

Figure 21.36 G0ERC to G1ERC Registers

Group i SI/O Special Communication Interrupt Detect Register (i=0,1)(1,2)

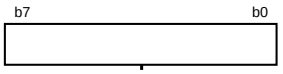


Symbol	Address	After Reset
G0IRF,G1IRF	00FE16, 013E16	0000 00XX2

Bit Symbol	Bit Name	Function	RW
——— (b1 - b0)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
BSERR	Bit Stuffing Error Detect Flag	0 : Not detected 1 : Detected	RW
ABT	Arbitration Lost Detect Flag	0 : Not detected 1 : Detected	RW
IRF0	Interrupt Cause Determination Flag 0(2)	0 : The GiDR register (receive data register) does not match the GiCMP0 register 1 : The GiDR register matches the GiCMP0 register	RW
IRF1	Interrupt Cause Determination Flag 1(2)	0 : The GiDR register (receive data register) does not match the GiCMP1 register 1 : The GiDR register matches the GiCMP1 register	RW
IRF2	Interrupt Cause Determination Flag 2(2)	0 : The GiDR register (receive data register) does not match the GiCMP2 register 1 : The GiDR register matches the GiCMP2 register	RW
IRF3	Interrupt Cause Determination Flag 3(2)	0 : The GiDR register (receive data register) does not match the GiCMP3 register 1 : The GiDR register matches the GiCMP3 register	RW

NOTES:
1. The GiETC register is used in special communication mode or HDLC data processing mode. Do not use in clock synchronous serial I/O mode or UART mode.
2. The SRTiR bit in the IIO4IR register is set to "1" if the BSERR bit, ABT bit or the IRF0 to IRF3 bits is set to "0".

Group i Transmit Buffer (Receive Data) Register (i=0,1)(1)



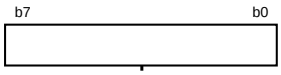
Symbol	Address	After Reset
G0TB,G0DR	00EA16	Indeterminate
G1TB,G1DR	012A16	Indeterminate

Function	RW
Set data to be transmitted. Values written in these registers are written to the GiTB register. Data read from these registers in HDLC data processing mode are values written in the GiDR register	WO (RO)

NOTES:
1. The GiTB register and the GiDR register share addresses.

Figure 21.37 G0IRF to G1IRF Registers and G0TB to G1TB Registers

Group i Data Compare Register j (i=0,1; j=0 to 3)

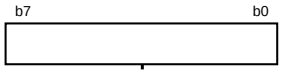


Symbol	Address	After Reset
G0CMP0 to G0CMP3	$00F0_{16}$, $00F1_{16}$, $00F2_{16}$, $00F3_{16}$	Indeterminate
G1CMP0 to G1CMP3	0130_{16}, 0131_{16}, 0132_{16}, 0133_{16}	Indeterminate

Function	Setting Range	RW
Data to be compared	00_{16} to FF_{16}	RW

NOTES:
1. Set the GiMSK0 register to use the GiCMP0 register.
   Set the GiMSK1 register to use the GiCMP1 register.

Group i Data Mask Register j (i=0,1; j=0,1)



Symbol	Address	After Reset
G0MSK0,G0MSK1	$00F4_{16}$, $00F5_{16}$	Indeterminate
G1MSK0,G1MSK1	0134_{16}, 0135_{16}	Indeterminate

Function	Setting Range	RW
Masked data for received data Set bits not being compared to "1"	00_{16} to FF_{16}	RW

Group i Transmit CRC Code Register (i=0,1)

Symbol	Address	After Reset
G0TCRC, G1TCRC	$00FB_{16}$-$00FA_{16}$, $013B_{16}$-$013A_{16}$	0000_{16}

Function	RW
Result of the transmit CRC calculation(1,2)	RO

NOTES:
1. Calculation results are reset by setting the TE bit in the GiCR register to "0" (transmit disabled). Default value is determined by setting the CRCV bit in the GiEMR register.
2. Transmit CRC calculation is performed with every bit of transmit data transmitted while theTCRCE bit in the GiETC register is set to "1" (used).

Group i Receive CRC Code Register (i=0,1)

Symbol	Address	After Reset
G0RCRC, G1RCRC	$00F9_{16}$-$00F8_{16}$, 0139_{16}-0138_{16}	Indeterminate

Function	RW
Result of the receive CRC calculation(1, 2, 3)	RO

NOTES:
1. The calculation result is reset by setting the RCRCE bit in the GiERC register to "0" (not used). If the the ACRC bit in the GiCMPj register is set to "1" (reset), the result is reset by matching the data in the GiCMPj register with the received data.
2. The result is reset to the default value selected by the CRCV bit in the GiEMR register before transmission starts.
3. Transmit CRC calculation is performed with every bit of transmit data transmitted while the RCRCE bit in the GiERC register is set to "1" (used).

Figure 21.38 G0CMP0 to G0CMP3 Registers, G1CMP0 to G1CMP3 Registers, G0MSK0 to G0MSK1 Registers, G1MSK0 to G1MSK1 Registers, G0TCRC to G1TCRC Registers, and G0RCRC to G1RCRC Registers

21.4.1 Clock Synchronous Serial I/O Mode (Groups 0 and 1)

In clock synchronous serial I/O mode, data is transmitted and received with the transfer clock. When the internal clock is selected as the transfer clock, the channel 0 and channel 3 waveform generation functions generate the internal clock. ISTxDi (i=0, 1), ISCLKi, and ISRxDi share pins with INPCi0 to INPCi2 and OUTCi0 to OUTCi2.

Table 21.16 lists specifications of clock synchronous serial I/O mode. Table 21.17 lists registers to be used and their settings. Tables 21.18 to 21.21 list pin settings. Figure 21.39 shows an example of a transmit and receive operation.

Table 21.16 Clock Synchronous Serial I/O Mode Specifications (Groups 0 and 1)

Item	Specification
Transfer Data Format	Transfer data : 8 bits long
Transfer Clock(1, 2)	When the CKDIR bit in the GiMR register (i=0, 1) is set to "0" (internal clock) : $\frac{f_{BTi}}{2(n+2)}$ n : setting value of the GiPO0 register, 0000_{16} to $FFFF_{16}$ • The GiPO0 register determines the bit rate and the transfer clock is generated in phase-delayed waveform output mode by the channel 3 waveform generation function. When the CKDIR bit is set to "1" (external clock) : input from the ISCLKi pin
Transmit Start Condition	Set registers associated with the waveform generation function, the GiMR register and GiERC register. Then set as is written below after waiting at least one transfer clock cycle. • Set the TE bit in the GiCR register to "1" (transmit enable) • Set the TI bit in the GiCR register to "0" (data in the GiTB register)
Receive Start Condition	Set registers associated with the waveform generation function, the GiMR register and GiERC register. Then set as is written below after waiting at least one transfer clock cycle. • Set the RE bit in the GiCR register to "1" (receive enable) • Set the TE bit to "1" (transmit enable) • Set the TI bit to "0" (data in the GiTB register)
Interrupt Request	• While transmitting, one of the following conditions can be selected to set the SIOiTR bit to "1" (see Figure 10.14): – The IRS bit in the GiMR register is set to "0" (no data in the GiTB register) and data is transferred to the transmit register from the GiTB register – The IRS bit is set to "1" (reception completed) and data transfer from the transmit register is completed • While receiving, the following condition can be selected to set the SIOiRR bit to "1" (see Figure 10.14): Data is transferred from the receive register to the GiRB register
Error Detection	Overrun error(3) This error occurs when the 8th bit of the next data is received before reading the GiRB register
Selectable Function	• LSB first/MSB first Select either bit 0 or bit 7 to transmit/receive data • ISTxDi and ISRxDi I/O polarity inverse ISTxDi pin output level and ISRxDi pin input level are inversed

NOTES:
1. The transfer clock must be f_{BTi} divided by six or more.
2. In clock synchronous serial I/O mode, set the RSHTE bit in the GiERC register (i=0, 1) to "1" (receive shift operation enabled).
3. When an overrun error occurs, the GiRB register is indeterminate.

When the OPOL bit in the GiCR register is set to "0" (no ISTxDi output polarity inversed), the ISTxDi pin outputs an "H" signal after selecting operation mode until transfer starts. When the OPOL bit is set to "1", the ISTxDi pin outputs an "L" signal.

Table 21.17 Registers to be Used and Settings

Register	Bit	Function
GiBCR0	BCK1 to BCK0	Set to "11$_2$"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
GiBCR1	7 to 0	Set to "0001 0010$_2$"
GiPOCR0	7 to 0	Set to "0000 0111$_2$"
GiPOCR1	7 to 0	Set to "0000 0111$_2$"
GiPOCR3	7 to 0	Set to "0000 0010$_2$" (1)
GiPO0	15 to 0	Set the bit rate $\frac{f_{BTi}}{2x(\text{setting value} + 2)}$ = transfer clock frequency(1)
GiPO3	15 to 0	Set to a value smaller than the GiPO0 register(1)
GiFS	FSC3,1,0	Set to "0"
GiFE	IFE3,1,0	Set to "1"
GiERC	7 to 0	Set to "0010 0000$_2$"
GiMR	GMD1 to GMD0	Set to "01$_2$"
	CKDIR	Select the internal clock or external clock
	STPS	Set to "0"
	UFORM	Select either LSB first or MSB first
	IRS	Select how the transmit interrupt is generated
GiCR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission and reception
	RE	Set to "1" to enable reception
	IPOL	Select ISRxD input polarity (usually set to "0")
	OPOL	Select ISTxD output polarity (usually set to "0")
GiTB	7 to 0	Write data to be transmitted
GiRB	15 to 0	Received data and error flag are stored

i = 0 to 1

NOTES:

1. The CKDIR bit in the GiMR register is set to "0" (internal clock)

Table 21.18 Pin Settings (1)

Port Name	Function	Bit and Setting					Register(1)
		PS1 Register	PSL1 Register	PSC Register	PD7 Register	IPS Register	
P7$_3$	ISTxD1 output	PS1_3 = 1	PSL1_3 = 0	PSC_3 = 1	-	-	G1POCR0
P7$_4$	ISCLK1 input	PS1_4 = 0	-	-	PD7_4 = 0	IPS1 = 0	-
	ISCLK1 output	PS1_4 = 1	PSL1_4 = 0	PSC_4 = 1	-	-	G1POCR1
P7$_5$	ISRxD1 input	PS1_5 = 0	-	-	PD7_5 = 0	IPS1 = 0	-
P7$_6$	ISTxD0 output	PS1_6 = 1	PSL1_6 = 0	PSC_6 = 0	-	-	G0POCR0
P7$_7$	ISCLK0 input	PS1_7 = 0	-	-	PD7_7 = 0	IPS0 = 0	-
	ISCLK0 output	PS1_7 = 1	-	-	-	-	G0POCR1

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).

Table 21.19 Pin Settings (2)

Port Name	Function	Bit and Setting			Register
		PS2 Register	PD8 Register	IPS register	
P8$_0$	ISRxD0 input	PS2_0 = 0	PD8_2 = 0	IPS0 = 0	-

Table 21. 20 Pin Settings (3)

Port Name	Function	Bit and Setting			Register(1)
		PS5 Register	PD11 Register	IPS Register	
P11$_0$	ISTxD1 output	PS5_0 = 1	-	-	G1POCR0
P11$_1$	ISCLK1 input	PS5_1 = 0	PD11_1 = 0	IPS1 = 1	-
	ISCLK1 output	PS5_1 = 1	-	-	G1POCR1
P11$_2$	ISRxD1 input	PS5_2 = 0	PD11_2 = 0	IPS1 = 1	-

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).

Table 21. 21 Pin Settings (4)

Port Name	Function	Bit and Setting			Register(1)
		PS9 Register	PD15 Register	IPS Register	
P15$_0$	ISTxD0 output	PS9_0 = 1	-	-	G0POCR0
P15$_1$	ISCLK0 input	PS9_1 = 0	PD15_2 = 0	IPS0 = 1	-
	ISCLK0 output	PS9_1 = 1	-	-	G0POCR1
P15$_2$	ISRxD0 input	PS9_2 = 0	PD15_2 = 0	IPS0 = 1	-

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).

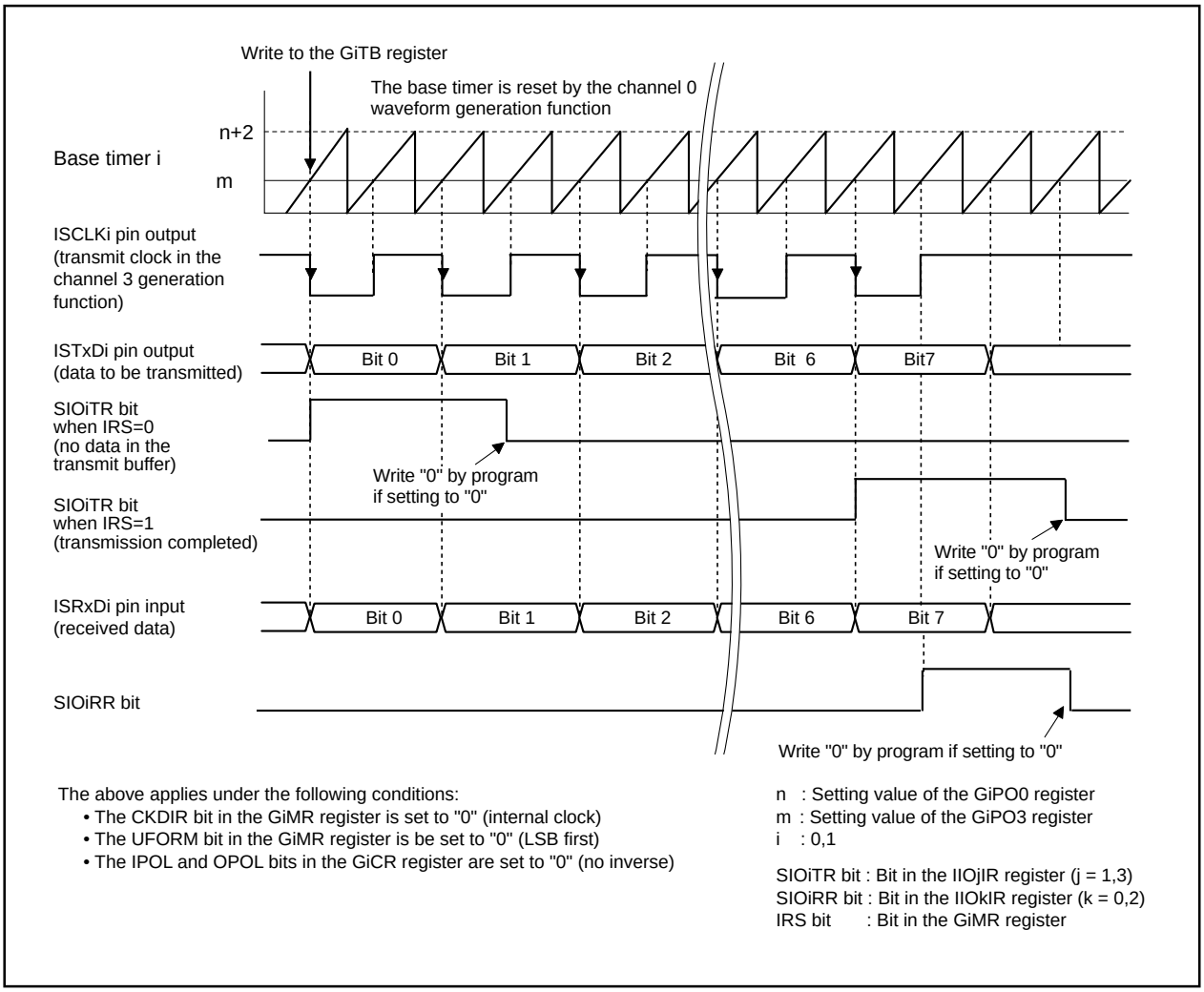


Figure 21.39 Transmit and Receive Operation

21.4.2 Clock Asynchronous Serial I/O Mode (UART) (Groups 0 and 1)

In clock asynchronous serial I/O mode (UART), data is transmitted at a desired bit rate and in a desired transfer data format. Table 21.22 lists specifications of UART mode groups 0 and 1. Table 21.23 lists registers to be used and their settings. Tables 21.24 to 21.27 list pin settings. Figure 21.40 shows an example of transmit operation. Figure 21.41 shows an example of receive operation.

Table 21.22 UART Mode Specifications

Item	Specification
Transfer Data Format	• Character Bit (transfer data) : 8 bits long • Start bit : 1 bit long • Stop bit : select length from 1 bit or 2 bits
Transfer Clock(1, 2)	When the CKDIR bit in the GiMR register (i=0, 1) is set to "0" (internal clock) : $\frac{f_{BTi}}{2(n+2)}$ n : setting value of the GiPO0 register, 0000_{16} to $FFFF_{16}$. • The GiPO0 register determines the bit rate. Transmit clock is generated in phase-delayed waveform output mode of the channel 3 waveform generation function. Receive clock is generated with the channel 2 time measurement function.
Transmit Start Condition	Set the registers associated with the waveform generation function, the GiMR register and GiERC register. Then, set as is written below after waiting at least one transfer clock cycle. • Set the TE bit in the GiCR register to "1" (transmit enable) • Set the TI bit in the GiCR register to "0" (data in the GiTB register)
Receive Start Condition	Set the registers associated with the waveform generation function, the GiMR register and GiERC register. Then, set as is written below after waiting at least one transfer clock cycle. • Set the RE bit in the GiCR register to "1" (receive enable) • Detect the start bit
Interrupt Request	• While transmitting, one of the following conditions can be selected to set the SIOiTR bit to "1" (see Figure 10.14): – The IRS bit in the GiMR register is set to "0" (no data in the GiTB register) and data is transferred to the transmit register from the GiTB register. – The IRS bit is set to "1" (reception completed) and data transfer from the transmit register is completed • While receiving, the following condition can be selected to set the SIOiRR bit to "1" (see Figure 10.14) : Data is transferred from the receive register to the GiRB register (data reception is completed)
Error detection	• Overrun error(3) This error occurs when the final stop bit of the next data is received before reading the GiRB register • Framing Error This error occurs when the number of the stop bits set is not detected
Selectable function	• Stop bit length The length of the stop bit is selected from 1 bit or 2 bits • LSB first/MSB first Select either bit 0 or bit 7 to transmit/receive data

NOTES:
1. The transfer clock must be f_{BTi} divided by six or more.
2. Set the GiPOCR2 register and the GiTMCR2 register.
3. When an overrun error occurs, the GiRB register is indeterminate.

Table 21.23 Registers to be Used and Settings

Register	Bit	Function
GiBCR0	BCK1 to BCK0	Set to "11$_2$"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
GiBCR1	7 to 0	Set to "0001 0010$_2$"
GiPOCR0	7 to 0	Set to "0000 0111$_2$"
GiPOCR2	7 to 0	Set to "0000 0110$_2$"
GiPOCR3	7 to 0	Set to "0000 0010$_2$"
GiTMCR2	7 to 0	Set to "0000 0010$_2$"
GiPO0	15 to 0	Set bit rate $\frac{f_{BTi}}{2 \times (\text{setting value} + 2)}$ = transfer clock frequency
GiPO3	15 to 0	Set to a value smaller than the GiPO0 register
GiFS	FSC3 to FSC0	Set to "0100$_2$"
GiFE	IFE3 to IFE0	Set to "1101$_2$"
GiMR	GMD1 to GMD0	Set to "00$_2$"
	CKDIR	Set to "0"
	STPS	Select stop bit length
	UFORM	Select LBS first or MSB first
	IRS	Select how the receive interrupt is generated
GiCR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission
	RE	Set to "1" to enable reception
	IPOL	Set to "1"
	OPOL	Set to "1"
GiTB	7 to 0	Write data to be transmitted
GiRB	15 to 0	Received data and error flag are stored

i = 0 to 1

Table 21.24 Pin Settings in UART Mode (1)

Port Name	Function	Bit and Setting					Register(1)
		PS1 Register	PSL1 Register	PSC Register	PD7 Register	IPS Register	
P73	ISTxD1 output	PS1_3 = 1	PSL1_3 = 0	PSC_3 = 1	-	-	G1POCR0
P75	ISRxD1 input	PS1_5 = 0	-	-	PD7_5 = 0	IPS1 = 0	-
P76	ISTxD0 output	PS1_6 = 1	PSL1_6 = 0	PSC_6 = 0	-	-	G0POCR0

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).

Table 21.25 Pin Settings (2)

Port Name	Function	Bit and Setting				Register
		PS2 Register	PSL2 Register	PD8 Register	IPS Register	
P80	ISRxD0 input	PS2_0 = 0	-	PD8_0 = 0	IPS0 = 0	-

Table 21.26 Pin Settings (3)

Port Name	Function	Bit and Setting			Register(1)
		PS5 Register	PD11 Register	IPS Register	
P110	ISTxD1 output	PS5_0 = 1	-	-	G1POCR0
P112	ISRxD1 input	PS5_2 = 0	PD11_2 = 0	IPS1 = 1	-

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).

Table 21.27 Pin Settings (4)

Port Name	Function	Bit and Setting			Register(1)
		PS9 Register	PD15 Register	IPS Register	
P150	ISTxD0 output	PS9_0 = 1	-	-	G0POCR0
P152	ISRxD0 input	-	PD15_2 = 0	IPS0 = 1	-

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).

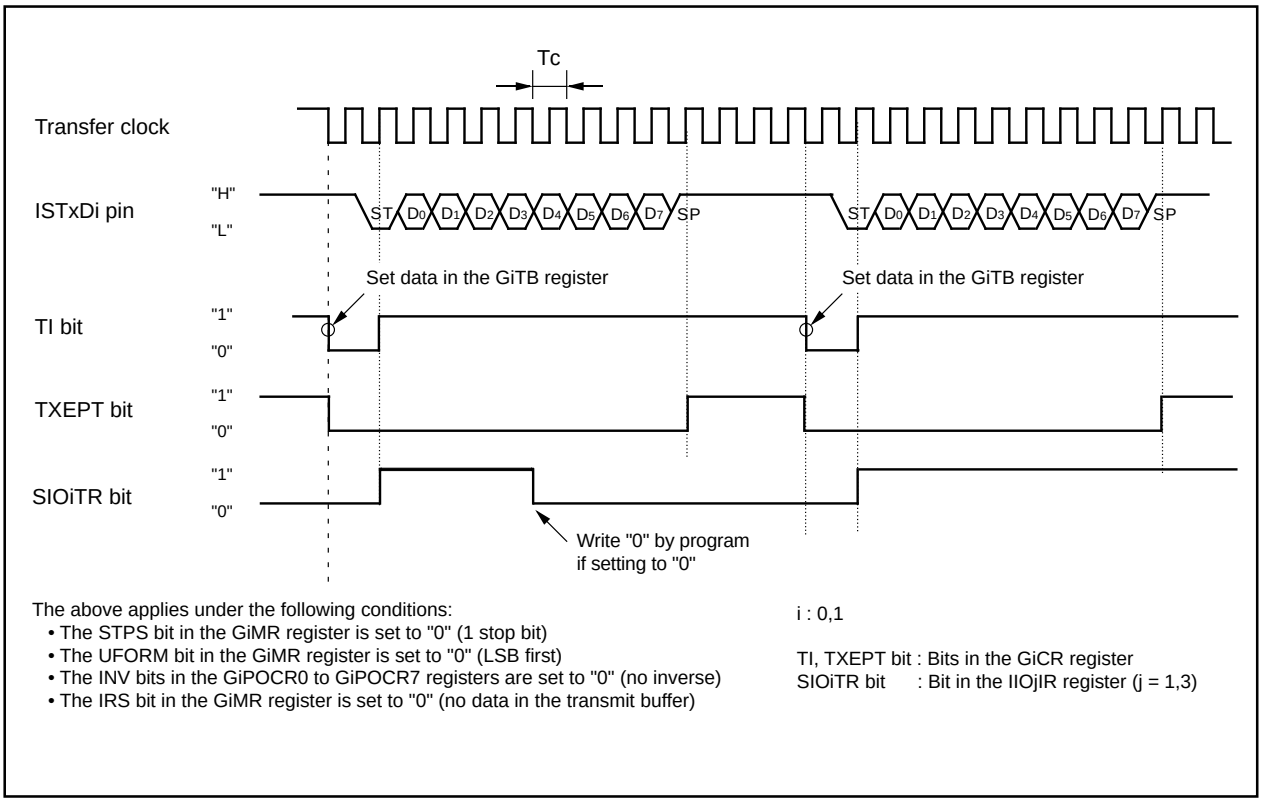


Figure 21.40 Transmit Operation

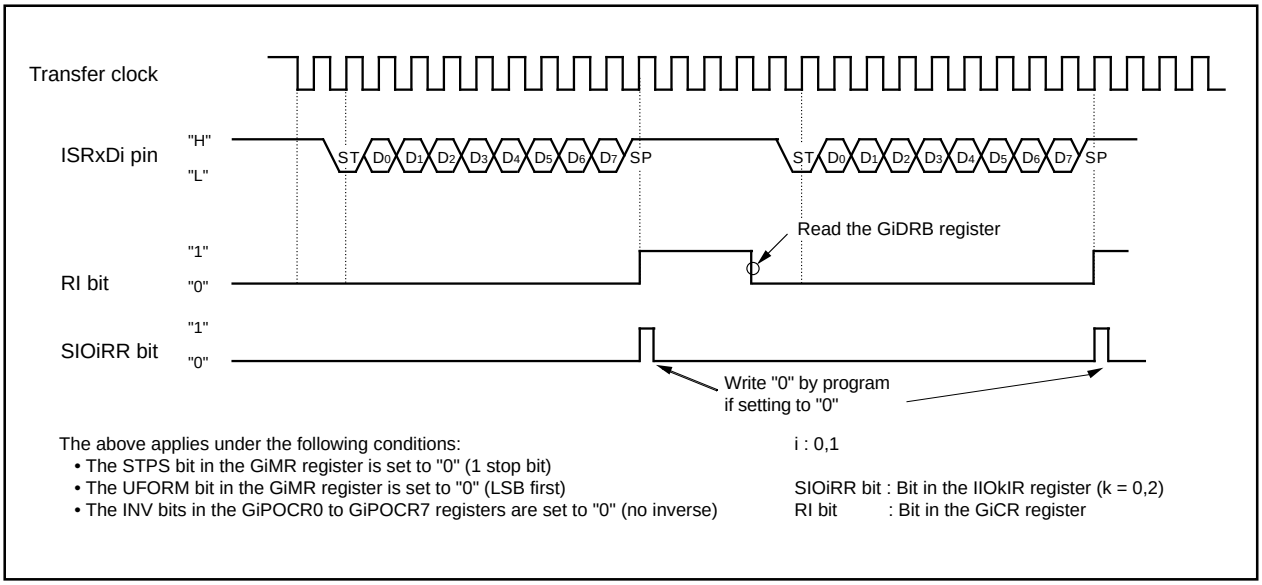


Figure 21.41 Receive Operation

21.4.3 HDLC Data Processing Mode (Group 0 and 1)

In HDLC data processing mode, bit stuffing, flag detection, abort detection and CRC calculation are available for HDLC control. The channel 0 and 1 are used to generate the transfer clock. No pins are used.

To convert data, data to be transmitted is written to the GiTB register (i=0,1) and the data conversion result is restored after data conversion. If any data are in the GiTO register after data conversion, the conversion is terminated. If no data is in the GiTO register, bit stuffing processing is executed regardless of there being no data in the transmit output buffer. A CRC value is calculated every time one bit is converted. If no data is in the GiRI register, received data conversion is terminated.

Table 21.28 list specifications of the HDLC data processing mode. Table 21.29 lists registers to be used and their settings.

Table 21.28 HDLC Processing Mode Specifications

Item	Specification
Input Data Format	8-bit data fixed, bit alignment is optional
Output Data Format	8-bit data fixed
Transfer Clock	When the CKDIR bit in the GiMR register (i=0, 1) is set to "0" (internal clock) : $\frac{f_{BTi}}{n+2}$ n : setting value of the GiPO0 register 0000_{16} to $FFFF_{16}$ • The GiPO0 register determines bit rate. The transfer clock is generated in phase-delayed waveform output mode of the channel 1 waveform generation function. When the RSHTE bit in the GiERC register is set to "1" (reception shift operation enabled), the transfer clock is generated in the receiver
I/O Method	• While transmitting, value set in the GiTB register is converted in HDLC data processing mode and transferred to the GiTO register • While receiving, value set in the GiRI register is converted in HDLC data processing mode and transferred to the GiRB register. The value in the GiRI register is also transferred to the GiDR register (received data register).
Bit Stuffing	While transmitting, "0" following five consecutive "1" is inserted. While receiving, "0" following five consecutive "1" is deleted.
Flag Detection	Write the flag data "$7E_{16}$" to the GiCMP3 register to use the special communication interrupt (the SRTiR bit in the IIO4IR register)
Abort Detection	Write the masked data "01_{16}" to the GiMSKk(k=0, 1) register
CRC	The CRC1 to CRC0 bits are set to "11_2" ($X^{16}+X^{12}+X^5+1$) The CRCV bit is set to "1" (set to "$FFFF_{16}$") • While transmitting, CRC calculation result is stored into the GiTCRC register. The TCRCE bit in the GiETC register is set to "1" (transmit CRC used). The CRC calculation result is reset when the TE bit in the GiCR register is set to "0" (transmit disabled)(1). • While receiving, CRC calculation result is stored into the GiRCRC register. The RCRCE bit in the GiERC register is set to "1" (receive CRC used). The CRC calculation result is reset by comparing the flag data "$7E_{16}$" and matching the result with the value in the GiCMP3 register. The ACRC bit in the GiEMR register is set to "1" (CRC reset)(2)

Table 21.28 HDLC Processing Mode Specifications (Continued)

Item	Specification
Data Processing Start Conditions	The following conditions are required to start transmit data processing: • The TE bit in the GiCR register is set to "1" (transmit enable) • Data is written to the GiTB register The following conditions are required to start receive data processing: • The RE bit in the GiCR register is set to "1" (receive enable) • Data is written to the GiRI register
Interrupt Request(3)	During transmit data processing, (1) One of the following conditions can be selected to set the GiTOR bit in the interrupt request register to "1" (interrupt request) (see Figure 10.14) – When the IRS bit in the GiMR register is set to "0" (no data in the GiTB register) and data is transferred from the GiTB register to the transmit register (transmit start) – When the IRS bit is set to "1" (reception completed) and data transfer from the transmit register to the GiTO register is completed (2) When data, which is already converted to HDLC data, is transferred from the receive register of the GiTO register to the transmit buffer, the GiTOR bit is set to "1" During received data processing, (1) When data is transferred from the GiRI register to the GiRB register (reception completed), the GiRIR bit is set to "1" (See Figure 10.14) (2) When received data is transferred from the receive buffer of the GiRI register to the receive register, the GiRIR bit is set to "1" (3) When the GiTB register is compared to the GiCMPj register (j=0 to 3), the SRTiR bit is set to "1"

NOTES:
1. Set the CRCV bit and ACRC bit in the GiEMR register to "1".
2. The CRC calculation circuit is reset after the GiRCRC register stores CRC data.
3. See Figure 10.14 for details on the GiTOR bit, GiRIR bit and SRTiR bit.

Table 21.29 Registers to be Used and Settings

Register	Bit	Function
GiBCR0	BCK1 to BCK0	Select count source
	DIV4 to DIV0	Select divide ratio of count source
	IT	Select the base timer interrupt
GiBCR1	7 to 0	Set to "0001 0010$_2$"
GiPOCR0	7 to 0	Set to "0000 0000$_2$"
GiPOCR1	7 to 0	Set to "0000 0000$_2$"
GiPO0	15 to 0	Set bit rate
GiPO1	15 to 0	Set the timing of the rising edge of the transfer clock. Timing of the falling edge (high-level signal ("H") width of the transfer clock) is fixed. Setting value of GiPO1 ≤ Setting value of GiPO0 .
GiFS	FSC1 to FSC0	Set to "00$_2$"
GiFE	IFE1 to IFE0	Set to "11$_2$"
GiMR	GMD1 to GMD0	Set to "11$_2$"
	CKDIR	Set to "0"
	UFORM	Set to "0"
	IRS	Select how the transmit interrupt is generated
GiEMR	7 to 0	Set to "1111 0110$_2$"
GiCR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Transmit enable bit
	RE	Receive enable bit
GiETC	SOF	Set to "0"
	TCRCE	Select whether the transmit CRC is used or not
	ABTE	Set to "0"
	TBSF0, TBSF1	Transmit bit stuffing
GiERC	CMP2E to CMP0E	Select whether received data is compared or not
	CMP3E	Set to "1"
	RCRCE	Select whether receive CRC is used or not
	RSHTE	Set to "1" to use it in the receiver
	RBSF0, RBSF1	Receive bit stuffing
GiIRF	BSERR, ABT	Set to "0"
	IRF3 to IRF0	Select how an interrupt is generated
GiCMP0, GiCMP1	7 to 0	Write "FE$_{16}$" to abort processing
GiCMP2	7 to 0	Data to be compared
GiCMP3	7 to 0	Write "7E$_{16}$"
GiMSK0, GiMSK1	7 to 0	Write "01$_{16}$" to abort processing
GiTCRC	15 to 0	Transmit CRC calculation result can be read
GiRCRC	15 to 0	Receive CRC calculation result can be read
GiTO	7 to 0	Data, which is output from a transmit data generation circuit, can be read
GiRI	7 to 0	Set data input to a receive data generation circuit
GiRB	7 to 0	Received data is stored
GiTB	7 to 0	For transmission : write data to be transmitted For reception : received data for comparison is stored

i = 0,1

21.5 Group 2 Communication Function

The communication function is available when two 8-bit shift registers are used with the waveform generation function.

In the intelligent I/O group 2, the variable clock synchronous serial I/O or IEBus(1) communication function is available. Figures 21.42 to 21.45 show registers associated with the communication function.

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.

Group 2 SI/O Transmit Buffer Register

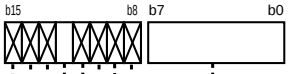
Symbol	Address	After Reset
G2TB	016D16-016C16	Indeterminate

Bit Symbol	Bit Name	Function	RW
——— (b7 - b0)	Transmit Buffer	Data to be transmitted	RO
SZ0	Transfer Bit Length Select Bit	b10 b9 b8 0 0 0 : 8 bits long 0 0 1 : 1 bits long 0 1 0 : 2 bits long 0 1 1 : 3 bits long 1 0 0 : 4 bits long 1 0 1 : 5 bits long 1 1 0 : 6 bits long 1 1 1 : 7 bits long	RW
SZ1			RW
SZ2			RW
——— (b12 - b11)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
A	ACK Function Select Bit	0 : Adds no ACK bit 1 : Adds the ACK bit after last transmit bit	RW
PC	Parity Calculation Continuing Bit(1)	0 : Adds the parity bit after a data to be transmitted 1 : Carries over a parity to a data to be transmitted	RW
P	Parity Function Select Bit	0 : No parity 1 : Parity (even parity only)	RW

NOTES:

1. Set the P bit to "0" before setting the PC bit to "1"

Group 2 SI/O Receive Buffer Register



Symbol	Address	After Reset
G2RB	016F16 - 016E16	Indeterminate

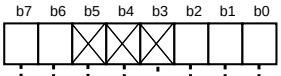
Bit Symbol	Bit Name	Function	RW
——— (b7 - b0)	Receive Buffer	Received data	RO
——— (b11 - b8)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
OER	Overrun Error Flag(1)	0 : No overrun error 1 : Overrun error found	RO
——— (b15 - b13)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:

1. The OER bit is set to "0" when the GMD1 to GMD0 bits in the G2MR register are set to "00$_2$" (communication unit reset) or the RE bit in the G2CR register is set to "0" (receive disable).

Figure 21.42 G2TB and G2RB Register

Group 2 SI/O Communication Mode Register

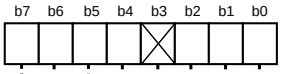


Symbol	Address	After Reset
G2MR	016A16	00XX X0002

Bit Symbol	Bit Name	Function	RW
GMD0	Communication Mode Select Bit	b1b0 0 0 : Communication unit is reset (The OER bit is set to "0")(1) 0 1 : Clock synchronous serial I/O mode(2) 1 0 : IE mode(2) 1 1 : Do not set to this value	RW
GMD1			RW
CKDIR	Internal/External Clock Select Bit	0 : Internal clock 1 : External clock	RW
____ (b5 - b3)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
UFORM	Transfer Direction Select Bit	0 : LSB first 1 : MSB first	RW
IRS	Transmit Interrupt Cause Select Bit	0 : No data is in the transmit buffer 1 : Transmission is completed	RW

NOTES:
1. Run the base timer clock for one or more cycles after the GMD1 to GMD0 bits are set to "002" (communication unit reset).
2. Set the GMD1 to GMD0 bits to "012" (clock synchronous serial I/O mode) or "102" (IE mode) while the base timer clock is stopped.

Group 2 SI/O Communication Control Register



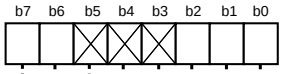
Symbol	Address	After Reset
G2CR	016B16	0000 X0002

Bit Symbol	Bit Name	Function	RW
TE	Transmit Enable Bit	0 : Transmit disabled 1 : Transmit enabled	RW
TXEPT	Transmit Register Empty Flag	0 : Data is in the transmit register (during transmission) 1 : No data is in the transmit register (transmission is completed)	RO
TI	Transmit Buffer Empty Flag	0 : Data is in the G2TB register 1 : No data is in the G2TB register	RO
____ (b3)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
RE	Receive Enable Bit1	0 : Receive disabled 1 : Receive enabled	RW
RI	Receive Complete Flag	0 : No data is in the G2RB register 1 : Data is in the G2RB register	RO
OPOL	ISTxD Output Polarity Switch Bit	0 : No inverse 1 : Inverse	RW
IPOL	ISRxD Input Polarity Switch Bit(1)	0 : No inverse 1 : Inverse	RW

NOTES:
1. The group 2 base timer may be reset when rewriting the RE or IPOL bit. To avoid resetting, set the RST2 bit in the G2BCR1 register to "0" (no base timer reset by a reset request from the communication function).

Figure 21.43 G2MR and G2CR Register

Group 2 IEBus Control Register



Symbol	Address	After Reset
IECR	0172_{16}	$00XX\ X000_2$

Bit Symbol	Bit Name	Function	RW
IEB	IEBus Enable Bit(1)	0 : Disables IEBus(2) 1 : Enables IEBus	RW
IETS	IEBus Transmit Start Request Bit	0 : Transmission is completed 1 : Transmission is started	RW
IEBBS	IEBus Busy Flag	0 : Idle state 1 : Busy state (start condition is detected)	RO
____ (b5 - b3)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
DF	Digital Filter Select Bit	0 : No digital filter 1 : Digital filter	RW
IEM	IEBus Mode Select Bit	0 : Mode 1 1 : Mode 2	RW

NOTES:
1. Set the IEB bit while the base timer clock is stopped.
2. After the IEB bit is set to "0", keep "0" for at least 1 f_{BT2} cycle. Set the BCK1 to BCK0 bits in the G2BCR0 register to "00_2" (clock stop) when setting the IEB bit to "1".

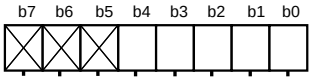
Group 2 IEBus Address Register

Symbol	Address	After Reset
IEAR	0171_{16} - 0170_{16}	Indeterminate

Function	RW
Address data	RW
Address data	RW
Nothing is assigned. When write, set to "0". When read, its content is indeterminate.	—

Figure 21.44 IECR and IEAR Registers

Group 2 IEBus Transmit Interrupt Cause Determination Register

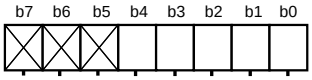


Symbol	Address	After Reset
IETIF	0173_{16}	$XXX0\ 0000_2$

Bit Symbol	Bit Name	Function	RW
IETNF	Normal Complete Flag(1)	0 : Transmission is completed in error 1 : Transmission is completed as expected	RW
IEACK	ACK Error Flag(1)	0 : No error found 1 : Error found	RW
IETMB	Maximum Transfer Byte Error Flag(1)	0 : No error found 1 : Error found	RW
IETT	Timing Error Flag(1)	0 : No error found 1 : Error found	RW
IEABL	Arbitration Lost Flag(1)	0 : No error found 1 : Error found	RW
____ (b7 - b5)	Nothing is assigned. When write, set to "0". When read, its contents is indeterminate.		_

NOTES:
1. This bit can be set to "0" by program, but cannot be set to "1". Set to "0" by setting the IEB bit in the IECR register to "0" (IEBus disabled to use).

Group 2 IEBus Receive Interrupt Cause Determination Register



Symbol	Address	After Reset
IERIF	0174_{16}	$XXX0\ 0000_2$

Bit Symbol	Bit Name	Function	RW
IERNF	Normal Completed Flag(1)	0 : Transmission is completed in error 1 : Transmission is completed as expected	RW
IEPAR	Parity Error Flag(1)	0 : No error found 1 : Error found	RW
IERMB	Max. Transfer Byte Error Flag(1)	0 : No error found 1 : Error found	RW
IERT	Timing Error Flag(1)	0 : No error found 1 : Error found	RW
IERETC	Other Cause Receive Completed Flag(1)	0 : No error found 1 : Error found	RW
____ (b7 - b5)	Nothing is assigned. When write, set to "0". When read, its contents is indeterminate.		_

NOTES:
1. This bit can be set to "0" by program, but not to "1". Set to "0" by setting the IEB bit in the IECR register to "0" (IEBus disabled to use).

Figure 21.45 IETIF and IERIF Registers

21.5.1 Variable Clock Synchronous Serial I/O Mode (Group 2)

In variable clock synchronous serial I/O mode, data is transmitted and received using the transfer clock. The length of data transferred is selected from 1 to 8 bits. Table 21.30 lists specifications of the group 2 variable clock synchronous serial I/O mode. Table 21.31 lists registers to be used and their settings. Tables 21.32 to 21.35 lists pin settings. Figure 21.46 shows an example of a transmit and receive operation.

Table 21.30 Variable Clock Synchronous Serial I/O Mode Specifications (Group 2)

Item	Specification
Transfer Data Format	• Transfer data length : 1 to 8 bits
Transfer Clock(1)	• When the CKDIR bit in the G2MR register is set to "0" (internal clock) : $\frac{f_{BT2}}{2(n+2)}$ n : setting value of the G2PO0 register 0000_{16} to $FFFF_{16}$ The G2PO0 register determines bit rate and the transfer clock is generated in phase-delayed waveform output mode of the channel 2 waveform generation function. • When the CKDIR bit is set to "1" (external clock) : input from the ISCLK2 pin(2)
Transmit Start Condition	• To start transmitting, the following conditions are required : - Set the TE bit in the G2CR register to "1" (transmit enable) - Write data to the G2TB register
Receive Start Condition	• To start receiving, the following conditions are required : - Set the RE bit in the G2CR register to "1" (receive enable) - Set the TE bit in the G2CR register to "1" (transmit enable) - Write data to the G2TB register
Interrupt Request	• While transmitting, one of the following conditions can be selected to set the SIO2TR bit in the IIO6IR register to "1" (see Figure 10.14): - The IRS bit in the G2MR register is set to "0" (no data in the G2TB register): when data is transferred from the G2TB register to the transmit register. - The IRS bit is set to "1" (reception completed): when data transfer from the transmit register is completed • While receiving, the following condition can be selected to set the SIO2RR bit in the IIO5IR register to "1" (interrupt request) (see Figure 10.14): when data is transferred from the receive register to the G2RB register (data reception is completed)
Error Detection	Overrun error(3) This error occurs when receiving the j bit (j=1 to 8) of the next data (transfer data length: j bits) before reading the G2RB register
Selectable Function	• LSB first/MSB first Select either bit 0 or bit 7 to transmit/receive data • ISTxD2 and ISRxD2 I/O polarity inverse ISTxD2 pin output level and ISRxD2 pin input level are inversed • Data transfer bit length Select from 1 to 8 bits

NOTES:

1. The transfer clock must be f_{BT2} divided by six or more when both transfer clock and transfer data are transmitted. Under conditions other than this, the transfer clock must be f_{BT2} divided by 20 or more.
2. Transfer clocks must be f_{BT2} divided by 20 or more.
3. When an overrun error occurs, the G2RB register is indeterminate.

Table 21.31 Register to be Used and Settings

Register	Bit	Function
G2BCR0	BCK1 to BCK0	Set to "11$_2$"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G2BCR1	7 to 0	Set to "0001 0010$_2$"
G2POCR0	7 to 0	Set to "0000 0111$_2$"
G2POCR1	7 to 0	Set to "0000 0111$_2$"
G2BCR2	7 to 0	Set to "0000 0010$_2$"
G2PO0	15 to 0	Set bit rate $\frac{f_{BT2}}{2 \times (\text{setting value} + 2)}$ = transfer clock frequency
G2PO2	15 to 0	Set to a value smaller than the G2PO0 register
G2FE	IFE2 to IFE0	Set to "111$_2$"
G2MR	GMD1 to GMD0	Set to "01$_2$"
	CKDIR	Select internal or external clock
	UFORM	Select either LSB first or MSB first
	IRS	Select how the transmit interrupt is generated
G2CR	TE	When transmission is enabled, set to "1"
	TXEPT	Transmit register empty flag
	TI	Transmit buffer empty flag
	RE	When reception is enabled, set to "1"
	RI	Receive complete flag
	OPOL	ISTxD2 output polarity inverse (usually set to "0")
	IPOL	ISRxD2 input polarity inverse (usually set to "0")
G2TB	15 to 0	Write transfer bit length and transmit data
G2RB	15 to 0	Received data and error flag are stored

Table 21.32 Pin Settings (1)

Port Name	Function	Bit and Setting					Register(2)
		PS1 Register	PSL1 Register	PSC Register	PD7 Register	IPS Register	
P7$_0$(1)	ISTxD2 output	PS1_0 = 1	PSL1_0 = 0	PSC_0 = 1	-	-	G2POCR0
P7$_1$	ISRxD2 input	PS1_1 = 0	-	-	PD7_1 = 0	IPS5 to 4 = 00$_2$	-

NOTES:
1. P7$_0$ is a port for the N-channel open drain output.
2. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function is used).

Table 21.33 Pin Settings (2)

Port Name	Function	Bit and Setting				Register(2)
		PS3 Register(1)	PSL3 Register	PD9 Register(1)	IPS Register	
P9$_1$	ISRxD2 input	PS3_1=0	-	PD9_1=0	IPS5 to 4=01$_2$	-
P9$_2$	ISTxD2 output	PS3_2=1	PSL3_2=1	-	-	G2POCR0

NOTES:
1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.
2. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).

Table 21.34 Pin Settings (3)

Port Name	Function	Bit and Setting				Register(1)
		PS0 Register	PSL0 Register	PD6 Register	IPS Register	
P6$_4$	ISCLK2 input	PS0_4 = 0	-	PD6_4 = 0	IPS6 = 0	-
	ISCLK2 output	PS0_4 = 1	PSL0_4 = 1	-	-	G2POCR1

NOTES:
1. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).

Table 21.35 Pin Settings (4)

Port Name	Function	Bit and Setting			Register(1)
		PS7 Register	PD13 Register	IPS Register	
P13$_4$	ISTxD2 output	PS7_4 = 1	-	-	G2POCR0
P13$_5$	ISRxD2 input	PS7_5 = 0	PD13_5 = 0	IPS5 to 4 = 10$_2$	-
P13$_6$	ISCLK2 input	PS7_6 = 0	PD13_6 = 0	IPS6 = 1	-
	ISCLK2 output	PS7_6 = 1	-	-	G2POCR1

NOTES:
1. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).

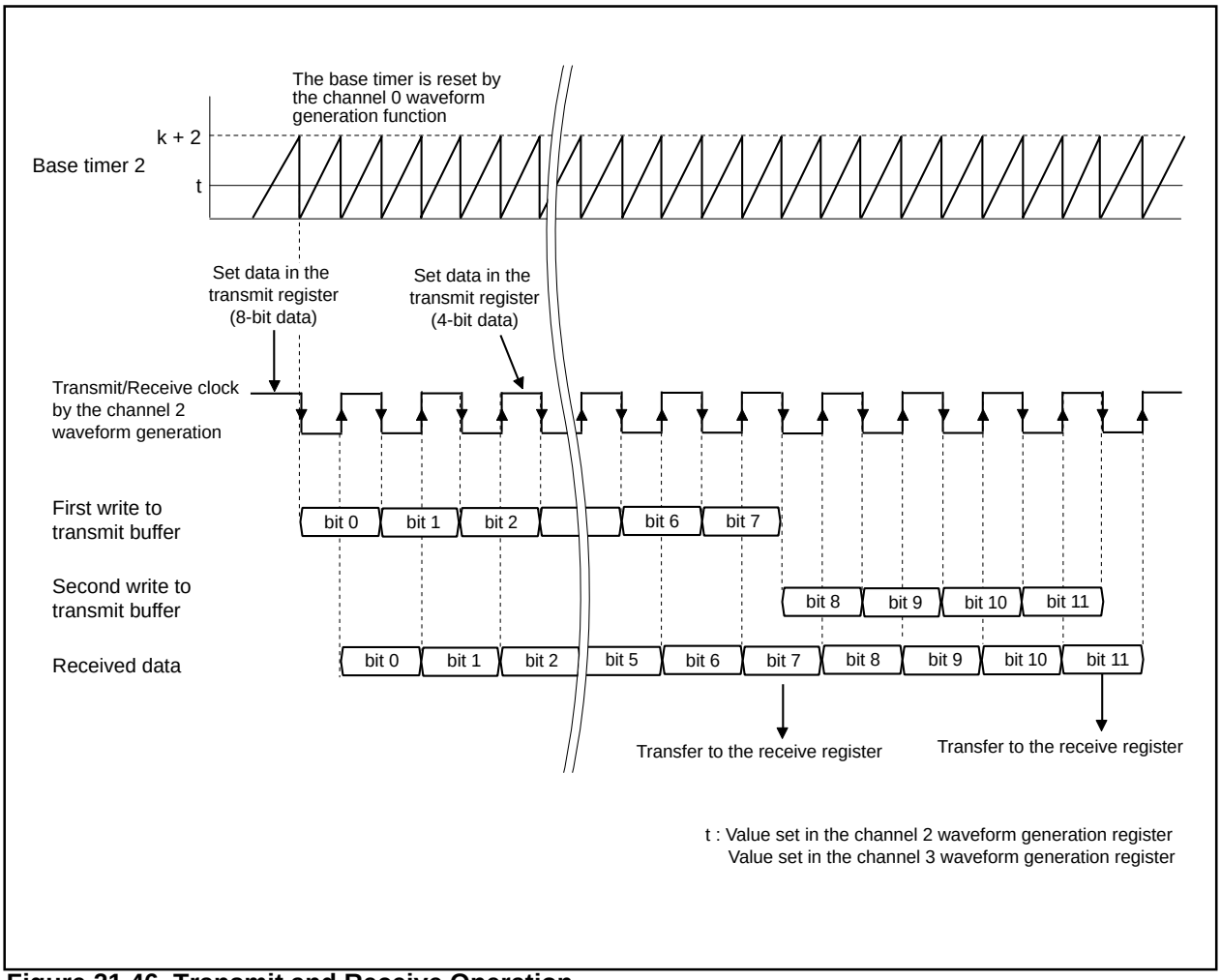


Figure 21.46 Transmit and Receive Operation

21.5.2 IEBus Mode (Group 2)

Table 21.36 lists specifications of IEBus mode. Table 21.37 lists registers to be used and settings. Tables 21.38 to 21.40 lists pin settings.

Table 21.36 IEBus Mode Specification

Item	Specification
Transfer Data Format	• Transfer data length: 1 to 8 bits
Transfer Clock	• When the CKDIR bit in the G2MR register is set to "0" (internal clock) : $\frac{f_{BT2}}{2(n+2)}$ n : setting value of the G2PO0 register, 0000_{16} to $FFFF_{16}$. The G2PO0 register determines bit rate and the transfer clock is generated in phase-delayed waveform output mode of the channel 2 waveform generation function. The G2PO2 register = $(n+2)/2$(1) • When the CKDIR bit is set to "1" (external clock) : input from the ISCLK2 pin(2)
Transmit Start Condition	To start transmitting, the following conditions are required : • Set the TE bit in the G2CR register to "1" (transmit enable) • Write data to G2TB register
Receive Start Condition	To start receiving, the following requirements must be met: • Set the RE bit in the G2CR register to "1" (receive enable) • Set the TE bit in the G2CR register to "1" (transmit enable) • Write data to the G2TB register
Interrupt Request	• While transmitting, the following conditions can be selected to set the SIO2TR bit in the IIO6R register to "1" (see Figure 10.14): - The IRS bit in the G2MR register is set to "0" (no data in the G2TB register): when data is transferred to the transmit register from the G2TB register (transmission started) - The IRS bit is set to "1" (reception completed): when data transfer from the transmit register to the G2TO register is completed • While receiving, the following condition can be selected to set the SIO2RR bit in the IIO5R register to "1" (see Figure 10.14): when data is transferred from receive register to the G2RB register (data reception is completed)
Error Detection	Overrun error(3) This error occurs when receiving the j bit (j=1 to 8) of the next data (transfer data length: j bits) before reading the G2RB register
Selectable Function	• LSB first/MSB first select Select either bit 0 or bit 7 to transmit/receive data • ISTxD2 and ISRxD2 I/O polarity inverse ISTxD2 pin output and ISRxD2 pin input levels are inversed • Data transfer bit length Select from 1 to 8 bits

NOTES:
1. The transfer clock must be f_{BT2} divided by six or more when both transfer clock and transfer data are transmitted. Under conditions other than this, the transfer clock must be f_{BT2} divided by 20 or more.
2. Transfer clock must be input f_{BT2} divided by 20 or more.
3. When an overrun error occurs, the G2RB register is indeterminate.

Table 21.37 Registers to be Used and Settings

Register	Bit	Function
G2BCR0	BCK1 to BCK0	Set to "11$_2$"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G2BCR1	7 to 0	Set to "00010010$_2$"
G2POCR0 to G2POCR7	MOD2 to MOD0	Set to "111$_2$"
	PRT	Set to "0"
	IVL	Set to "0"
	RLD	Set to "0"
	RTP	Set to "0"
	INV	Set to "0"
G2PO0 to G2PO7	15 to 0	Set compared data for waveform generation
G2FE	7 to 0	Set bit of corresponding channel to "1"
G2MR	GMD1 to GMD0	Select serial I/O mode
	CKDIR	Select internal clock or external clock
	UFORM	Select either LSB first or MSB first
	IRS	Select how the transmit interrupt is generated
G2CR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	When transmission is enabled, set to "1"
	RE	When reception is enabled, set to "1"
	IPOL	ISRxD2 output polarity inverse (usually set to "0")
	OPOL	ISTxD2 output polarity inverse (usually set to "0")
IECR	IEB	Set to "1"
	IETS	When transmission starts, set to "1"
	IEBBS	Select IEBus busy flag
	DF	Select whether the digital filter is available or not
	IEM	Select mode
IEAR	11 to 0	Set address data
IETIF	IETNF	Normal complete flag when transmitting
	IEACK	ACK error flag when transmitting
	IETMB	Maximum transfer byte error flag when transmitting
	IETT	Timing error flag when transmitting
	IEABL	Arbitration lost flag when transmitting
IERIF	IERNF	Normal complete flag when receiving
	IEPAR	Parity error flag when receiving
	IERMB	Maximum transfer byte error flag when receiving
	IERT	Timing error flag when receiving
	IERETC	Other cause receive completed flag when receiving
G2RB	7 to 0	Received data and error flag are stored
	OER	Overrun error flag
G2TB	7 to 0	Write transfer bit length and data to be transmitted

Table 21.38 Pin Settings (1)

Port Name	Function	Bit and Setting					Register(2)
		PS1 Register	PSL1 Register	PSC Register	PD7 Register	IPS Register	
P70(1)	IEOUT output	PS1_0 = 1	PSL1_0 = 0	PSC_0 = 1	-	-	G2POCR0
P71	IEIN input	PS1_1 = 0	-	-	PD7_1 = 0	IPS5 to 4 = 002	-

NOTES:
1. P70 is a port for the N-channel open drain output.
2. Set the MOD2 to MOD0 bits in the G2POCR0 register to "1112".

Table 21.39 Pin Settings (2)

Port Name	Function	Bit and Setting				Register(1)
		PS3 Register(2)	PSL3 Register	PD9 Register(2)	IPS Register	
P91	IEIN input	PS3_1 = 0	-	-	IPS5 to 4 = 012	-
P92	IEOUT output	PS3_2 = 1	PSL3_2 = 1	PD9_2 = 0	-	G2POCR0

NOTES:
1. Set the MOD2 to MOD0 bits in the G2POCR0 register to "1112".
2. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

Table 21.40 Pin Settings (3)

Port Name	Function	Bit and Setting			Register(1)
		PS7 Register	PSL7 Register	IPS Register	
P134	IEOUT output	PS7_4 = 1	-	-	G2POCR0
P135	IEIN input	PS7_5 = 0	PD13_5 = 0	IPS5 to 4 = 102	-

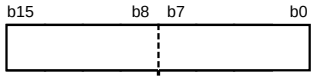
NOTES:
1. Set the MOD2 to MOD0 bits in the G2POCR0 register to "1112".

21.6 Group 3 Communication Function

The communication function is available when two 16-bit shift registers are used with the waveform generation function.

In the intelligent I/O group 3, 8-bit or 16-bit synchronous communication function is available. Figures 21.47 to 21.49 show registers associated with the communication function.

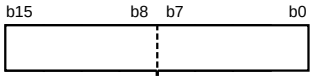
Group 3 SI/O Transmit Buffer Register



Symbol	Address	After Reset
G3TB	017D16 - 017C16	Indeterminate

Bit Name	Function	RW
Transmit Buffer	Data to be transmitted (8 low-order bits)	WO
	Data to be transmitted (8 high-order bits)	WO

Group 3 SI/O Receive Buffer Register

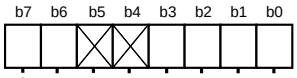


Symbol	Address	After Reset
G3RB	017F16 - 017E16	Indeterminate

Bit Name	Function	RW
Receive Buffer	Received data (8 low-order bits)	RO
	Received data (8 high-order bits)	RO

Figure 21.47 G3TB Register and G3RB Register

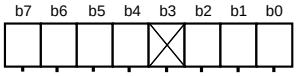
Group 3 SI/O Communication Mode Register



Symbol	Address	After Reset
G3MR	$017A_{16}$	$00XX\ 0000_2$

Bit Symbol	Bit Name	Function	RW
GMD0	Communication Mode Select Bit	b1 b0 0 0 : Communication unit is reset (The ROER bit is set to "0") 0 1 : Clock synchronous serial I/O mode 1 0 : Do not set to this value 1 1 : Do not set to this value	RW
GMD1			RW
CKDIR	Internal/External Clock Select Bit	0 : Internal clock 1 : External clock	RW
TLD	Transfer Data Length Select Bit	0 : 16 bits long 1 : 8 bits long	RW
____ (b5 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
UFORM	Transfer Format Select Bit	0 : LSB first 1 : MSB first	RW
IRS	Transmit Interrupt Cause Select Bit	0 : No data is in the transmit buffer 1 : Transmission is completed	RW

Group 3 SI/O Communication Control Register

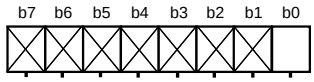


Symbol	Address	After Reset
G3CR	$017B_{16}$	$0000\ X000_2$

Bit Symbol	Bit Name	Function	RW
TE	Transmit Enable Bit	0 : Transmit disable 1 : Transmit enable	RW
TXEPT	Transmit Register Empty Flag	0 : Data is in transmit register (during transmission) 1 : No data is in the transmit register (transmission is completed)	RO
TI	Transmit Buffer Empty Flag	0 : Data is in the G3TB register 1 : No data is in the G3TB register	RO
____ (b3)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
RE	Receive Enable Bit	0 : Receive disabled 1 : Receive enabled	RW
RI	Receive Complete Flag	0 : No data is in the G3RB register 1 : Data is in the G3RB register	RO
OPOL	ISTxD Output Polarity Switch Bit	0 : No inverse 1 : Inverse	RW
IPOL	ISRxD Input Polarity Switch Bit	0 : No inverse 1 : Inverse	RW

Figure 21.48 G3MR Register and G3CR Register

Group 3 SI/O Communication Flag Register



Symbol	Address	After Reset
G3FLG	$01AD_{16}$	XXXX $XXX0_2$

Bit Symbol	Bit Name	Function	RW
ROER	Receive Overrun Error Flag(1)	0 : No error found 1 : Error found	RO
____ (b7 - b1)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. The ROER bit is set to "0" when the RE bit in the G3CR register is set to "0".

Figure 21.49 G3FLG Register

21.6.1 8-bit or 16-bit Clock Synchronous Serial I/O Mode (Group 3)

In 8-bit or 16-bit clock synchronous serial I/O mode, data is transmitted and received using the transfer clock. When the internal clock is selected as the transfer clock, the channel 0 and channel 2 waveform generation functions generate the transfer clock. ISTxD3, ISCLK3 and ISRxD3 share pins with OUTC30 to OUTC32 and are available in the 144-pin package only.

Table 21.41 lists specifications of clock synchronous serial I/O mode. Table 21.42 lists registers to be used and their settings. Tables 21.43 and 21.44 list pin settings. Figure 21.50 and 21.51 shows an example of transmit and receive operation.

Table 21.41 Clock Synchronous Serial I/O Mode (Group 3)

Item	Specification
Transfer Data Format	• Transfer data : 8 bits or 16 bits long
Transfer Clock(1)	• When the CKDIR bit in the G3MR register is set to "0" (internal clock) : $\frac{f_{BT3}}{2(n+2)}$ n : setting value of the G3PO0 register, 0001_{16} to $FFFD_{16}$ – The G3PO0 register determines the bit rate and the transfer clock is generated in phase-delayed waveform output mode of the channel 2 waveform generation function. • When the CKDIR bit is set to "1" (external clock) : input from the ISCLK3 pin
Transmit Start Condition(2)	Set registers associated with the waveform generation function and the G3MR register. Then, set as written below after waiting at least one transfer clock cycle. • Set the TE bit in the G3CR register to "1" (transmit enable) • Set the TI bit in the G3CR register to "0" (data in the G3TB register)
Receive Start Condition	Set registers associated with the waveform generation function and the G3MR register. Then, set as written below after waiting at least one transfer clock cycle. • Set the RE bit in the G3CR register to "1" (receive enable) • Set theTE bit to "1" (transmit enable) • Set the TI bit to "0" (data in the G3TB register)
Interrupt Request	• While transmitting, one of the following conditions can be selected to set the SIO3TR bit in the IIO10IR register to "1" (see Figure 10.14) : – When the IRS bit in the G3MR register is set to "0" (no data in the transmit buffer), one transfer clock cycle after data transmission starts – When the IRS bit is set to "1" (reception completed), 15 transfer clock cycles after data transmission starts in 16-bit clock synchronous serial I/O mode (set the DLS bit in the G3MR register to "0"), or 7 transfer clock cycles after data transmission starts in 8-bit clock clock synchronous serial I/O mode (set the DLS bit to "1"). • While receiving, the following condition can be selected to set the SIO3RR bit in the IIO9IR register to "1" (see Figure 10.14) : 15.5 transfer clock cycles after data transmission starts in 16-bit clock synchronous serial I/O mode, or 7.5 transfer clock cycles after data transmission starts in 8-bit clock synchronous serial I/O mode
Error Detection	• Overrun error(3) This error occurs in 16-bit clock synchronous serial I/O mode when the 15th bit of the next data is received before reading the G3RB register. This error occurs in 8-bit clock synchronous serial I/O mode when the 7th bit of the next data is received before reading the G3RB register.
Selectable Function	• LSB first/MSB first Select either bit 0 or bit 7 to transmit/receive data • ISTxD3 and ISRxD3 I/O polarity inverse ISTxD3 pin output level and ISRxD3 pin input level are inversed

NOTES:
1. The transfer clock must be f_{BT3} divided by six or more.
2. Transmit interrupt request is generated when the TE bit is set to "1". Set the interrupt-associated registers after setting the TE bit.
3. When an overrun error occurs, the G3RB register is indeterminate.

Table 21.42 Registers to be Used and Settings

Register	Bit	Function
G3BCR0	BCK1 to BCK0	Set to "11$_2$"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G3BCR1	7 to 0	Set to "0001 0010$_2$"
G3POCR0	7 to 0	Set to "0000 0111$_2$"
G3POCR1	7 to 0	Set to "0000 0111$_2$"
G3POCR2	7 to 0	Set to "0000 0010$_2$"
G3PO0	15 to 0	Set bit rate $\frac{f_{BT3}}{2 \times (\text{setting value} + 2)}$ = transfer clock frequency
G3PO2	15 to 0	Set to a value smaller than the G3PO0 register
G3FE	7 to 0	Set to "0000 0111$_2$"
G3MR	GMD1 to GMD0	Set to "01$_2$"
	CKDIR	Select the internal clock or external clock
	TLD	Select transfer data length
	UFORM	Select either LSB first or MSB first
	IRS	Select how the transmit interrupt is generated
G3CR	TE	Set to "1" to enable transmission
	TXEPT	Transmit register empty flag
	TI	Transmit buffer empty flag
	RE	Set to "1" to enable reception
	RI	Receive complete flag
	OPOL	ISTxD3 output polarity inverse (usually set to "0")
	IPOL	ISRxD3 input polarity inverse
G3TB	15 to 0	Write transmit data
G3RB	15 to 0	Received data is stored

Table 21.43 Pin Setting in Clock Synchronous Serial I/O Mode (Group 3)

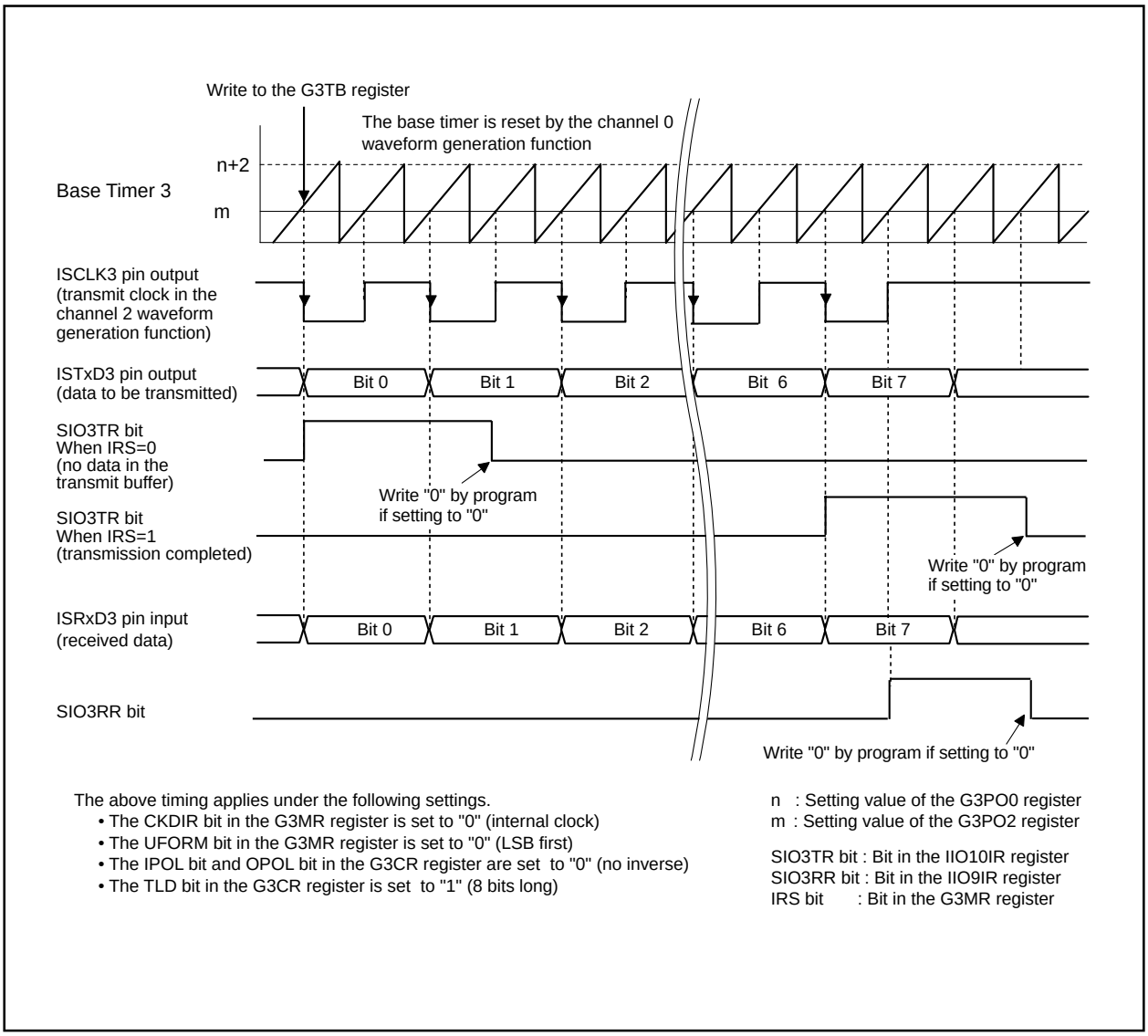
Port Name	Function	Bit and Setting				Register(1)
		PS2 Register	PSL2 Register	PD8 Register	IPS Register	
P8$_1$	ISTxD3 output	PS2_1 = 1	PSL2_1 = 1	-	-	G3POCR0
P8$_2$	ISRxD3 input	PS2_2 = 0	-	PD8_2 = 0	IPS7 = 0	-

NOTES:
1. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).

Table 21.44 Pin Setting (Continued)

Port Name	Function	Bit and Setting			Register(1)
		PS6 Register	PD12 Register	IPS Register	
P12$_0$	ISTxD3 output	PS6_0 =1	-	-	G3POCR0
P12$_1$	ISCLK3 input	PS6_1 = 0	PD12_1 = 0	-	-
	ISCLK3 output	PS6_1 = 1	-	-	G3POCR1
P12$_2$	ISRxD3 input	PS6_2 = 0	PD12_2 = 0	IPS7 = 1	-

NOTES:
1. Set the MOD2 to MOD0 bits in the corresponding register to "111$_2$" (output of the communication function used).



The above timing applies under the following settings.
- The CKDIR bit in the G3MR register is set to "0" (internal clock)
- The UFORM bit in the G3MR register is set to "0" (LSB first)
- The IPOL bit and OPOL bit in the G3CR register are set to "0" (no inverse)
- The TLD bit in the G3CR register is set to "1" (8 bits long)

n : Setting value of the G3PO0 register
m : Setting value of the G3PO2 register

SIO3TR bit : Bit in the IIO10IR register
SIO3RR bit : Bit in the IIO9IR register
IRS bit : Bit in the G3MR register

Figure 21. 50 Transmit and Receive Operation (8-bit Length)

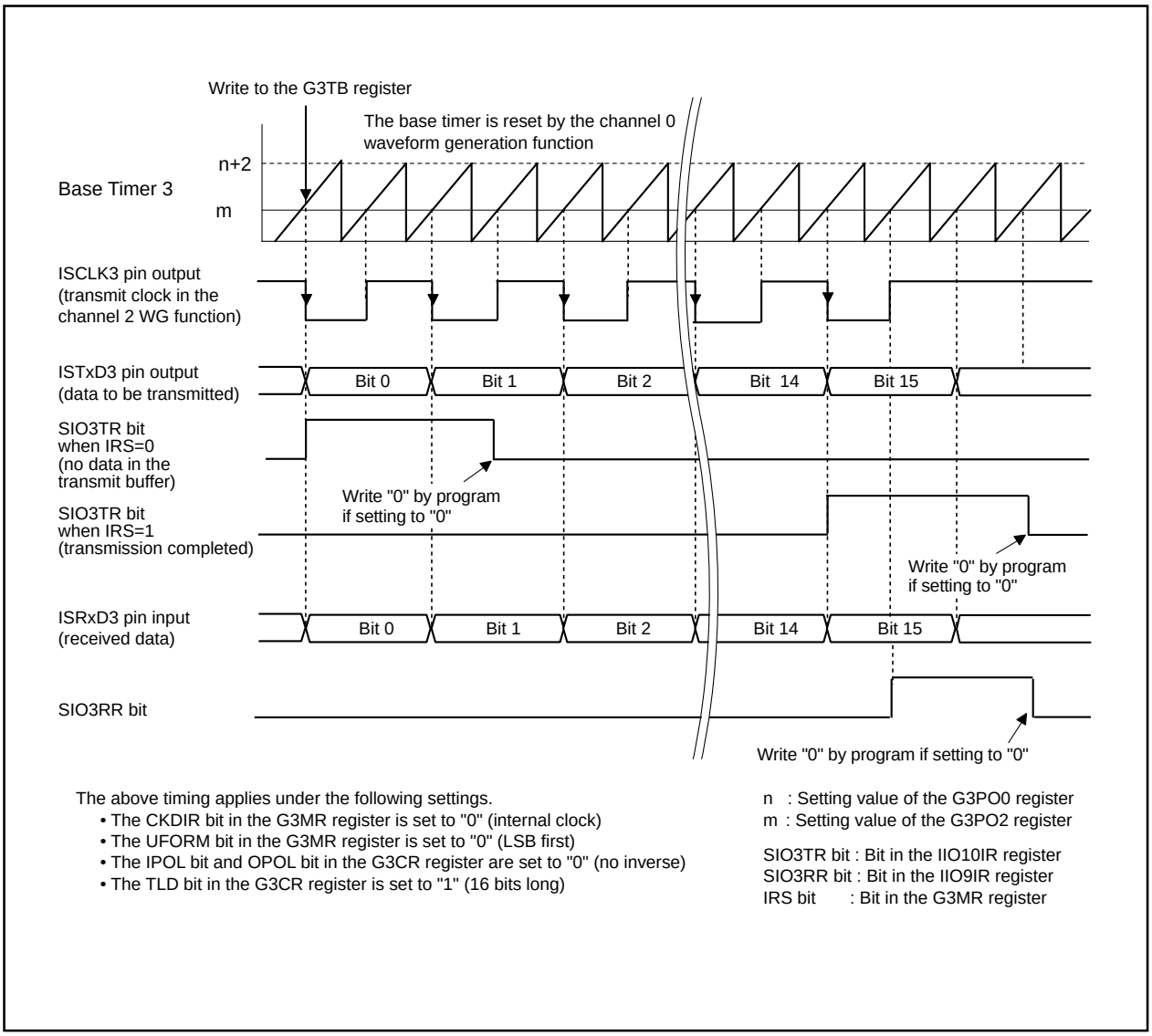


Figure 21. 51 Transmit and Receive Operation (16-bit Length)

22. CAN Module

The CAN (Controller Area Network) module incorporated in the M32C/83 group is a Full CAN module, compatible with CAN Specification 2.0 Part B. Table 22.1 lists specifications of the CAN module.

Table 22.1 CAN Module Specifications

Item	Specification
Protocol	CAN Specification 2.0 Part B
Message Slots	16 slots
Polarity	Dominant: "L" Recessive: "H"
Acceptance Filter	Global mask: 1 mask (for message slots 0 to 13) Local mask: 2 masks (for message slots 14 and 15 respectively)
Baud Rate	Baud rate = $\frac{1}{\text{Tq clock cycle x Tq per bit}}$ --- Max. 1 Mbps Tq clock cycle = $\frac{\text{BRP + 1}}{f_1}$ Tq per bit = SS + PTS +PBS1+PBS2 Tq: Time quantum BRP: Setting value in the C0BRP and C1BRP registers, 1-255 SS: Synchronization Segment; 1 Tq PTS: Propagation Time Segment; 1 to 8 Tq PBS1: Phase Buffer Segment 1; 2 to 8 Tq PBS2: Phase Buffer Segment 2 ; 2 to 8 Tq
Remote Frame Automatic Answering Function	Message slot that receives the remote frame transmits the data frame automatically
Time Stamp Function	Time stamp function with a 16-bit counter. Count source can be selected from the CAN bus bit clock divided by 1, 2, 3 or 4.
BasicCAN Mode	BasicCAN function can be used with the CANi message slots 14 and 15.
Transmit Abort Function	Transmit request is aborted
Loopback Function	Frame transmitted by the CAN module is received by the same CAN module
Forcible Error Active Clear Function	The CAN module is forced into an error active state

NOTES:
1. Use an oscillator with maximum 1.58% oscillation tolerance.

Figure 22.1 shows a block diagram of the CAN module. Figure 22.2 shows CANi message slot buffer (the message slot buffer) (i=0,1) and CANi message slot (the message slot) j (j=0 to 15). Table 22.2 lists pin settings of the CAN module.

The message slot cannot be accessed directly from the CPU. Allocate the message slot j to be used to the message slot buffer 0 or 1. The message slot j is accessed via the message slot buffer address. The CiSBS register selects the message slot j to be allocated. Figure 22.2 shows the 16-byte message slot buffer and message slot.

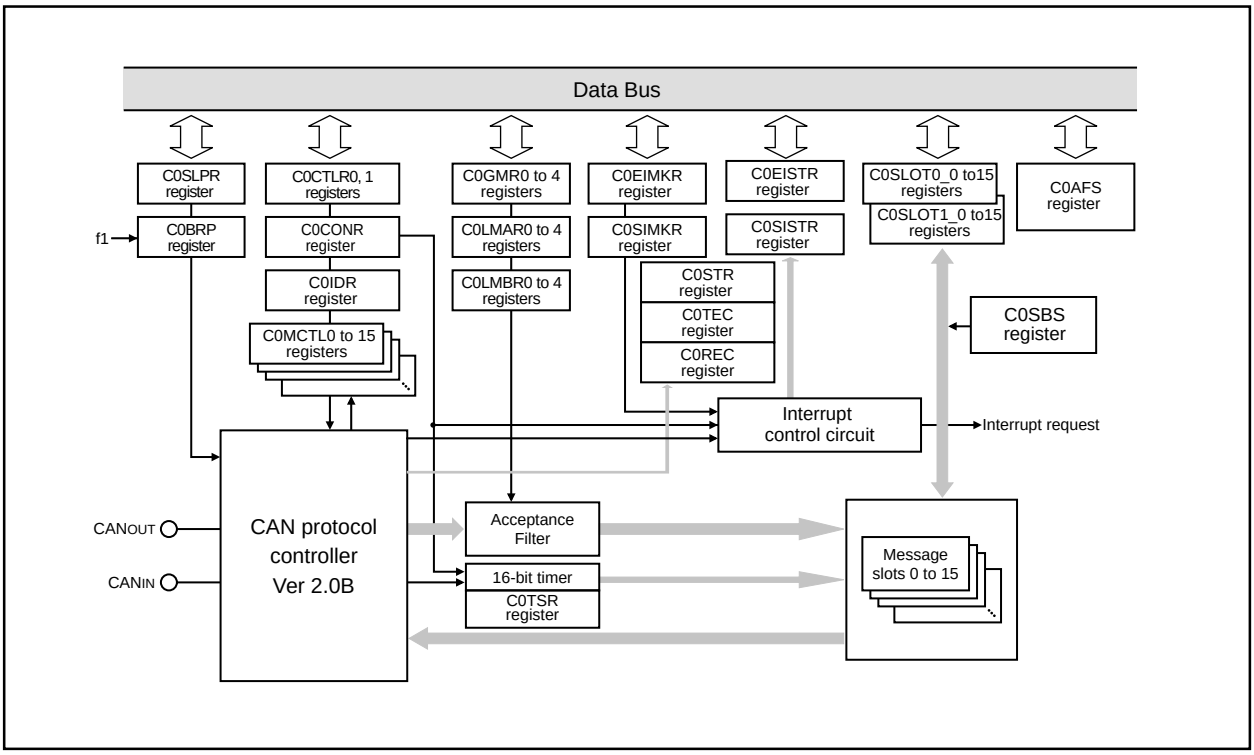


Figure 22.1 CAN Module Block Diagram

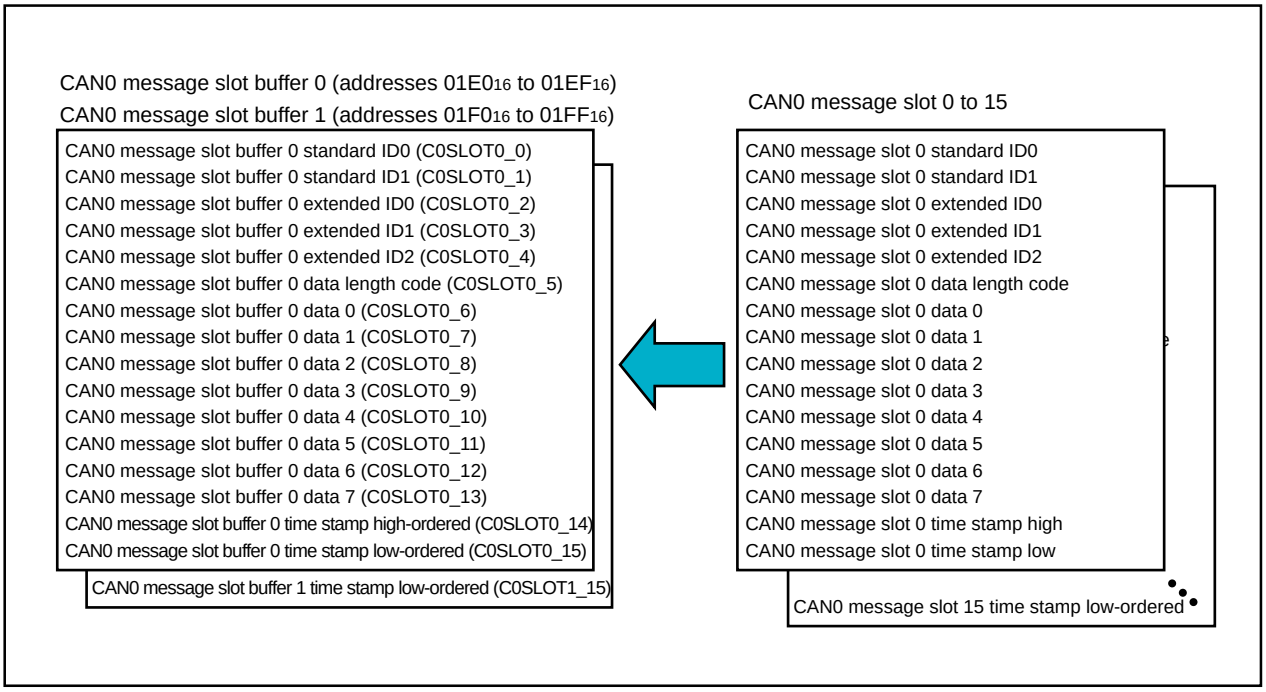


Figure 22.2 Message Slot Buffer and Message Slot

Table 22.2 Pin Settings

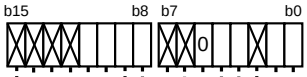
Port	Function	Bit and Setting				
		PS1, PS2 Registers	PSL1, PSL2 Registers	PSC Registers	IPS Registers	PD7, PD8 Registers
P7₆	CANOUT	PS1_6=1	PSL1_6=0	PSC_6=1	–	–
P7₇	CANIN	PS1_7=0	–	–	IPS3=0	PD7_7=0
P8₂	CANOUT	PS2_2=1	PSL2_2=1	–	–	–
P8₃	CANIN	–	–	–	IPS3=1	PD8_3=0

22.1 CAN-Associated Registers

Figures 22.3 to 22.26 show registers associated with CAN. To access the associated registers, set the MCD4 to MCD0 bits in the MCD register to "10010$_2$" (no division of CPU clock), the PM13 bit in the PM1 register to "1" (2 wait states), and the CM07 bit in the CM0 register to "0" (XIN-XOUT selected).

22.1.1 CAN0 Control Register 0 (C0CTLR0 Register)

CAN0 Control Register 0



Symbol	Address	After Reset(1)
C0CTLR0	0201$_{16}$ - 0200$_{16}$	XXXX 0000 XX01 0X01$_2$

Bit Symbol	Bit Name	Function	RW
RESET0	CAN Reset Bit 0	0: CAN module is not reset 1: CAN module is reset(2)	RW
LOOPBACK	Loop Back Mode Select Bit	0: Disables Loop back function 1: Enables Loop back function	RW
(b2)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
BASICCAN	Basic CAN Mode Select Bit	0 : Disables basic CAN mode function 1 : Enables basic CAN mode function	RW
RESET1	CAN Reset Bit 1	0: CAN module is not reset 1: CAN module is reset(2)	RW
(b5)	Reserved Bit	Set to "0".	RW
(b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
TSPRE0	Time Stamp Prescaler Select Bit	b9 b8 0 0: Selects the CAN bus bit clock 0 1: Selects the CAN bus bit clock divided by 2 1 0: Selects the CAN bus bit clock divided by 3 1 1: Selects the CAN bus bit clock divided by 4	RW
TSPRE1			RW
TSRESET	Time Stamp Counter Reset Bit	When this bit is set to "1", the C0TSR register is set to "0000$_{16}$". After that, this bit is automatically set to "0".(3)	RW
ECRESET	Error Counter Reset Bit	When this bit is set to "1", the C0TEC and C0REC registers are set to "00$_{16}$". After that, this bit is automatically set to "0".(3)	RW
(b15 - b12)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
2. Set the RESET0 bit and RESET1 bit to the same value simultaneously.
3. This bit can be set to "1" by program, but cannot be set to "0".

Figure 22.3 C0CTLR0 Register

22.1.1.1 RESET0 Bit and RESET1 Bit

When both RESET0 and RESET1 bits are set to "1", the CAN module is immediately reset regardless of ongoing CAN communication.

After the RESET0 and RESET1 bits are set to "1" and the CAN module reset is completed, the C0TSR register is set to "0000$_{16}$". The C0TEC and C0REC registers are set to "00$_{16}$" and the STATE_ERRPAS and STATE_BUSOFF bits in the C0STR register are set to "0" as well.

When both RESET0 and RESET1 bits are changed "1" to "0", the C0TSR register starts counting. CAN communication is available after 11 continuous recessive bits are detected.

NOTES:

1. Set the same value in both RESET0 and RESET1 bits simultaneously.
2. Set CAN configuration upon confirming that the STATE_RESET bit in the C0STR register is set to "1" (CAN module reset completed) after setting the RESET0 and RESET1 bits to "1".
3. The CAN$_{OUT}$ pin outputs an "H" signal as soon as the RESET0 and RESET1 bits are set to "1". CAN bus error may occur when the RESET0 and RESET1 bits are set to "1" while the CAN frame is transmitting.
4. For CAN communication, set the PS1, PS2, PSL1, PSL2, PSC, and IPS registers when the STATE_RESET bit is set to "1" (CAN module reset completed).

22.1.1.2 LOOPBACK Bit

When the LOOPBACK bit is set to "1" (loopback function enabled) and the receive message slot has a matched ID and frame format with a transmitted frame, the transmitted frame is stored to the receive message slot.

NOTES:

1. No ACK for the transmitted frame is returned.
2. Change the LOOPBACK bit only when the STATE_RESET bit is set to "1" (CAN module reset completed).

22.1.1.3 BASICCAN Bit

When the BASICCAN bit is set to "1", the message slots 14 and 15 enter BasicCAN mode.

In BasicCAN mode, the message slots 14 and 15 are used as dual-structured buffers. The message slot 14 and 15 alternately store a received frame having matched ID detected by acceptance filtering. The ID in the message slot 14 and the C0LMAR0 to C0LMAR4 registers are used for acceptance filtering when the message slot 14 is active (the next received frame is to be stored in the message slot 14). The ID in the message slot 15 and the C0LMBR0 to C0LMBR4 registers are used when the message slot 15 is active. Both data frame and remote frame can be received.

When entering BasicCAN mode, set the same ID in two message slots and set the same values in the C0LMAR0 to C0LMAR4 registers and in the C0LMBR0 to C0LMBR4 registers.

Follow the procedure below to enter BasicCAN mode.

(1) Set the BASICCAN bit to "1".

(2) Set IDs in the message slots 14 and 15. Set the C0LMAR0 to C0LMAR4 registers and C0LMBR0 to C0LMBR4 registers. (Set to the same values.)

(3) Set the IDE14 and 15 bits in the C0IDR register to select a frame format (standard or extended) for the message slots 14 and 15. (Set to the same format.)

(4) Set the REMACTIVE bit in the C0MCTL14 and C0MCTL15 registers in the message slots 14 and 15 to "0" (data frame received) and the RECREQ bit to "1" (request to receive).

NOTES:
1. Change the BASICCAN bit only when the STATE_RESET bit is set to "1" (CAN module reset completed).
2. The message slot 14 is the first slot to become active after the RESET0 and RESET1 bits are set to "0".
3. The message slots 0 to 13 are not affected by entering BasicCAN mode.

22.1.1.4 TSPRE1, TSPRE0 Bits

The TSPRE1 and TSPRE0 bits determine which count source is used for the time stamp counter.

NOTES:
1. Change the TSPRE1 to TSPRE0 bits only when the STATE_RESET bit is set to "1" (CAN module reset completed).

22.1.1.5 TSRESET Bit

When the TSRESET bit is set to "1" (counter reset), the C0TSR register is set to "0000$_{16}$". The TSRESET bit is automatically set to "0" after the C0TSR register is set to "0000$_{16}$".

22.1.1.6 ECRESET Bit

When the ECRESET bit is set to "1", the C0TEC and C0REC registers are set to "00$_{16}$". The CAN module forcibly goes into an error active state.

The ECRESET bit is automatically set to "0" after the CAN module enters an error active state.

NOTES:
1. In an error active state, the CAN module is ready to communicate when 11 continuous recessive bits are detected on the CAN bus.

22.1.2 CAN0 Control Register 1 (C0CTLR1 Register)

CAN0 Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
X	X	0	0		0	X	X

Symbol	Address	After Reset(1)
C0CTLR1	0241_{16}	$XX00\ 00XX_2$

Bit Symbol	Bit Name	Function	RW
____ (b1 - b0)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
____ (b2)	Reserved Bit	Set to "0".	RW
BANKSEL	CAN0 Bank Switch Bit	0 : Selects the message slot control register 1 : Selects the masked register	RW
____ (b5 - b4)	Reserved Bit	Set to "0".	RW
____ (b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Figure 22.4 C0CTLR1 Register

22.1.2.1 BANKSEL Bit

The BANKSEL bit in the C0CTLR1 register selects the registers allocated to addresses 0220_{16} to $023F_{16}$.

The C0MCTL0 to C0MCTL15 registers can be accessed by setting the BANKSEL bit to "0". The C0GMR0 to C0GMR4 registers, C0LMAR0 to C0LMAR4 registers and C0LMBR0 to C0LMBR4 registers can be accessed by setting the BANKSEL bit to "1".

22.1.3 CAN0 Sleep Control Register (C0SLPR Register)

CAN0 Sleep Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	

Symbol	Address	After Reset
C0SLPR	0242_{16}	XXXX $XXX0_2$

Bit Symbol	Bit Name	Function	RW
SLEEP	Sleep Mode Control Bit	0 : Enters sleep mode 1 : Exits sleep mode (Note 1)	RW
____ (b7 - b1)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

NOTES:
1. Set up CAN module configuration after CAN sleep mode is exited. While the CAN module is in sleep mode, no SFR (addresses $01E0_{16}$ to 0245_{16}) for the CAN module, except the C0SLPR register, can be accessed.

Figure 22.5 C0SLPR Register

22.1.3.1 SLEEP Bit

When the SLEEP bit is set to "0", the clock supplied to the CAN module stops running and enters sleep mode.

When the SLEEP bit is set to "1", the clock supplied to the CAN module starts running and exits sleep mode.

NOTES:
1. Enter sleep mode after the STATE_RESET bit in the C0STR register is set to "1" (CAN module reset completed).

22.1.4 CAN0 Status Register (C0STR Register)

CAN0 Status Register

b15 b8 b7 b0

Symbol	Address	After reset(1)
C0STR	0203_{16} - 0202_{16}	X000 0X01 0000 0000$_2$

Bit Symbol	Bit Name	Function	RW
MBOX0	Active Slot Determination Bit	b3 b2 b1 b0 0 0 0 0 : Message slot 0 0 0 0 1 : Message slot 1 0 0 1 0 : Message slot 2 0 0 1 1 : Message slot 3 . . . . 1 1 0 1 : Message slot 13 1 1 1 0 : Message slot 14 1 1 1 1 : Message slot 15	RO
MBOX1			RO
MBOX2			RO
MBOX3			RO
TRMSUCC	Transmit Complete State Flag	0: Transmission is not completed 1: Transmission is completed	RO
RECSUCC	Receive Complete State Flag	0: Reception is not completed 1: Reception is completed	RO
TRMSTATE	Transmit State Flag	0: Not transmitting 1: During transmission	RO
RECSTATE	Receive State Flag	0: Not receiving 1: During reception	RO
STATE_RESET	CAN Reset State Flag	0: CAN module is operating 1: CAN module reset is completed	RO
STATE_LOOPBACK	Loop Back State Flag	0: Mode except Loop back mode 1: Loop back mode	RO
(b10)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
STATE_BASICCAN	Basic CAN State Flag	0: Mode except Basic CAN mode 1: Basic CAN mode	RO
STATE_BUSERROR	CAN Bus Error State Flag	0: No error occurs 1: Error occurs	RO
STATE_ERRPAS	Error Passive State Flag	0: No error passive state 1: Error passive state	RO
STATE_BUSOFF	Bus-off State Flag	0: No bus-off state 1: Bus-off state	RO
(b15)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Figure 22.6 C0STR Register

22.1.4.1 MBOX3 to MBOX0 Bits

The MBOX3 to MBOX0 bits store relevant slot numbers when the CAN module has completed transmitting data or storing received data.

22.1.4.2 TRMSUCC Bit

The TRMSUCC bit is set to "1" when the CAN module has transmitted data as expected.

The TRMSUCC bit is set to "0" when the CAN module has received data as expected.

22.1.4.3 RECSUCC Bit

The RECSUCC bit is set to "1" when the CAN module has received data as expected. (Whether received message has been stored in the message slot or not is irrelevant.) If the received message is transmitted in loopback mode, the TRMSUCC bit is set to "1" and the RECSUCC bit is set to "0".
The RECSUCC bit is set to "0" when the CAN module has transmitted data as expected.

22.1.4.4 TRMSTATE Bit

The TRMSTATE bit is set to "1" when the CAN module is performing as a transmit node.
The TRMSTATE bit is set to "0" when the CAN module is in a bus-idle state or starts performing as a receive node.

22.1.4.5 RECSTATE Bit

The RECSTATE bit is set to "1" when the CAN module is performing as a receive node.
The RECSTATE bit is set to "0" when the CAN module is in a bus-idle state or starts performing as a transmit node.

22.1.4.6 STATE_RESET Bit

After both RESET0 and RESET1 bits are set to "1" (CAN module reset), the STATE_RESET bit is set to "1" as soon as the CAN module is reset.
The STATE_RESET bit is set to "0" when the RESET0 and RESET1 bits are set to "0".

22.1.4.7 STATE_LOOPBACK Bit

The STATE_ LOOPBACK bit is set to "1" when the CAN module is in loopback mode.
The STATE_LOOPBACK bit is set to "1" when the LOOPBACK bit in the C0CTLR0 register is set to "1" (loop back function enabled).
The STATE_LOOPBACK bit is set to "0" when the LOOPBACK bit is set to "0" (loop back function disabled).

22.1.4.8 STATE_BASICCAN Bit

The STATE_BASICCAN bit is set to "1" when the CAN module is in BasicCAN mode.
Refer to **22.1.1.3 BASICCAN Bit** for BasicCAN mode.
The STATE_BASICCAN bit is set to "0" when the BASICCAN bit is set to "0" (BasicCAN mode function disabled).
The STATE_BASICCAN bit is set to "1" when the BASICCAN bit is set to "1" (BasicCAN mode function enabled), the REMACTIVE bits in the C0MCTL14 and C0MCTL15 registers in the message slot 14 and 15 are set to "0" (data frame received) and the RECREQ bit is set to "1" (request to receive the frame).

22.1.4.9 STATE_BUSERROR Bit

The STATE_BUSERROR bit is set to "1" when an CAN communication error is detected.
The STATE_BUSERROR bit is set to "0" when the CAN module has transmitted or received data as expected. Whether a received message has been stored into the message slot or not is irrelevant.
NOTES:

1. When the STATE_BUSERROR bit is set to "1", the STATE_BUSERROR bit remains unchanged even if both RESET 0 and RESET1 bits are set to "1" (CAN module reset).

22.1.4.10 STATE_ERRPAS Bit

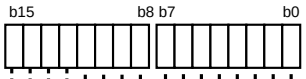
The STATE_ERRPAS bit is set to "1" when the value of the C0TEC or C0REC register exceeds 127 and places the CAN module in an error-passive state.
The STATE_ERRPAS bit is set to "0" when the CAN module in an error passive state is placed in another error state.
The STATE_ERRPAS bit is set to "0" when both RESET0 and RESET1 bits are set to "1" (CAN module is reset).

22.1.4.11 STATE_BUSOFF Bit

The STATE_BUSOFF bit is set to "1" when the value of the C0TEC register exceeds 255 and the CAN module in a bus-off state.
The STATE_BUSOFF bit is set to "0" when the CAN module in a bus-off state is placed in an error-active state.
The STATE_BUSOFF bit is set to "0" when both RESET0 and RESET1 bits are set to "1" (CAN module reset).

22.1.5 CAN0 Extended ID Register (C0IDR Register)

CAN0 Extended ID Register



Symbol	Address	After Reset(1)
C0IDR	0205_{16} - 0204_{16}	0000_{16}

Bit Symbol	Bit Name	Function	RW
IDE15	Extended ID15 (message slot 15)	Standard or extended format is set by the corresponding message slot 0: Standard format 1: Extended format	RW
IDE14	Extended ID14 (message slot 14)		RW
IDE13	Extended ID13 (message slot 13)		RW
IDE12	Extended ID12 (message slot 12)		RW
IDE11	Extended ID11 (message slot 11)		RW
IDE10	Extended ID10 (message slot 10)		RW
IDE9	Extended ID9 (message slot 9)		RW
IDE8	Extended ID8 (message slot 8)		RW
IDE7	Extended ID7 (message slot 7)		RW
IDE6	Extended ID6 (message slot 6)		RW
IDE5	Extended ID5 (message slot 5)		RW
IDE4	Extended ID4 (message slot 4)		RW
IDE3	Extended ID3 (message slot 3)		RW
IDE2	Extended ID2 (message slot 2)		RW
IDE1	Extended ID1 (message slot 1)		RW
IDE0	Extended ID0 (message slot 0)		RW

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

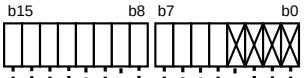
Figure 22.7 C0IDR Register

Bits in the C0IDR register determine the frame format in the message slot corresponding to each bit.
The standard format is selected when the bit is set to "0".
The extended format is selected when the bit is to set "1".

NOTES:
1. Set each bit in the C0IDR register when neither transmit request nor receive request from the message slot is generated.

22.1.6 CAN0 Configuration Register (C0CONR Register)

CAN0 Configuration Register



Symbol	Address	After Reset(1)
C0CONR	0207_{16} - 0206_{16}	0000 0000 0000 XXXX$_2$

Bit Symbol	Bit Name	Function	RW
____ (b3 - b0)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
SAM	Sampling Number	0: Sampled once 1: Sampled three times	RW
PTS0	Propagation Time Segment	b7 b6 b5 0 0 0: PTS = 1Tq 0 0 1: PTS = 2Tq 0 1 0: PTS = 3Tq 0 1 1: PTS = 4Tq 1 0 0: PTS = 5Tq 1 0 1: PTS = 6Tq 1 1 0: PTS = 7Tq 1 1 1: PTS = 8Tq	RW
PTS1			RW
PTS2			RW
PBS10	Phase Buffer Segment 1	b10 b9 b8 0 0 0: Do not set to this value 0 0 1: PBS1 = 2Tq 0 1 0: PBS1 = 3Tq 0 1 1: PBS1 = 4Tq 1 0 0: PBS1 = 5Tq 1 0 1: PBS1 = 6Tq 1 1 0: PBS1 = 7Tq 1 1 1: PBS1 = 8Tq	RW
PBS11			RW
PBS12			RW
PBS20	Phase Buffer Segment 2	b13 b12 b11 0 0 0: Do not set to this value 0 0 1: PBS2 = 2Tq 0 1 0: PBS2 = 3Tq 0 1 1: PBS2 = 4Tq 1 0 0: PBS2 = 5Tq 1 0 1: PBS2 = 6Tq 1 1 0: PBS2 = 7Tq 1 1 1: PBS2 = 8Tq	RW
PBS21			RW
PBS22			RW
SJW0	reSynchronization Jump Width	b15 b14 0 0: SJW = 1Tq 0 1: SJW = 2Tq 1 0: SJW = 3Tq 1 1: SJW = 4Tq	RW
SJW1			RW

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

PTS: Propagation Time Segment, PBS1: Phase Buffer Segment 1, PBS2: Phase Buffer Segment 2,
SJW: reSynchronization Jump Width

Figure 22.8 C0CONR Register

22.1.6.1 SAM Bit

The SAM bit determines the number of sample points to be taken per bit.

When the SAM bit is set to "0", only one sample is taken per bit at the end of the Phase Buffer Segment 1 (PBS1) to determine the value of the bit.

When the SAM bit is set to "1", three samples per bit are taken; one time quantum and two time quanta before the end of PBS1, and at the end of PBS1. The sample result value which is detected more than twice becomes the value of the bit sampled.

22.1.6.2 PTS2 to PTS0 Bits

The PTS2 to PTS0 bits determine PTS width.

22.1.6.3 PBS12 to PBS10 Bits

The PBS12 to PBS10 bits determine PBS1 width. Set the PBS12 to 10 bits to "001_2" or more.

22.1.6.4 PBS22 to PBS20 Bits

The PBS22 to PBS20 bits determine PBS2 width. Set the PBS22 to PBS20 bits to "001_2" or more.

22.1.6.5 SJW1 to SJW0 Bits

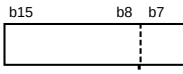
The SJW1 to SJW0 bits determine SJW width. Set the SJW1 to SJW0 bits to a value equal to or less than that of the PBS12 to PBS10 bits and PBS22 to PBS20 bits.

Table 22.3 Bit Timing when CPU Clock = 30 MHz

Baud Rate	BRP	Tq Clock Cycles (ns)	Tq Per Bit	PTS+PBS1	PBS2	Sample Point
1Mbps	1	66.7	15	12	2	87%
	1	66.7	15	11	3	80%
	1	66.7	15	10	4	73%
	2	100	10	7	2	80%
	2	100	10	6	3	70%
	2	100	10	5	4	60%
500Kbps	2	100	20	16	3	85%
	2	100	20	15	4	80%
	2	100	20	14	5	75%
	3	133.3	15	12	2	87%
	3	133.3	15	11	3	80%
	3	133.3	15	10	4	73%
	4	166.7	12	9	2	83%
	4	166.7	12	8	3	75%
	4	166.7	12	7	4	67%
	5	200	10	7	2	80%
	5	200	10	6	3	70%
	5	200	10	5	4	60%

22.1.7 CAN0 Time Stamp Register (C0TSR Register)

CAN0 Time Stamp Register



Symbol	Address	After reset(1)
C0TSR	0209_{16} - 0208_{16}	0000_{16}

Function	RW
Value of Time Stamp	RO

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Figure 22.9 C0TSR Register

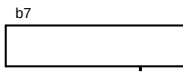
The C0TSR register is a 16-bit counter. The TSPRE0 and TSPRE1 bits in the C0CTLR0 register select the CAN bus bit clock divided by 1, 2, 3 or 4 as the count source for the C0TSR register.
When data transmission or reception is completed, the value of the C0TSR register is automatically stored into the message slot.
The C0TSR register starts a counter increment when the RESET0 and RESET1 bits in the C0CTLR0 register are set to "0".
The C0TSR register is set to "0000_{16}":

- at the next count timing after the C0TSR register is set to "$FFFF_{16}$";
- when the RESET0 and RESET1 bits are set to "1" (CAN module reset) by program, or
- when the TSRESET bit is set to "1" (C0TSR register reset) by program.

In loopback mode, when either data frame receive message slot or remote frame receive message slot is available to store the message, the value of the C0TSR register is also stored into the message slot when data reception is completed. The value of the C0TSR register is not stored when data transmission is completed.

22.1.8 CAN0 Transmit Error Count Register (C0TEC Register)

CAN0 Transmit Error Count Register



Symbol	Address	After Reset(1)
C0TEC	$020A_{16}$	00_{16}

Function	RW
Counter Value of Transmit Errors	RO

NTOES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Figure 22.10 C0TEC Register

In an error active or an error passive state, the count value of a transmission error is stored into the C0TEC register. The counter is decremented when the CAN module has transmitted data as expected or is incremented when an transmit error occurs.
In a bus-off state, an indeterminate value is stored into the C0TEC register. The C0TEC register is set to "00_{16}" when the CAN module is placed in an error active state again.

22.1.9 CAN0 Receive Error Count Register (C0REC Register)

CAN0 Receive Error Count Register

b7 ... b0	Symbol	Address	After Reset(1)
	C0REC	$020B_{16}$	00_{16}

Function	RW
Count Value of Reception Error	RO

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Figure 22.11 C0REC Register

In an error active or an error passive state, a count value of the reception error is stored into the C0REC register. The counter is decremented when the CAN module has received data as expected or is incremented when an error occurs while receiving data.
The C0REC register is set to 127 when the C0REC register is 128 (error passive state) or more and the CAN module has received as expected.
In a bus-off state, an indeterminate value is stored into the C0REC register. The C0REC register is set to "00_{16}" when the CAN module is placed in an error active state again.

22.1.10 CAN0 Baud Rate Prescaler (C0BRP Register)

CAN0 Baud Rate Prescaler

b7 ... b0	Symbol	Address	After reset(1)
	C0BRP	0217_{16}	01_{16}

Function	Setting Range	RW
If setting value is n, the CPU clock is divided by (n+1).	01_{16} to FF_{16}(2)	RW

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
2. Do not set to "00_{16}" (divide-by-1).

Figure 22.12 C0BRP Register

The C0BRP register determines the Tq clock cycle of the CAN bit timing. The baud rate is obtained from Tq clock cycle x Tq per bit.

Tq clock cycle = (BRP+1) / f_1

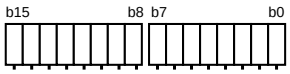
$$\text{Baud rate} = \frac{1}{\text{Tq clock cycle} \times \text{Tq per bit}}$$

Tq per bit = SS + PTS + PBS1 + PBS2

Tq: Time quantum
BRP: Setting value of the C0BRP register; 1-255
SS: Synchronization Segment; 1 Tq
PTS: Propagation Time Segment; 1 to 8 Tq
PBS1: Phase Buffer Segment 1; 2 to 8 Tq
PBS2: Phase Buffer Segment 2; 2 to 8 Tq

22.1.11 CAN0 Slot Interrupt Status Register (C0SISTR Register)

CAN0 Slot Interrupt Status Register



Symbol	Address	After Reset(1)
C0SISTR	020D16 - 020C16	000016

Bit Symbol	Bit Name	Function	RW
SIS15	Message Slot 15 Interrupt Request Status Bit	Determines whether an interrupt of a corresponding message slot is requested or not. 0: No interrupt requested 1: Interrupt requested (Note 2)	RW
SIS14	Message Slot 14 Interrupt Request Status Bit		RW
SIS13	Message Slot 13 Interrupt Request Status Bit		RW
SIS12	Message Slot 12 Interrupt Request Status Bit		RW
SIS11	Message Slot 11 Interrupt Request Status Bit		RW
SIS10	Message Slot 10 Interrupt Request Status Bit		RW
SIS9	Message Slot 9 Interrupt Request Status Bit		RW
SIS8	Message Slot 8 Interrupt Request Status Bit		RW
SIS7	Message Slot 7 Interrupt Request Status Bit		RW
SIS6	Message Slot 6 Interrupt Request Status Bit		RW
SIS5	Message Slot 5 Interrupt Request Status Bit		RW
SIS4	Message Slot 4 Interrupt Request Status Bit		RW
SIS3	Message Slot 3 Interrupt Request Status Bit		RW
SIS2	Message Slot 2 Interrupt Request Status Bit		RW
SIS1	Message Slot 1 Interrupt Request Status Bit		RW
SIS0	Message Slot 0 Interrupt Request Status Bit		RW

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
2. Set to "0" by program. If it is set to "1", the value before setting to "1" remains.

Figure 22.13 C0SISTR Register

When using the CAN interrupt, the C0SISTR register indicates which message slot is requesting an interrupt. The SISi bits (i=0 to 15) are not automatically set to "0" (no interrupt requested) when an interrupt is acknowledged. Set the SISj bits to "0" by program(1).
Refer to **22.3 CAN Interrupt** for details.

22.1.11.1 Message Slot for Transmission

The SISi bit is set to "1" (interrupt requested) when the C0TSR register is stored into the message slot i after data transmission is completed.

22.1.11.2 Message Slot for Reception

The SISi bit is set to "1" when the received message is stored in the message slot i after data reception is completed.

NOTES:

1. Use the MOV instruction, instead of the bit clear instruction, to set the SISi bit to "0". Set bits in the C0SISTR register, which are not being changed to "0", to "1".
   For example: To set the SIS0 bit to "0"
   Assembly language: mov.w #07FFFh, C0SISTR
   C language: c0sistr = 0x7FFF;
2. If the automatic answering function is enabled in the remote frame receive message slot, the SISi bit is set to "1" after the remote frame is received and after the data frame is transmitted.
3. In the remote frame transmit message slot, the SISi bit is set to "1" after the remote frame is transmitted and after the data frame is received.
4. The SISi bit is set to "1" if the SISi bit is set to "1" by an interrupt request and "0" by program simultaneously.

22.1.12 CAN0 Slot Interrupt Mask Register (C0SIMKR Register)

CAN0 Slot Interrupt Mask Register

b15 b8 b7 b0

Symbol	Address	After Reset(1)
C0SIMKR	0211_{16} - 0210_{16}	0000_{16}

Bit Symbol	Bit Name	Function	RW
SIM15	Slot 15 Interrupt Request Mask Bit	Determines whether the interrupt request of the corresponding message slot is enabled or masked. 0: Masks (disables) an interrupt request 1: Enables an interrupt request	RW
SIM14	Slot 14 Interrupt Request Mask Bit		RW
SIM13	Slot 13 Interrupt Request Mask Bit		RW
SIM12	Slot 12 Interrupt Request Mask Bit		RW
SIM11	Slot 11 Interrupt Request Mask Bit		RW
SIM10	Slot 10 Interrupt Request Mask Bit		RW
SIM9	Slot 9 Interrupt Request Mask Bit		RW
SIM8	Slot 8 Interrupt Request Mask Bit		RW
SIM7	Slot 7 Interrupt Request Mask Bit		RW
SIM6	Slot 6 Interrupt Request Mask Bit		RW
SIM5	Slot 5 Interrupt Request Mask Bit		RW
SIM4	Slot 4 Interrupt Request Mask Bit		RW
SIM3	Slot 3 Interrupt Request Mask Bit		RW
SIM2	Slot 2 Interrupt Request Mask Bit		RW
SIM1	Slot 1 Interrupt Request Mask Bit		RW
SIM0	Slot 0 Interrupt Request Mask Bit		RW

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Figure 22.14 C0SIMKR Register

The CiSIMKR register determines whether an interrupt request that is generated by a data transmission or reception in the corresponding message slot is enabled or disabled. When the SIMi bit (i=0 to 15) is set to "1", an interrupt request generated by a data transmission or reception in the corresponding message slot is enabled. Refer to **22.3 CAN Interrupt** for details.

22.1.13 CAN0 Error Interrupt Mask Register (C0EIMKR Register)

CAN0 Error Interrupt Mask Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset(1)
								C0EIMKR	0214_{16}	XXXX X000$_2$

Bit Symbol	Bit Name	Function	RW
BOIM	Bus-off Interrupt Mask Bit	0: Masks (disables) an interrupt request 1: Enables an interrupt request	RW
EPIM	Error-passive Interrupt Mask Bit	0: Masks (disables) an interrupt request 1: Enables an interrupt request	RW
BEIM	CAN bus-error Interrupt Mask Bit	0: Masks (disables) an interrupt request 1: Enables an interrupt request	RW
____ (b7 - b3)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		__

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying the clock to the CAN module after reset.

Figure 22.15 C0EIMKR Register

22.1.13.1 BOIM Bit

The BOIM bit determines whether an interrupt request is enabled or disabled when the CAN module is placed in a bus-off state. When the BOIM bit is set to "1", the bus-off interrupt request is enabled.

22.1.13.2 EPIM Bit

The EPIM bit determines whether an interrupt request is enabled or disabled when the CAN module is placed in an error passive state. When the EPIM bit is set to "1", the error passive interrupt request is enabled.

22.1.13.3 BEIM Bit

The BEIM bit determines whether an interrupt request is enabled or disabled when a CAN bus error occurs. When the BEIM bit is set to "1", the CAN bus error interrupt request is enabled.

Refer to **22.3 CAN Interrupt** for details.

22.1.14 CAN0 Error Interrupt Status Register (C0EISTR Register)

CAN0 Error Interrupt Status Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset(1)
								C0EISTR	0215_{16}	XXXX X000$_2$

Bit Symbol	Bit Name	Function	RW
BOIS	Bus-Off Interrupt Status Bit(2)	0: No interrupt is requested 1: Interrupt is requested	RW
EPIS	Error-Passive Interrupt Status Bit(2)	0: No interrupt is requested 1: Interrupt is requested	RW
BEIS	CAN Bus-Error Interrupt Status Bit(2)	0: No interrupt is requested 1: Interrupt is requested	RW
____ (b7 - b3)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying the clock to the CAN module after reset.
2. Set to "0" by program. If it is set to "1", the value before setting to "1" remains.

Figure 22.16 C0EISTR Register

When using the CAN interrupt, the C0EISTR register indicates the cause of the generated error interrupt. The BOIS, EPIS and BEIS bits are not automatically set to "0" (no interrupt requested) even if an interrupt is acknowledged. Set these bits to "0" by program(1).
Refer to **22.3 CAN Interrupt** for details.

22.1.14.1 BOIS Bit

The BOIS bit is set to "1" when the CAN module is placed in a bus-off state.

22.1.14.2 EPIS Bit

The EPIS bit is set to "1" when the CAN module is placed in an error passive state.

22.1.14.3 BEIS Bit

The BEIS bit is set to "1" when a CAN bus error is detected.

NOTES:
1. Use the MOV instruction, instead of the bit clear instruction, to set each bit in the CoEISTR register to "0". Bits not being changed to "0" must be set to "1".
   For example: To set the BOIS bit to "0"
   Assembly language: mov.b#006h, C0EISTR
   C language: c0eistr = 0x06;

22.1.15 CAN0 Global Mask Register, CAN0 Local Mask Register A and CAN0 Local Mask Register B (C0GMRj (j=0 to4), C0LMARj and C0LMBRj Registers)

The C0GMRj, C0LMARj and C0LMBRj registers are used for acceptance filtering.

The C0GMRj register determines whether the IDs in the message slots 0 to 13 are verified. The C0LMARj register determines whether the ID in the message slot 14 is verified. The C0LMBRj register determines whether the ID in the message slot 15 is verified.

- When bits in these registers are set to "0", each ID bit, standard ID 0 to 1 bit and extended ID0 to 2 bit in the CAN0 message slots i (i=0 to 15) corresponding to the bits in the above registers, is masked while acceptance filtering. (The corresponding bits are assumed to have matching IDs.)
- When bits in these registers are set to "1", corresponding ID bits are compared with received IDs while acceptance filtering. If the received ID matches the ID in the message slot i, the received data having the matching ID is stored into that message slot.

NOTES:

1. Change the C0GMRj register only when the message slots 0 to 13 have no receive request.
2. Change the C0LMARj register only when the message slot 14 has no receive request.
3. Change the C0LMBRj register only when the message slot 15 has no receive request.

CAN0 Global Mask Register Standard ID0(1)
CAN0 Local Mask Register A Standard ID0(1)
CAN0 Local Mask Register B Standard ID0(1)

Symbol	Address	After Reset(2)
C0GMR0	0228_{16}	$XXX0\ 0000_2$
C0LMAR0	0230_{16}(3)	$XXX0\ 0000_2$
C0LMBR0	0238_{16}(4)	$XXX0\ 0000_2$

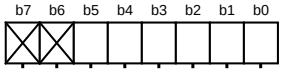
Bit Symbol	Bit Name	Function	RW
SID6M	Standard ID6	0: No ID is checked 1: ID is checked	RW
SID7M	Standard ID7		RW
SID8M	Standard ID8		RW
SID9M	Standard ID9		RW
SID10M	Standard ID10		RW
____ (b7 - b5)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:

1. This register can be accessed when the BANKSEL bit in the C0CTLR1 register is set to "1".
2. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
3. The C0LMAR0 register shares the same address with the C0MCTL0 register.
4. The C0LMBR0 register shares the same address with the C0MCTL8 register.

Figure 22.17 C0GMR0, C0LMAR0 and C0LMBR0 Registers

CAN0 Global Mask Register Standard ID1(1)
CAN0 Local Mask Register A Standard ID1(1)
CAN0 Local Mask Register B Standard ID1(1)

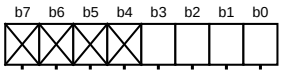


Symbol	Address	After Reset(2)
C0GMR1	022916	XX00 0000$_2$
C0LMAR1	023116(3)	XX00 0000$_2$
C0LMBR1	023916(4)	XX00 0000$_2$

Bit Symbol	Bit Name	Function	RW
SID0M	Standard ID0	0: No ID is checked 1: ID is checked	RW
SID1M	Standard ID1		RW
SID2M	Standard ID2		RW
SID3M	Standard ID3		RW
SID4M	Standard ID4		RW
SID5M	Standard ID5		RW
—— (b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. This register can be accessed when the BANKSEL bit in the C0CTLR1 register is set to "1".
2. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
3. The C0LMAR1 register shares the same address with the C0MCTL1 register.
4. The C0LMBR1 register shares the same address with the C0MCTL9 register.

CAN0 Global Mask Register Extended ID0(1)
CAN0 Local Mask Register A Extended ID0(1)
CAN0 Local Mask Register B Extended ID0(1)



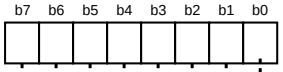
Symbol	Address	After Reset(2)
C0GMR2	$022A16$	XXXX 0000$_2$
C0LMAR2	023216(3)	XXXX 0000$_2$
C0LMBR2	$023A16$(4)	XXXX 0000$_2$

Bit Symbol	Bit Name	Function	RW
EID14M	Extended ID14	0: No ID is checked 1: ID is checked	RW
EID15M	Extended ID15		RW
EID16M	Extended ID16		RW
EID17M	Extended ID17		RW
—— (b7 - 4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. This register can be accessed when the BANKSEL bit in the C0CTLR1 register is set to "1".
2. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
3. The C0LMAR2 register shares the same address with the C0MCTL2 register.
4. The C0LMBR2 register shares the same address with the C0MCTL10 register.

Figure 22.18 C0GMR1, C0LMAR1 and C0LMBR1 Registers and C0GMR2, C0LMAR2 and C0LMBR2 Registers

CAN0 Global Mask Register Extended ID1(1)
CAN0 Local Mask Register A Extended ID1(1)
CAN0 Local Mask Register B Extended ID1(1)

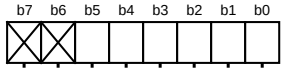


Symbol	Address	After Reset(2)
C0GMR3	$022B_{16}$	00_{16}
C0LMAR3	0233_{16}(3)	00_{16}
C0LMBR3	$023B_{16}$(4)	00_{16}

Bit Symbol	Bit Name	Function	RW
EID6M	Extended ID6	0: No ID is checked 1: ID is checked	RW
EID7M	Extended ID7		RW
EID8M	Extended ID8		RW
EID9M	Extended ID9		RW
EID10M	Extended ID10		RW
EID11M	Extended ID11		RW
EID12M	Extended ID12		RW
EID13M	Extended ID13		RW

NOTES:
1. This register can be accessed when the BANKSEL bit in the C0CTLR1 register is set to "1".
2. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
3. The C0LMAR3 register shares the same address with the C0MCTL3 register.
4. The C0LMBR3 register shares the same address with the C0MCTL11 register.

CAN0 Global Mask Register Extended ID2(1)
CAN0 Local Mask Register A Extended ID2(1)
CAN0 Local Mask Register B Extended ID2(1)



Symbol	Address	After Reset(2)
C0GMR4	$022C_{16}$	$XX00\ 0000_2$
C0LMAR4	0234_{16}(3)	$XX00\ 0000_2$
C0LMBR4	$023C_{16}$(4)	$XX00\ 0000_2$

Bit Symbol	Bit Name	Function	RW
EID0M	Extended ID0	0: No ID is checked 1: ID is checked	RW
EID1M	Extended ID1		RW
EID2M	Extended ID2		RW
EID3M	Extended ID3		RW
EID4M	Extended ID4		RW
EID5M	Extended ID5		RW
____ (b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. This register can be accessed when the BANKSEL bit in the C0CTLR1 register is set to "1".
2. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
3. The C0LMAR4 register shares the same address with the C0MCTL4 register.
4. The C0LMBR4 register shares the same address with the C0MCTL12 register.

Figure 22.19 C0GMR3, C0LMAR3 and C0LMBR3 Registers and C0GMR4, C0LMAR4 and C0LMBR4 Registers

22.1.16 CAN0 Message Slot i Control Register (C0MCTLi Register) (i=0 to 15)

CAN0 Message Slot i Control Register (i=0 to 15)(1)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset (2)
C0MCTL0 to C0MCTL3	0230_{16}(3), 0231_{16}(3), 0232_{16}(3), 0233_{16}(3)	$0000\ 0000_2$
C0MCTL4 to C0MCTL7	0234_{16}(3), 0235_{16}, 0236_{16}, 0237_{16}	$0000\ 0000_2$
C0MCTL8 to C0MCTL11	0238_{16}(3), 0239_{16}(3), $023A_{16}$(3), $023B_{16}$(3)	$0000\ 0000_2$
C0MCTL12 to C0MCTL15	$023C_{16}$(3), $023D_{16}$, $023E_{16}$, $023F_{16}$	$0000\ 0000_2$

Bit Symbol	Bit Name	Function	RW
When receive, NEWDATA When transmit, SENTDATA	Receive Complete Flag Transmit Complete Flag	When transmitting 0: Not transmitted(4) 1: Transmit complete When receiving 0: Not received(4) 1: Receive complete	RW
When receive, INVALDATA When transmit, TRMACTIVE	Receiving Flag Transmitting Flag	When transmitting 0: Stops transmitting 1: Transmits When receiving 0: Stops receiving 1: Stores received data	RO
MSGLOST	Overwrite Flag	0: No overrun error occurs 1: Overrun error occurs (Note 4)	RW
REMACTIVE	Remote Frame Transmit/Receive Status Flag	In modes other than BasicCan mode 0: Data frame 1: Remote frame In BasicCan mode 0: Receives the data frame (status) 1: Receives the remote frame (status)	RO
RSPLOCK	Automatic Answering Disable Mode Select Bit	0: Enables automatic answering of the remote frame 1: Disables automatic answering of the remote frame	RW
REMOTE	Remote Frame Set Bit	0: Transmits/receives the data frame 1: Transmits/receives the remote frame	RW
RECREQ	Receive Request Bit	0: No request to receive the frame 1: Request to receive data	RW
TRMREQ	Transmit Request Bit	0: No request to transmit the frame 1: Request to transmit data	RW

NOTES:
1. This register can be accessed when the BANKSEL bit in the C0CTLR1 register is set to "1".
2. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
3. The C0MCTL0 to C0MCTL4 registers each share addresses with the C0MAR0 to C0MAR4 registers.
4. Each bit can be set to "0" by program. If it is set to "1", the value before setting to "1" remains.

Figure 22.20 C0MCTL0 to C0MCTL15 Registers

Table 22.4 C0MCTLi Register (i= 0 to 15) Settings and Transmit/Receive Mode

Settings for the C0MCTLi Register								Transmit/Receive Mode
TRMREQ	RECREQ	REMOTE	RSPLOCK	REMACTIVE	MSGLOST	TRMACTIVE INVALDATA	SENTDATA NEWDATA	
0	0	0	0	0	0	0	0	No frame is transmitted or received
0	1	0	0	0	0	0	0	Data frame is received
0	1	1	1 or 0	0	0	0	0	Remote frame is received (The data frame is transmitted after receiving the remote frame.)
1	0	0	0	0	0	0	0	Data frame is transmitted
1	0	1	0	0	0	0	0	Remote frame is transmitted (The data frame is received after transmitting the remote frame)

22.1.16.1 SENTDATA/NEWDATA Bit

The SENTDATA/NEWDATA bit indicates that the CAN module has transmitted or received the CAN message. Set the SENTDATA/NEWDATA bit to "0 " (not transmitted or not received) by program before data transmission and reception is started. The SENTDATA/NEWDATA bit is not set to "0" automatically. When the TRMACTIVE/INVALDATA bit is set to "1" (during transmission or storing received data), the SENTDATA/NEWDATA bit cannot be set to "0".

SENTDATA : The SENTDATA bit is set to "1" (transmit complete) when a data transmission is completed in the transmit message slot.

NEWDATA : The NEWDATA bit is set to "1" (receive complete) when the message to be stored into the message slot i (i=0 to 15) is received in the receive message slot as expected.

NOTES:

1. To read a received data from the message slot i, set the NEWDATA bit to "0" before reading. If the NEWDATA bit is set to "1" immediately after reading, this indicates that new received data has been stored into the message slot while reading and the data read contains an indeterminate value. In this case, discard the data with indeterminate value and then read the message slot again after the NEWDATA bit is set to "0".
2. When the remote frame is transmitted or received, the SENTDATA/NEWDATA bit remains unchanged after the remote frame transmission or reception is completed. The SENTDATA/NEWDATA bit is set to "1" when a subsequent data frame transmission or reception is completed.

22.1.16.2 TRMACTIVE/INVALDATA Bit

The TRMACTIVE/INVALDATA bit indicates that the CAN module is transmitting or receiving a message and accessing the message slot i. The TRMACTIVE/INVALDATA bit is set to "1" when the CAN module is accessing the message slot and to "0 " when not accessing the message slot.

TRMACTIVE : The TRMACTIVE bit is set to "1" (transmitting) when a data transmission is started in the message slot. The TRMACTIVE bit is set to "0" (stops transmitting) if the CAN module loses in bus arbitration and a CAN bus error occurs or when a data transmission is completed.

INVALDATA : The INVALDATA bit is set to "1" (storing received data) when receiving a message and storing a received data into the message slot i. Data, if read from the message slot i while this bit is set to "1", is indeterminate.

22.1.16.3 MSGLOST Bit

The MSGLOST bit is valid only when the message slot is set for reception. The MSGLOST bit is set to "1" (overrun error occurred) when the message slot i is overwritten by a new received message while the NEWDATA bit set to "1" (already received).

The MSGLOST bit is not automatically set to "0". Set to "0" (no overrun error occurred) by program.

22.1.16.4 REMACTIVE Bit

The C0MCTL0 to C0MCTL15 registers all have the same function when the STATE_BASICCAN bit is set to "0" (other than BasicCAN mode).

The REMACTIVE bit is set to "1" (remote frame) when the message slot i is set to transmit or receive the remote frame. The REMACTIVE bit is set to "0" (data frame) after the remote frame has been transmitted or received.

The functions of the C0MCTL14 and C0MCTL15 registers change when the STATE_BASICCAN bit is set to "1" (BasicCAN mode). When the REMACTIVE bit is set to "0", this indicates that a message stored into the message slot is the data frame. When the REMACTIVE bit is set to "1", this indicates a message stored into the message slot is the remote frame.

22.1.16.5 RSPLOCK Bit

The RSPLOCK bit is valid only when remote frame reception shown in Table 22.4 is selected. The RSPLOCK bit determines whether the received remote frame is processed or not.

When the RSPLOCK bit is set to "0" (automatic answering of the remote frame enabled), the slot automatically changes to a transmit slot after the remote frame is received, and the message stored into the message slot is automatically transmitted as the data frame.

When the RSPLOCK bit is set to "1" (automatic answering of the remote frame disabled), message is not automatically transmitted upon receiving the remote frame.

Set the RSPLOCK bit to "0" to select any transmit/receive mode other than the remote frame reception.

22.1.16.6 REMOTE Bit

The REMOTE bit selects transmit/receive mode shown in Table 22.4. Set the REMOTE bit to "0" to transmit or receive data frame. Set to "1" to transmit or receive remote frame.

The followings occur during remote frame transmission or reception.

- Transmitting the remote frame

  A message stored into the message slot i (i=0 to 15) is transmitted as the remote frame. After transmission, the slot automatically becomes ready to receive data frame.

  If the data frame is received before the remote frame is transmitted, the data frame is stored into the message slot i. The remote frame is not transmitted.

- Receiving the remote frame

  The message slot receives the remote frame. The RSPLOCK bit determines whether or not to process the received remote frame.

22.1.16.7 RECREQ Bit

The RECREQ bit selects transmit/receive mode shown in Table 22.4. Set the RECREQ bit to "1" (receive requested) when data frame or remote frame is received. Set the RECREQ bit to "0" (no receive requested) when data frame or remote frame is transmitted.

When a data frame is automatically transmitted after a remote frame is received, the RECREQ bit remains set to "1". Set the RECREQ bit to "0" to transmit a remote frame. After a remote frame is transmitted, a data frame is automatically received while the RECREQ bit remains set to "0".

When setting the TRMREQ bit to "1" (transmit requested), do not set the RECREQ bit to "1" (receive requested).

22.1.16.8 TRMREQ Bit

The TRMREQ bit selects transmit/receive mode shown in Table 22.4. Set the TRMREQ bit to "1" (transmit requested) when data frame or remote frame is transmitted.

Set the TRMREQ bit to "0" (no request to transmit the frame) when data frame or remote frame is received.

When the data frame is automatically received after the remote frame is transmitted, the TRMREQ bit remains set to "1". Set the TRMREQ bit to "0" to receive the remote frame. After the remote frame is received, data frame is automatically transmitted while the TRMREQ bit remains set to "0".

If the RECREQ bit is set to "1" (request to receive the frame), do not set the TRMREQ bit to "1" (request to transmit the frame).

22.1.17 CAN0 Slot Buffer Select Register (C0SBS Register)

CAN0 Slot Buffer Select Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset(2)
								C0SBS	0240₁₆	00₁₆

Bit Symbol	Bit Name	Function	RW
SBS00	CAN0 Message Slot Buffer 0 Number Select Bit	b3 b2 b1 b0 0 0 0 0 : Message slot 0 0 0 0 1 : Message slot 1 0 0 1 0 : Message slot 2 0 0 1 1 : Message slot 3 (Note 1) 1 1 0 0 : Message slot 12 1 1 0 1 : Message slot 13 1 1 1 0 : Message slot 14 1 1 1 1 : Message slot 15	RW
SBS01			RW
SBS02			RW
SBS03			RW
SBS10	CAN0 Message Slot Buffer 1 Number Select Bit	b3 b2 b1 b0 0 0 0 0 : Message slot 0 0 0 0 1 : Message slot 1 0 0 1 0 : Message slot 2 0 0 1 1 : Message slot 3 (Note 1) 1 1 0 0 : Message slot 12 1 1 0 1 : Message slot 13 1 1 1 0 : Message slot 14 1 1 1 1 : Message slot 15	RW
SBS11			RW
SBS12			RW
SBS13			RW

NOTES:
1. 16 CAN0 message slots provided. Each message slot can be selected as a transmit or a receive slot.
2. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Figure 22.21 C0SBS Register

22.1.17.1 SBS03 to SBS00 Bits

If the SBS03 to SBS00 bits select a number i (i=0 to 15), the message slot i is allocated to the CAN0 message slot buffer 0. The message slot i can be accessed via addresses 01E0₁₆ to 01EF₁₆.

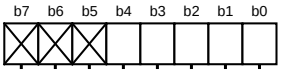
22.1.17.2 SBS13 to SBS10 Bits

If the SBS13 to SBS10 bits select a number i, the message slot i is allocated to the CAN0 message slot buffer 1. The message slot i can be accessed via addresses 01F0₁₆ to 01FF₁₆.

22.1.18 Message Slot Buffer

The message slot, selected by setting the C0SBS register, is read by reading the message slot buffer. A message can be written in the message slot selected by the C0SBS register if the message is written to the message slot buffer.

CAN0 Message Slot Buffer i Standard ID0 (i=0,1)(1)

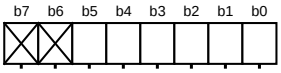


Symbol	Address	After Reset
C0SLOT0_0, C0SLOT1_0	$01E0_{16}$, $01F0_{16}$	Indeterminate

Bit Symbol	Bit Name	Function	RW
SID6	Standard ID6	Read or write the standard ID6 in the message slot j (j=0 to 15)	RW
SID7	Standard ID7	Read or write the standard ID7 in the message slot j	RW
SID8	Standard ID8	Read or write the standard ID8 in the message slot j	RW
SID9	Standard ID9	Read or write the standard ID9 in the message slot j	RW
SID10	Standard ID10	Read or write the standard ID10 in the message slot j	RW
____ (b7 - b5)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

NOTES:
1. Select, by setting the C0SBS register, the message slot j to be accessed by the C0SLOTi_0 register.

CAN0 Message Slot Buffer i Standard ID1 (i=0,1)(1)



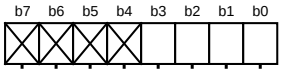
Symbol	Address	After Reset
C0SLOT0_1, C0SLOT1_1	$01E1_{16}$, $01F1_{16}$	Indeterminate

Bit Symbol	Bit Name	Function	RW
SID0	Standard ID0	Read or write the standard ID0 in the message slot j (j=0 to 15)	RW
SID1	Standard ID1	Read or write the standard ID1 in the message slot j	RW
SID2	Standard ID2	Read or write the standard ID2 in the message slot j	RW
SID3	Standard ID3	Read or write the standard ID3 in the message slot j	RW
SID4	Standard ID4	Read or write the standard ID4 in the message slot j	RW
SID5	Standard ID5	Read or write the standard ID5 in the message slot j	RW
____ (b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

NOTES:
1. Select, by setting the C0SBS register, the message slot j to be accessed by the C0SLOTi_0 register.

Figure 22.22 C0SLOT0_0, C0SLOT1_0 Registers and C0SLOT0_1, C0SLOT1_1 Registers

CAN0 Message Slot Buffer i Extended ID0 (i=0,1)(1, 2)

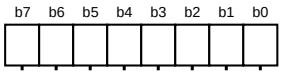


Symbol	Address	After Reset
C0SLOT0_2, C0SLOT1_2	01E2$_{16}$, 01F2$_{16}$	Indeterminate

Bit Symbol	Bit Name	Function	RW
EID14	Extended ID14	Read or write the extended ID14 in the message slot j (j=0 to 15)	RW
EID15	Extended ID15	Read or write the extended ID15 in the message slot j	RW
EID16	Extended ID16	Read or write the extended ID16 in the message slot j	RW
EID17	Extended ID17	Read or write the extended ID17 in the message slot j	RW
____ (b7 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

NOTES:
1. If the receive slot is standard ID formatted, the EID bits are indeterminate when the received data is stored.
2. Select, by setting the C0SBS register, the message slot j to be accessed by the C0SLOTi_2 register.

CAN0 Message Slot Buffer i Extended ID1 (i=0,1)(1, 2)



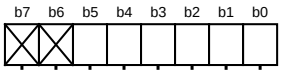
Symbol	Address	After Reset
C0SLOT0_3, C0SLOT1_3	01E3$_{16}$, 01F3$_{16}$	Indeterminate

Bit Symbol	Bit Name	Function	RW
EID6	Extended ID6	Read or write the extended ID6 in the message slot j (j=0 to 15)	RW
EID7	Extended ID7	Read or write the extended ID 7 in the message slot j	RW
EID8	Extended ID8	Read or write the extended ID 8 in the message slot j	RW
EID9	Extended ID9	Read or write the extended ID 9 in the message slot j	RW
EID10	Extended ID10	Read or write the extended ID 10 in the message slot j	RW
EID11	Extended ID11	Read or write the extended ID 11 in the message slot j	RW
EID12	Extended ID12	Read or write the extended ID 12 in the message slot j	RW
EID13	Extended ID13	Read or write the extended ID 13 in the message slot j	RW

NOTES:
1. If the receive slot is standard ID formatted, the EID bits are indeterminate when the received data is stored.
2. Select, by setting the C0SBS register the message slot j to be accessed by the C0SLOTi_3 register.

Figure 22.23 C0SLOT0_2, C0SLOT1_2 Registers and C0SLOT0_3, C0SLOT1_3 Registers

CAN0 Message Slot Buffer i Extended ID2 (i=0,1)(1, 2)

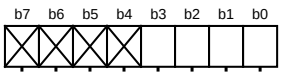


Symbol	Address	After Reset
C0SLOT0_4, C0SLOT1_4	01E4$_{16}$, 01F4$_{16}$	Indeterminate

Bit Symbol	Bit Name	Function	RW
EID0	Extended ID0	Read or write the extended ID0 in the message slot j (j=0 to 15)	RW
EID1	Extended ID1	Read or write the extended ID1 in the message slot j	RW
EID2	Extended ID2	Read or write the extended ID2 in the message slot j	RW
EID3	Extended ID3	Read or write the extended ID3 in the message slot j	RW
EID4	Extended ID4	Read or write the extended ID4 in the message slot j	RW
EID5	Extended ID5	Read or write the extended ID5 in the message slot j	RW
____ (b7 - b6)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

NOTES:
1. If the receive slot is standard ID formatted, the EID bits are indeterminate when received data is stored.
2. Select, by setting the C0SBS register, the message slot j to be accessed by the C0SLOTi_4 register.

CAN0 Message Slot Buffer i Data Length Code (i=0,1)(1)



Symbol	Address	After Reset
C0SLOT0_5, C0SLOT1_5	01E5$_{16}$, 01F5$_{16}$	Indeterminate

Bit Symbol	Bit Name	Function	RW
DLC0	Data Length Set Bit	Read or write the data length set bit in the message slot j (j=0 to 15)	RW
DLC1			RW
DLC2			RW
DLC3			RW
____ (b7 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		_

NOTES:
1. Select, by setting the C0SBS register, the message slot j to be accessed by the C0SLOTi_5 register.

Figure 22.24 C0SLOT0_4, C0SLOT1_4 Registers and C0SLOT0_5 and C0SLOT1_5 Registers

CAN0 Message Slot Buffer i Data k (i=0,1 k=0 to 7)(1)

b7 b0

Symbol	Address	After Reset
C0SLOT0_q(q=k+6,k=0 to 3)	$01E6_{16}$, $01E7_{16}$, $01E8_{16}$, $01E9_{16}$	Indeterminate
C0SLOT0_q(q=k+6,k=4 to 7)	$01EA_{16}$, $01EB_{16}$, $01EC_{16}$, $01ED_{16}$	Indeterminate
C0SLOT1_q(q=k+6,k=0 to 3)	$01F6_{16}$, $01F7_{16}$, $01F8_{16}$, $01F9_{16}$	Indeterminate
C0SLOT1_q(q=k+6,k=4 to 7)	$01FA_{16}$, $01FB_{16}$, $01FC_{16}$, $01FD_{16}$	Indeterminate

Function	Setting Range	RW
Read or write data k in the message slot j (j=0 to 15)	00_{16} to FF_{16}	RW

NOTES:
1. Select, by setting the C0SBS register, the data k in the message slot j to be accessed by the C0SLOTi_q register.

CAN0 Message Slot Buffer i Time Stamp High-Ordered (i=0,1)(1)

b7 b0

Symbol	Address	After Reset
C0SLOT0_14, C0SLOT1_14	$01EE_{16}$, $01FE_{16}$	Indeterminate

Function	Setting Range	RW
Read or write the time stamp high-ordered in the message slot j (j=0 to 15)	00_{16} to FF_{16}	RW

NOTES:
1. Select, by setting the COSBS register, the time stamp high-ordered in the message slot j to be accessed by the C0SLOTi_14 register.

CAN0 Message Slot Buffer i Time Stamp Low-Ordered (i=0,1)(1)

b7 b0

Symbol	Address	After Reset
C0SLOT0_15, C0SLOT1_15	$01EF_{16}$, $01FF_{16}$	Indeterminate

Function	Setting Range	RW
Read or write the time stamp low-ordered in the message slot j (j=0 to 15)	00_{16} to FF_{16}	RW

NOTES:
1. Select, by setting the COSBS register, the time stamp low-ordered in the message slot j to be accessed by the C0SLOTi_15 register.

Figure 22.25 C0SLOT0_6 to C0SLOT0_13, C0SLOT1_6 to C0SLOT1_13, C0SLOT0_14, C0SLOT1_14, C0SLOT0_15 and C0SLOT1_15 Registers

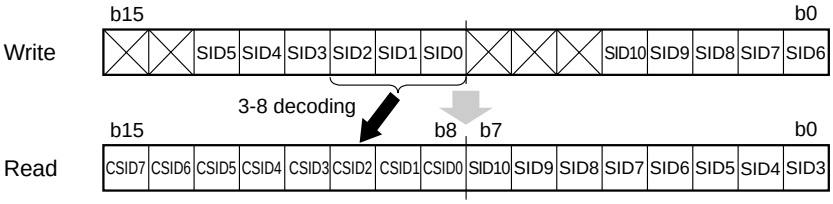
22.1.19 CAN0 Acceptance Filter Support Register (C0AFS Register)

CAN0 Acceptance Filter Support Register

Symbol	Address	After Reset(1)
C0AFS	0245_{16} - 0244_{16}	0100_{16}

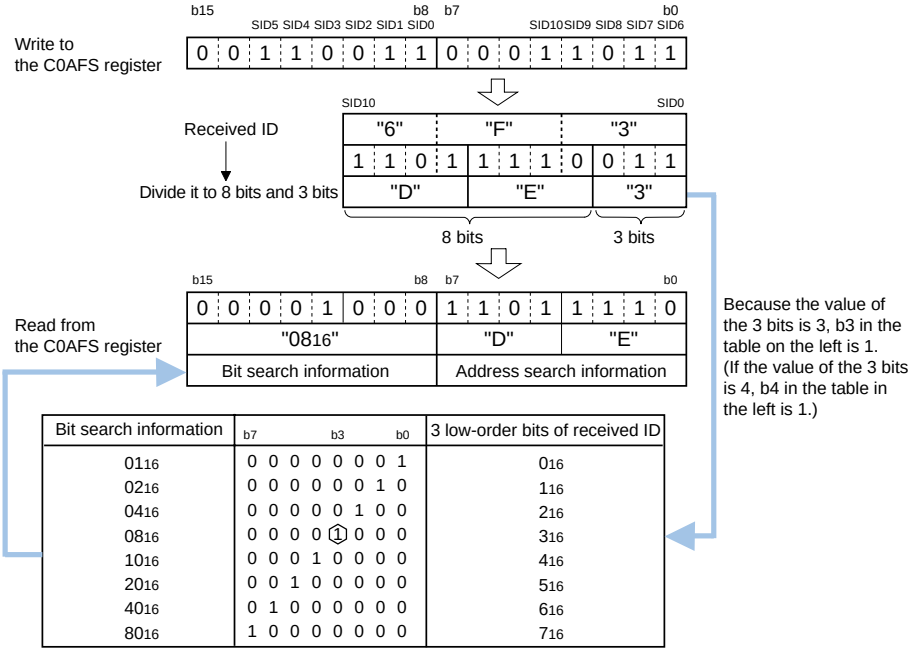
Function	Setting Range	RW
Generates data to determine a received ID	0000_{16} to $FFFF_{16}$	RW

NOTES:
1. Value is obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying the clock to the CAN module after reset.



Data used to search a data table is generated from a received ID in standard format. The table search with this data determines whether or not a received ID is valid.

	b7	b6	b5	b4	b3	b2	b1	b0
Top+00_{16}	007_{16} "0"	006_{16} "0"	005_{16} "0"	004_{16} "0"	003_{16} "0"	002_{16} "0"	001_{16} "1"	000_{16} "0"
Top+01_{16}	$00F_{16}$ "1"	$00E_{16}$ "0"	$00D_{16}$ "0"	$00C_{16}$ "0"	$00B_{16}$ "0"	$00A_{16}$ "0"	009_{16} "0"	008_{16} "0"
	≈							≈
Top+DE_{16}	$6F7_{16}$ "0"	$6F6_{16}$ "0"	$6F5_{16}$ "0"	$6F4_{16}$ "0"	$6F3_{16}$ "1"	$6F2_{16}$ "0"	$6F1_{16}$ "0"	$6F0_{16}$ "0"
	≈							≈
Top+FE_{16}	$7F7_{16}$ "0"	$7F6_{16}$ "0"	$7F5_{16}$ "0"	$7F4_{16}$ "0"	$7F3_{16}$ "0"	$7F2_{16}$ "0"	$7F1_{16}$ "0"	$7F0_{16}$ "1"
Top+FF_{16}	$7FF_{16}$ "0"	$7FE_{16}$ "0"	$7FD_{16}$ "1"	$7FC_{16}$ "0"	$7FB_{16}$ "0"	$7FA_{16}$ "0"	$7F9_{16}$ "0"	$7F8_{16}$ "0"
	Address search information		Bit search information					



Bit search information	b7 b3 b0	3 low-order bits of received ID
01_{16}	0 0 0 0 0 0 0 1	0_{16}
02_{16}	0 0 0 0 0 0 1 0	1_{16}
04_{16}	0 0 0 0 0 1 0 0	2_{16}
08_{16}	0 0 0 0 ① 0 0 0	3_{16}
10_{16}	0 0 0 1 0 0 0 0	4_{16}
20_{16}	0 0 1 0 0 0 0 0	5_{16}
40_{16}	0 1 0 0 0 0 0 0	6_{16}
80_{16}	1 0 0 0 0 0 0 0	7_{16}

Figure 22.26 C0AFS Register

The C0AFS register enables prompt performance of the table search to determine the validity of a received ID. This function is for standard-formatted ID only.

22.2 Timing with CAN-Associated Registers

22.2.1 CAN Module Reset Timing

Figure 22.27 shows an operation example of when the CAN module is reset.

(1) The CAN module can be reset when the STATE_RESET bit in the C0STR register is set to "1" (CAN module reset completed) after the RESET0 and RESET1 bits in the C0CTLR0 register are set to "1" (CAN module reset).

(2) Set necessary CAN-associated registers.

(3) CAN communication can be established after the STATE_RESET bit is set to "0" (resetting) after the RESET0 and RESET1 bits are set to "0" (CAN module reset exited) .

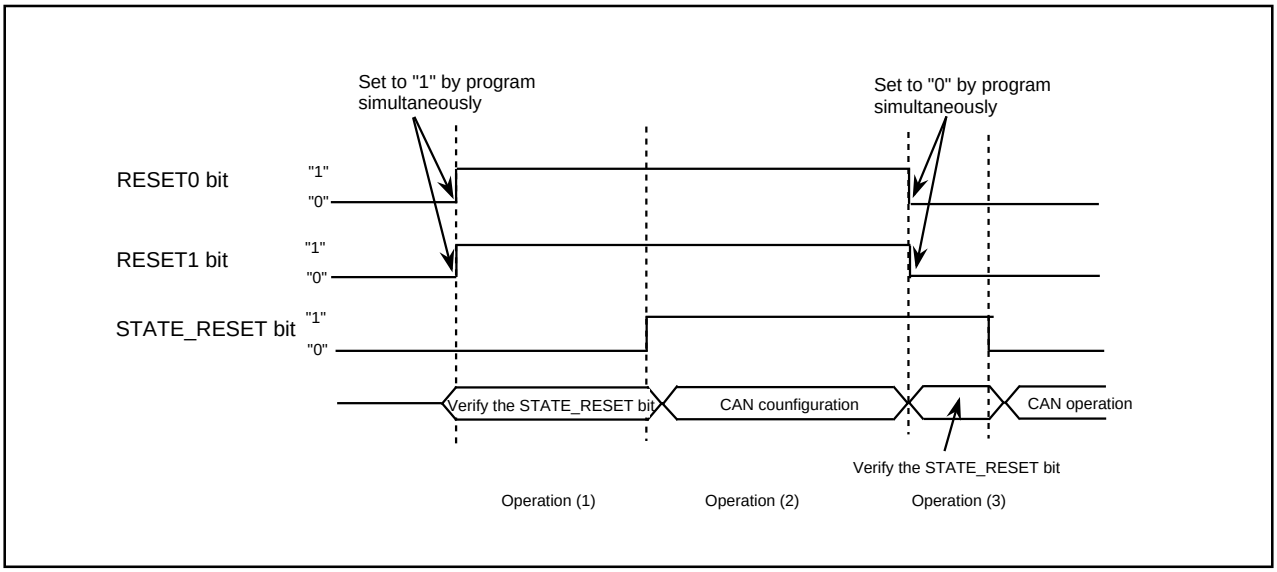


Figure 22.27 Example of CAN Module Reset Operation

22.2.2 CAN Transmit Timing

Figure 22.28 shows an operation example of when the CAN transmits a frame.

(1) When the TRMREQ bit is set to "1" (request to transmit the data frame) while the CAN bus is idle, the TRMACTIVE bit in the C0MCTLi register (i=0 to 15) is set to "1" (during transmission) and the TRMSTATE bit in the C0STR register is set to "1" (during transmission). The CAN starts transmitting the frame.

(2) After a CAN frame transmission is completed, the SENTDATA bit in the C0MCTLi register is set to "1" (already transmitted), the TRMSUCC bit in the C0STR register to "1" (transmission completed) and the SISi bit in the C0SISTR register to "1" (interrupt requested). The MBOX3 to MBOX0 bits in the C0STR register store transmitted message slot numbers.

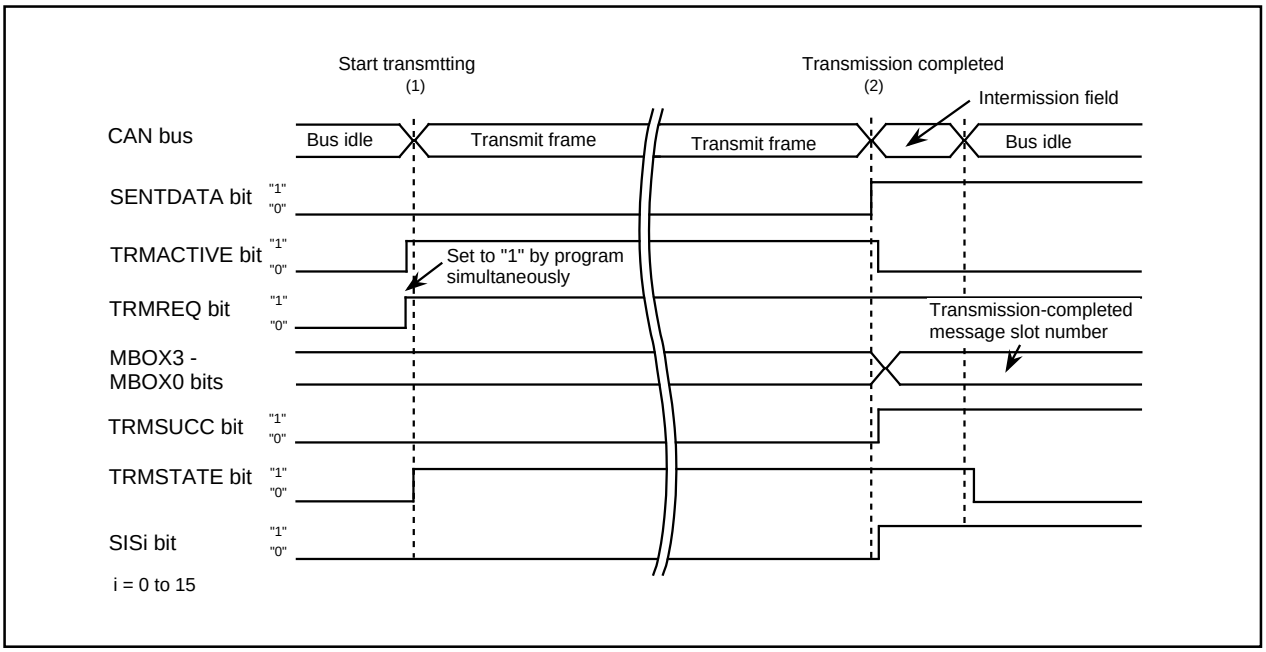


Figure 22.28 Example of CAN Data Frame Transmission Operation

22.2.3 CAN Receive Timing

Figure 22.29 shows an operation example of when the CAN receives a frame.

(1) When the RECREQ bit in the C0MCTLi register (i=0 to 15) is set to "1" (receive requested), the CAN is ready to receive the frame at anytime.

(2) When the CAN starts receiving the frame, the RECSTATE bit in the C0STR register is set to "1" (during reception).

(3) After the CAN frame reception is completed, the INVALDTA bit in the C0MCTLi register is set to "1" (storing received data), the NEWDATA bit in the C0MCTLi register is set to "1" (receive complete) and the RECSUCC bit in the C0STR register is set to "1" (reception completed).

(4) After data is written to the message slot, the INVALDATA bit is set to "0" (stops receiving) and the SISi bit is set to "1" (interrupt requested). The MBOX3 to MBOX0 bits store received message slot numbers.

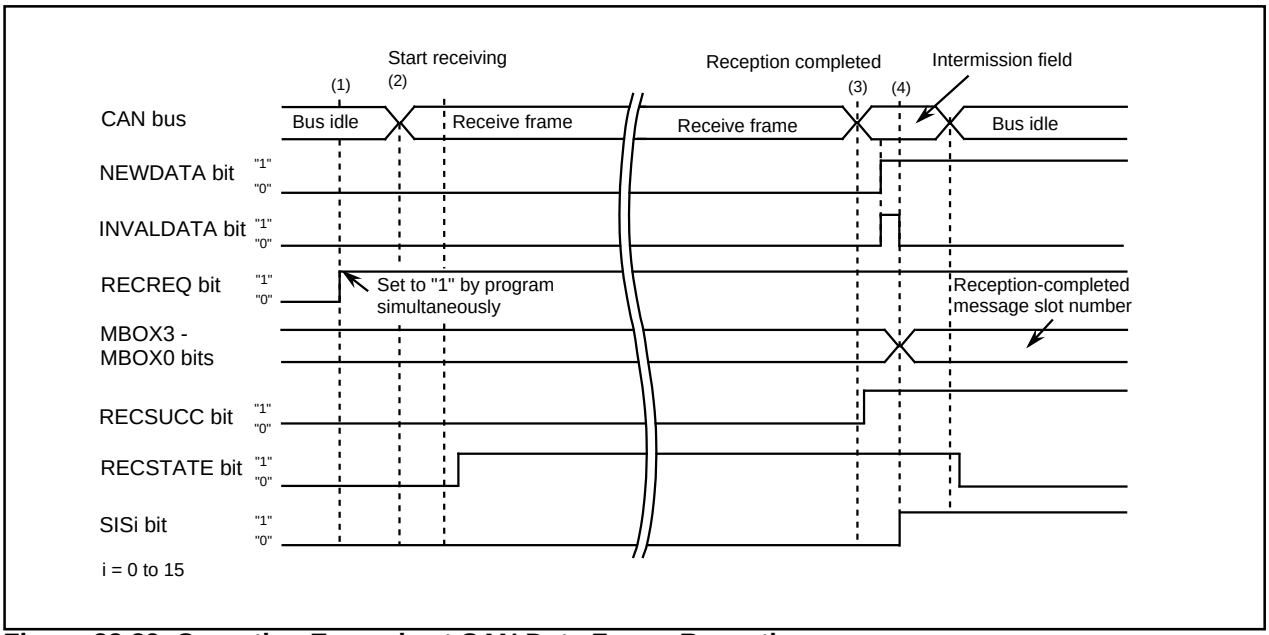


Figure 22.29 Operation Example at CAN Data Frame Reception

22.2.4 CAN Bus Error Timing

Figure 22.30 shows an operation example of when a CAN bus error occurs.

(1) When a CAN bus error is detected, the STATE_BUSERROR bit in the CiSTR register is set to "1", (error occurred) and the BEIS bit in the CiEISTR register is set to "1" (interrupt requested). The CAN starts transmitting the error frame.

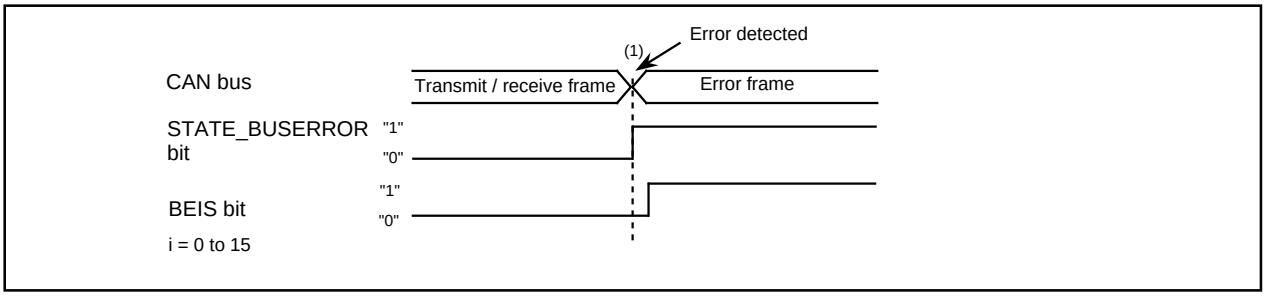


Figure 22.30 Operation Timing when a CAN Bus Error Occurs

22.3 CAN Interrupts

The CANj interrupt (j=0 to 2) is provided as the CAN interrupt. Figure 22.31 shows a block diagram of the CAN interrupt.

The following factors cause the CAN-associated interrupt request to be generated.

- The CAN0 slot i (i=0 to 15) completes a transmission
- The CAN0 slot i completes a reception
- The CAN0 module detects a bus error
- The CAN0 module moves into an error-passive state
- The CAN0 module moves into a bus-off state

The CANj interrupt, caused by one of the CANi interrupt request factors listed above, is generated via the OR circuit.

If an interrupt request factor is established, the corresponding bit in the C0SISTR register is set to "1" (interrupt requested) when the CAN0 slot k completes a transmission or a reception. The corresponding bit in the C0EISTR register is set to "1" (interrupt requested) when the CANi module detects a bus error, moves into an error-passive state, or moves into a bus-off state.

The CAN0 interrupt request signal is set to "1" when the corresponding bit in the C0SISTR or C0EISTR is set to "1" and the corresponding bit in the C0SIMKR or C0EIMKR is set to "1".

When the CAN0 interrupt request signal changes from "0" to "1", all CANjR bits in the IIO9IR to IIO11IR registers are set to "1" (interrupt requested).

If at least one of the CANjE bits in the IIO9IE to IIO11IE registers is set to "1" (interrupt enabled), the IR bits in the corresponding CANjIC registers are set to "1" (interrupt requested). The CAN0 interrupt request signal remains set to "1" if another interrupt request causes a corresponding bit in the C0SISTR or C0EISTR to be set to "1" and the corresponding bit in the C0SIMKR or C0EIMKR to be set to "1" after the CAN0 interrupt request signal changes "0" to "1". The CANjR and IR bits also remain unchanged.

Bits in the C0SISTR or C0EISTR register and CANjR bits (j=0 to 2) in the IIO9IR to IIO11IR registers are not set to "0" automatically, interrupt acknowledgment notwithstanding. Set these bits to "0" by program.

The CANi interrupts are acknowledged when the CANjR bit in the IIO9IR to IIO11IR register and the corresponding bit in the C0SISTR or C0EISTR register, which are set to enable interrupts though setting the C0SIMKR or C0EIMKR register, are set to "0". If these bits remain set to "1", all CAN-associated interrupt request factors become invalid.

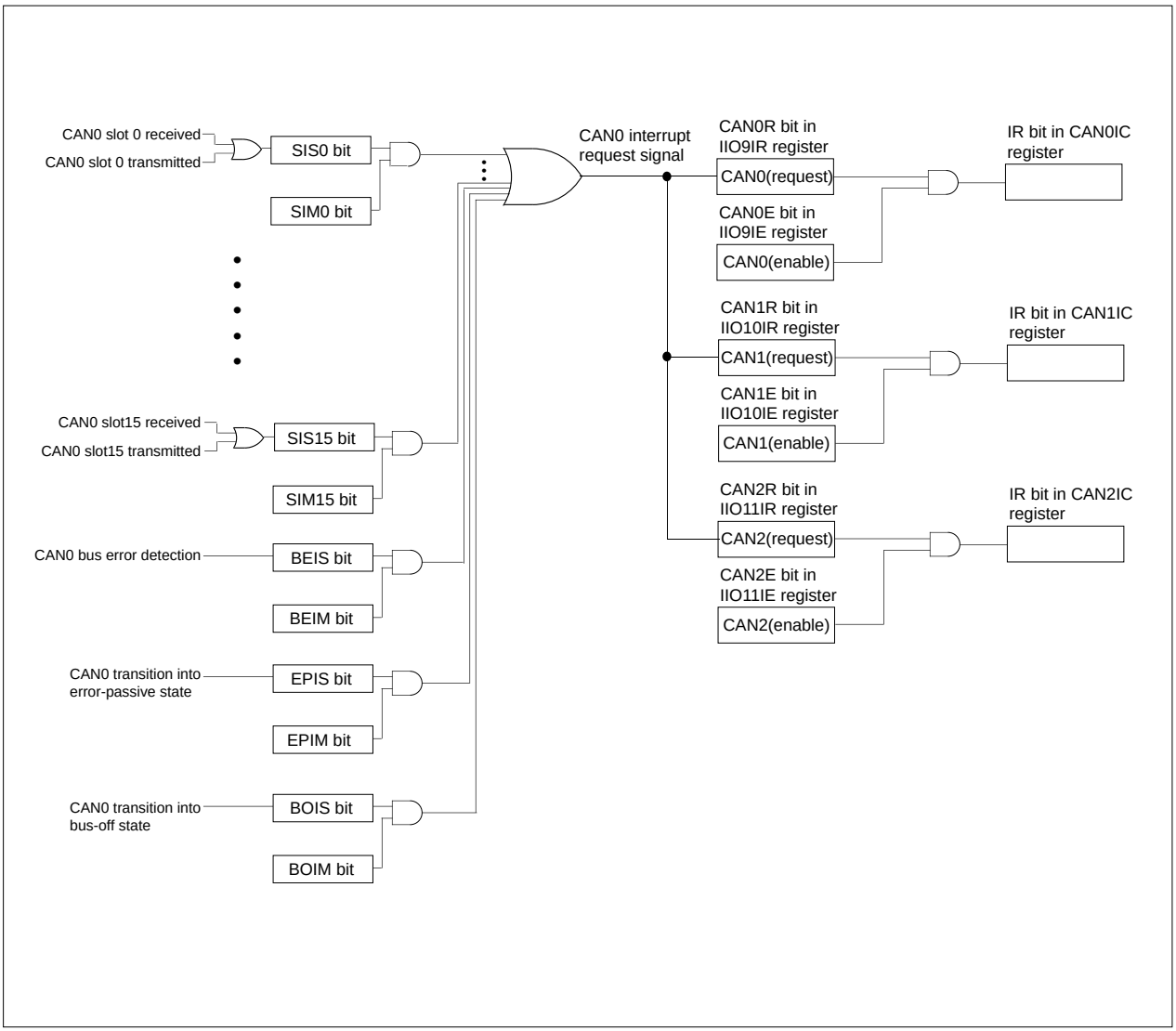


Figure 22.31 CAN Interrupts

23. DRAMC

The DRAM controller (DRAMC) controls the DRAM area, which ranges from 512 Kbytes to 8 Mbytes. Table 23.1 lists specifications of the DRAMC.

Table 23.1 DRAMC Specifications

Item	Specification
DRAM Area	512 KB, 1 MB, 2 MB, 4 MB, 8 MB
Bus Control	2CAS/1W
Refresh	$\overline{CAS}$-before-$\overline{RAS}$ refresh, Self refresh
Supported Function Mode	EDO, fast page mode
Wait State Insertion	1-wait state, 2-wait state

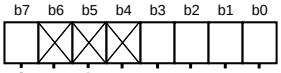
Table 23.2 shows pins associated with DRAMC. Signals listed in Table 23.2 are output by setting the AR2 to AR0 bits in the DRAMCONT register for the DRAM area and accessing DRAM. See **Table 7.9** for $\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$ and $\overline{DW}$ signal operations. Figure 23.1 shows the DRAMCONT register and REFCNT register.

Table 23.2 DRAMC-associated Pins

Port	Bus for Device Access except DRAM(1)	Bus for DRAM Access
P0	D_0 to D_7	D_0 to D_7
P1	D_8 to D_{15}	D_8 to D_{15}(2)
P3	A_8 to D_{15}	MA_0 to MA_7
$P4_0$ to $P4_4$	A_{16} to A_{20}	MA_8 to MA_{12}
$P5_0$	$\overline{WRL}$ / $\overline{WR}$	$\overline{CASL}$
$P5_1$	$\overline{WRH}$ / $\overline{BHE}$	$\overline{CASH}$
$P5_2$	$\overline{RD}$	$\overline{DW}$
$P5_6$	ALE	$\overline{RAS}$

NOTES:
1. This is an example of the separate bus and 16-bit data bus.
2. This bus is available when the DS2 bit in the DS register is set to "1" (16-bit data bus) and the PM02 bit in the PM0 register is set to "1" ($\overline{RD}$/$\overline{WRL}$/$\overline{WRH}$ in R/W mode).

DRAM Control Register

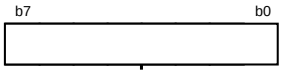


Symbol	Address	After Reset
DRAMCONT	0040_{16}	Indeterminate(1)

Bit Symbol	Bit Name	Function	RW
WT	Wait Select Bit(2)	0 : 2-wait state 1 : 1-wait state	RW
AR0	DRAM Area Select Bit	b3 b2 b1 0 0 0 : Disables DRAM 0 0 1 : Do not set to this value 0 1 0 : 512KB 0 1 1 : 1MB 1 0 0 : 2MB 1 0 1 : 4MB 1 1 0 : 8MB 1 1 1 : Do not set to this value	RW
AR1			RW
AR2			RW
___ (b6 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
SREF	Self-refresh Mode Bit(3)	0 : Self-refresh is off 1 : Self-refresh is on	RW

Notes:
1. Contents of the DRAMCONT register is indeterminate. DRAMC starts operation when this register is written to.
2. Bus cycle with two waits is 3-2-2.... It is 2-1-1... with one wait.
3. Refer to **23.2.2 Self-refresh** for SREF bit setup procedure.
   When the SREF bit is set to "1", both $\overline{RAS}$ and $\overline{CAS}$ output "L". When any external device, excluding DRAM, is attached, the WR signal is "L".
4. The DS register determines the data bus width . $\overline{CASH}$ is indeterminate when the 8-bit data bus is selected.

DRAM Refresh Interval Set Register



Symbol	Address	After Reset
REFCNT	0041_{16}	Indeterminate

Function	Setting Range	RW
If setting value is n, Refresh interval = CPU clock cycle X (n + 1) X 32	00_{16} to FF_{16}	RW

Figure 23.1 DRAMCONT Register and REFCNT Register

DRAMC is not available when the PM11 to PM10 bits in the PM1 register are set to "11$_2$" (mode 3). Set the PM11 to PM10 bits to "00$_2$," "01$_2$" or "10$_2$" (mode 0 to 2). When the 16-bit DRAM data bus is selected, set the PM02 bit in the PM0 register to "1" ($\overline{RD}$/$\overline{WRH}$/$\overline{WRL}$).
Required wait time between DRAM power-on and memory operation, and necessary processing of dummy cycle for refresh varies with externally attached DRAM specifications.

23.1 DRAMC Multiplexed Address Output

DRAMC outputs signals, which are multiplexed row addresses and column addresses, to address bus A$_8$ to A$_{20}$. Figure 23.2 shows an output format for multiplexed addresses.

23.2 Refresh

23.2.1 Refresh

Refresh method is the $\overline{CAS}$-before-$\overline{RAS}$ refresh. The REFCNT register controls the refresh interval. Refresh signals are not output in a hold state.
The setting value of the REFCNT register is obtained as follows:
The value of the REFCNT register (00$_{16}$ to FF$_{16}$) = refresh interval time / (CPU clock frequency X 32) - 1

23.2.2 Self-Refresh

The refresh signal described in 23.2.1 stops while the CPU stops in stop mode, etc. The DRAM self-refresh function can be activated by setting the self-refresh before the CPU stops. Setting and cancellation procedures for the self-refresh are as follows:

(1) Setting self-refresh (with 1 wait state, 4 Mbytes)

```
•••
mov.b   #00000001b,DRAMCONT     ;Set the AR2 to AR0 bits to "000₂" (DRAM disabled)
mov.b   #10001011b,DRAMCONT     ;Set the AR2 to AR0 bits again and the SREF bit to "1"
                                 (self-refresh on) simultaneously

nop     ;Execute the nop instruction twice
nop     ;
•••
```

(2) Cancellation of self-refresh (with 1 wait state, 4M bytes)

```
•••
mov.b   #00000001b,DRAMCONT     ;Set the AR2 to 0 bits to "000₂" (self-refresh cancellation)
                                 and the SREF bit to "0" (DRAM disabled) simultaneously
mov.b   #00001011b,DRAMCONT     ;Set the AR2 to AR0 bits again
mov.b   400h, 400h              ;DRAM access is disabled immediately after cancellation.
                                 This is an example of a dummy read operation.
•••
```

Both $\overline{RAS}$ and $\overline{CAS}$ are held "L" during self-refresh. When devices other than DRAM are attached, the $\overline{WR}$ signal is held "L". Take procedures such as applying an "H" signal to the $\overline{CS}$.
Figures 23.3 to 23.5 show bus timings during DRAM access.

(1) In 8-bit Bus Mode

Pin Function	MA12 (A20)	MA11 (A19)	MA10 (A18)	MA9 (A17)	MA8 (A16)	MA7 (A15)	MA6 (A14)	MA5 (A13)	MA4 (A12)	MA3 (A11)	MA2 (A10)	MA1 (A9)	MA0 (A8)
Row Address	(A20)	(A19)	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	–
Column Address	(A22)	(A22)	A19	A8	A7	A6	A5	A4	A3	A2	A1	A0	–

Address used for 512K-byte and 1M-byte DRAM area

Row Address	(A20)	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	–
Column Address	(A22)	A21	A20	A8	A7	A6	A5	A4	A3	A2	A1	A0	–

Address used for 2M-byte and 4M-byte DRAM area

Row Address	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	–
Column Address	(A22)	A22	A21	A8	A7	A6	A5	A4	A3	A2	A1	A0	–

Address used for 8M-byte DRAM area

(2) In 16-bit Bus Mode

Pin Function	MA12 (A20)	MA11 (A19)	MA10 (A18)	MA9 (A17)	MA8 (A16)	MA7 (A15)	MA6 (A14)	MA5 (A13)	MA4 (A12)	MA3 (A11)	MA2 (A10)	MA1 (A9)	MA0 (A8)
Row Address	(A20)	(A19)	A18	A17	A16	A15	A14	A13	A12	A11	A10	(A9)	–
Column Address	(A22)	(A20)	$\overline{A9}$	A8	A7	A6	A5	A4	A3	A2	A1	(A0)	–

Address used for 512K-byte DRAM area

Row Address	(A20)	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	(A9)	–
Column Address	(A22)	A20	$\overline{A9}$	A8	A7	A6	A5	A4	A3	A2	A1	(A0)	–

Address used for 1M-byte and 2M-byte DRAM area

Row Address	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	(A9)	–
Column Address	A22	A21	$\overline{A9}$	A8	A7	A6	A5	A4	A3	A2	A1	(A0)	–

Address used for 4M-byte and 8M-byte(1) DRAM area

( ): disabled bits, :bits which output addresses changed by data bus width and the DRAM area

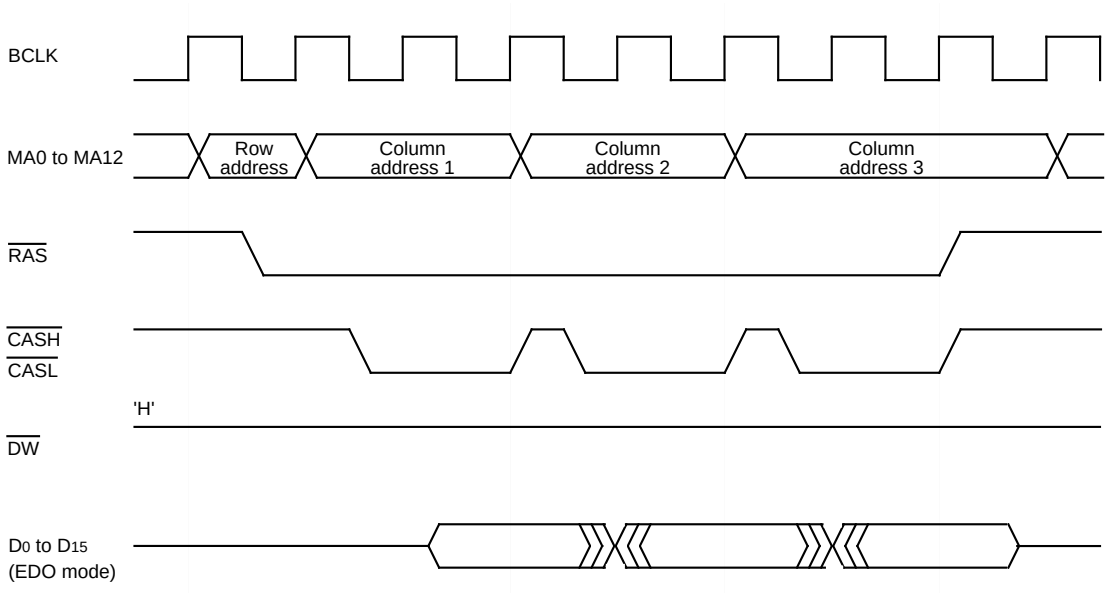
–: indetermimate

NOTES:

1. The above applies when using a 4Mx1 or 4Mx4 memory configuration. When using a 4Mx16 configuration, implement the following combinations:
   For row addresses, MA0 to MA12; for column addresses, MA2 to MA8, MA11 and MA12.
   Or for row addresses, MA1 to MA12; for column addresses, MA2 to MA9, MA11 and MA12.

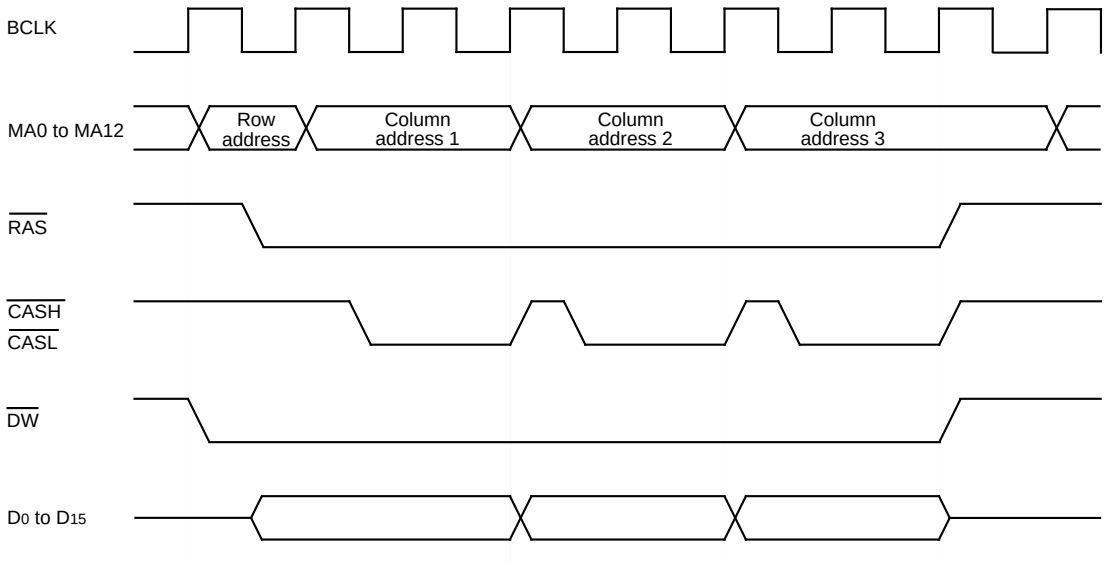
Figure 23.2 Multiplexed Address Output Pattern

(1) Read cycle (WT bit = 0 with 2 wait states)



NOTES:
1. With an 8-bit data bus, only $\overline{\text{CASL}}$ outputs a data enabled to read. $\overline{\text{CASH}}$ outputs an indeterminate data.

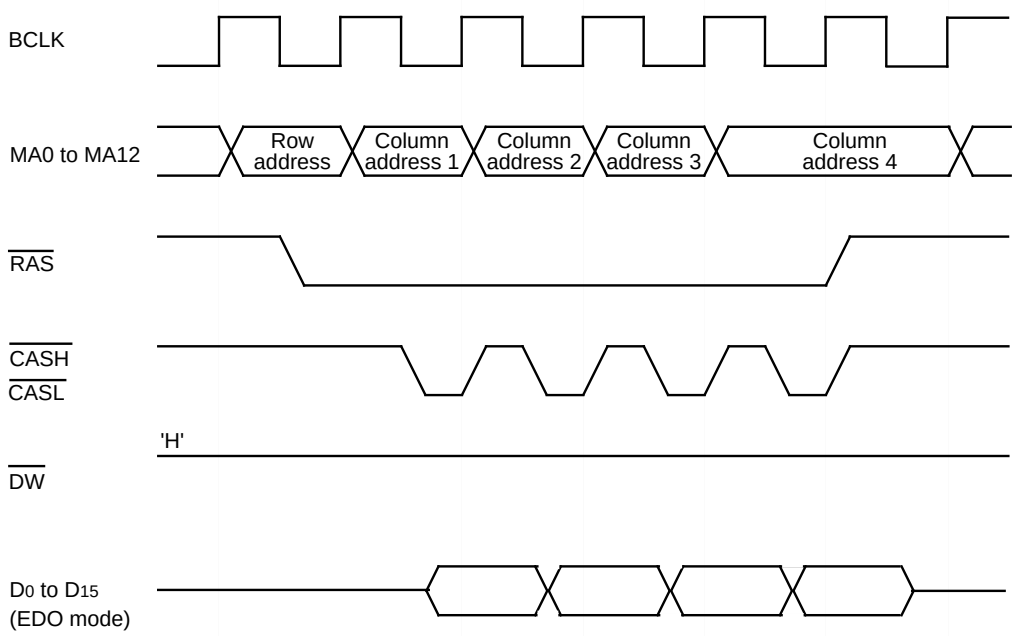
(2) Write cycle (WT bit = 0)



NOTES:
1. With an 8-bit data bus, only $\overline{\text{CASL}}$ outputs data enabled to read. $\overline{\text{CASH}}$ outputs an indeterminate data.

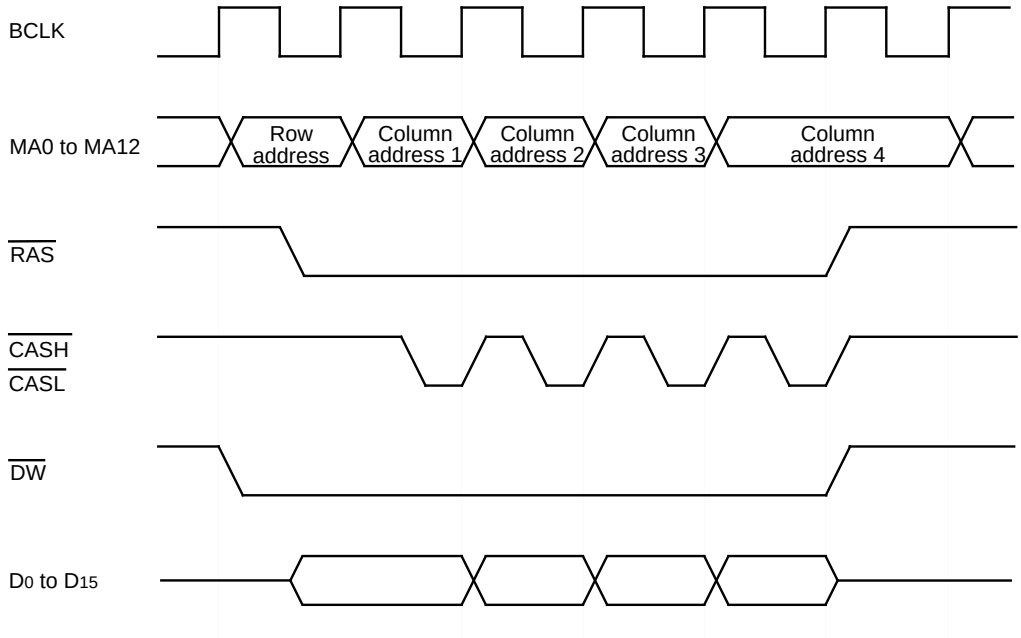
Figure 23.3 Bus Timing during DRAM Access (1)

(1) Read cycle (WT bit = 1 with 1 wait state)



NOTES:
1. With an 8-bit data bus, only $\overline{CASL}$ outputs a data enabled to read. $\overline{CASH}$ outputs an indeterminate data.

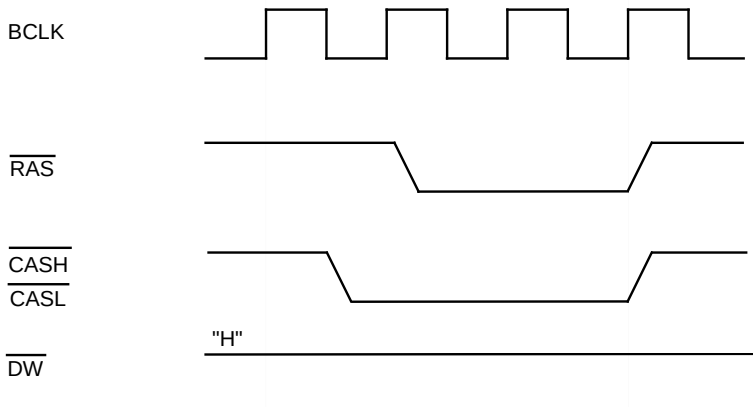
(2) Write cycle (WT bit = 1)



NOTES:
1. With an 8-bit data bus, only $\overline{CASL}$ outputs a data enabled to read. $\overline{CASH}$ outputs an indeterminate data.

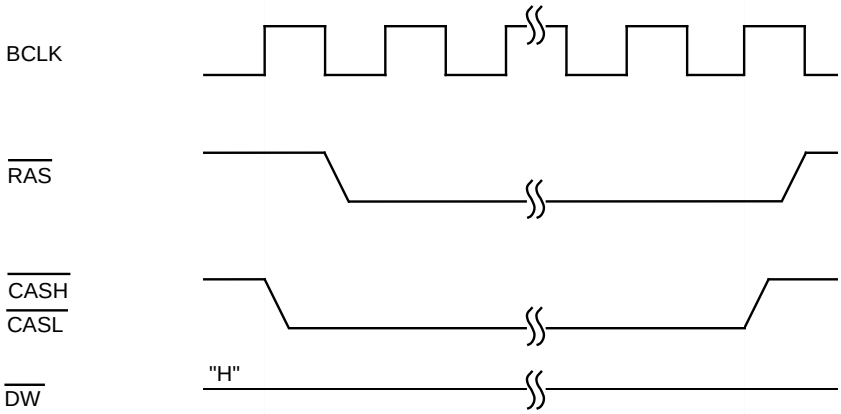
Figure 23.4 Bus Timing during DRAM Access (2)

(1) $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle



NOTES:
1. With an 8-bit data bus, only $\overline{CASL}$ outputs a data enabled to read. $\overline{CASH}$ outputs an indeterminate data.

(1) Self-Refresh cycle



NOTES:
1. With an 8-bit data bus, only $\overline{CASL}$ outputs a data enabled to read. $\overline{CASH}$ outputs an indeterminate data.

Figure 23.5 Bus Timing during DRAM Access (3)

24. Programmable I/O Ports

87 programmable I/O ports from P0 to P10 (excluding P8$_5$) are available in the 100-pin package and 123 programmable I/O ports from P0 to P15 (excluding P8$_5$) are in the 144-pin package. The direction registers determine each port status, input or output. The pull-up control registers determine whether the ports, divided into groups of four ports, are pulled up or not. P8$_5$ is an input port and no pull-up for this port is allowed. The P8_5 bit in the P8 register indicates an $\overline{\text{NMI}}$ input level since P8$_5$ shares pins with $\overline{\text{NMI}}$.

Figures 24.1 to 24.4 show programmable I/O port configurations.

Each pin functions as the programmable I/O port, an I/O pin for internal peripheral functions or the bus control pin.

To use the pins as input or output pins for internal peripheral functions, refer to the explanations for each function. Refer to **7. Bus** when used as the bus control pin.

The registers, described below, are associated with the programmable I/O ports.

24.1 Port Pi Direction Register (PDi Register, i=0 to 15)

Figure 24.5 shows the PDi register.

The PDi register selects input or output status of a programmable I/O port. Each bit in the PDi register corresponds to a port.

In memory expansion and microprocessor mode, pins being used as bus control pins (A0 to A$_{22}$, $\overline{\text{A}_{23}}$, D$_0$ to D$_{15}$, MA$_0$ to MA$_{12}$, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{WRL}}$/$\overline{\text{WR}}$/$\overline{\text{CASL}}$, $\overline{\text{WRH}}$/$\overline{\text{BHE}}$, $\overline{\text{RD}}$/$\overline{\text{DW}}$, BCLK/ALE/CLKOUT, $\overline{\text{HLDA}}$/ALE, $\overline{\text{HOLD}}$, ALE/$\overline{\text{RAS}}$, and $\overline{\text{RDY}}$) cannot be controlled by the PDi register. No bits controlling P8$_5$ are provided in the direction registers .

24.2 Port Pi Register (Pi Register, i=0 to 15)

Figure 24.6 shows the Pi register.

The Pi register writes and reads data to communicate with external devices. The Pi register consists of a port latch to hold output data and a circuit to read pin states. Each bit in the Pi register corresponds to a port.

In memory expansion and microprocessor mode, pins being used as bus control pins (A$_0$ to A$_{22}$, $\overline{\text{A}_{23}}$, D$_0$ to D$_{15}$, MA$_0$ to MA$_{12}$, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{WRL}}$/$\overline{\text{WR}}$/$\overline{\text{CASL}}$, $\overline{\text{WRH}}$/$\overline{\text{BHE}}$, $\overline{\text{RD}}$/$\overline{\text{DW}}$, BCLK/ALE/CLKOUT, $\overline{\text{HLDA}}$/ALE, $\overline{\text{HOLD}}$, ALE/$\overline{\text{RAS}}$, and $\overline{\text{RDY}}$) cannot be controlled by the Pi register.

24.3 Function Select Register Aj (PSj Register) (j=0 to 3, 5 to 9)

Figures 24.7 to 24.11 show the PSj registers.

The PSj register selects either I/O port or peripheral function output if an I/O port shares pins with a peripheral function output (excluding DA0 and DA1.)

Tables 24.3 to 24.12 list peripheral function output control settings for each pin.

When multiple peripheral function outputs are assigned to a pin, set the PSLk (k=0 to 3) and PSC registers to select which function is used.

24.4 Function Select Register Bk (PSLk Register) (k=0 to 3)

Figures 24.12 and 24.13 show the PSL0 to PSL3 registers.

When multiple peripheral function outputs are assigned to a pin, the PSL0 to PSL3 registers select which peripheral function output is used.

Refer to **24.9 Analog Input and Other Peripheral Function Input** for the PSL3_3 to PSL3_6 bits in the PSL3 register.

24.5 Function Select Register C (PSC Register)

Figure 24.14 show the PSC register.

When multiple peripheral function outputs are assigned to a pin, the PSC register select which peripheral function output is used.

Refer to **24.9 Analog Input and Other Peripheral Function Input** for the PSC_7 bit in the PSC register.

24.6 Pull-up Control Register 0 to 4 (PUR0 to PUR4 Registers)

Figures 24.15 to 24.16 show the PUR0 to PUR4 registers.

The PUR0 to PUR4 registers select whether the ports, divided into groups of four ports, are pulled up or not. Ports with bits in the PUR0 to PUR4 registers set to "1" (pull-up) and the direction registers set to "0" (input mode) are pulled up.

Set bits in the PUR0 and PUR1 registers which control P0 to P5, used as bus in memory expansion and microprocessor mode, to "0" (no pull-up) . P0, P1, $P4_0$ to $P4_3$ can be pulled up when they are used as input ports in memory expansion and microprocessor mode.

24.7 Port Control Register (PCR Register)

Figure 24.17 shows the PCR register.

The PCR register selects either CMOS output or N-channel open drain output as the P1 output format. If the PCR0 bits is set to "1", N-channel open drain output is selected because the P-channel in the CMOS port is turned off. This is, however, not a perfect open drain. Therefore, the absolute maximum rating of the input voltage is from -0.3V to Vcc + 0.3V.

If P1 is used as the data bus in memory expansion and microprocessor mode, set the PCR0 bit to "0". If P1 is used as a port in memory expansion and microprocessor mode, the PCR0 bit determines the output format.

24.8 Input Function Select Register (IPS Register)

Figure 24.18 shows the IPS registers.

The IPS0 to IPS1 and IPS3 bits in the IPS register and the IPSA_0 and IPSA_3 bits in the IPSA register select which pin is assigned the intelligent I/O or CAN input functions.

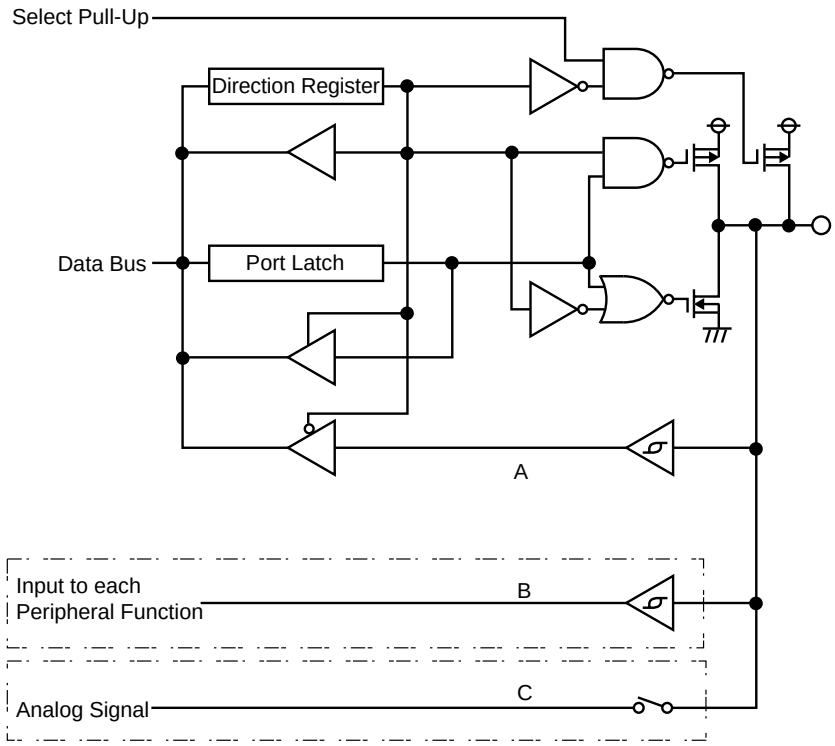
Refer to **24.9 Analog Input and Other Peripheral Function Input** for the IPS2 bit.

24.9 Analog Input and Other Peripheral Function Input

The PSL3_3 to PSL3_6 bits in the PSL3 register, the PSC_7 bit in the PSC register and the IPS2 bit in the ISP register are each used to separate analog I/O ports from other peripheral functions. Setting the corresponding bit to "1" (analog I/O) to use the analog I/O port (DA0, DA1, ANEX0, ANEX1, AN_4 to AN_7 or $AN15_0$ to $AN15_7$) prevents an intermediate potential from being impressed to other peripheral functions. The impressed intermediate potential may cause increase in power consumption.

Set the corresponding bit to "0" (except analog I/O) when analog I/O is not used. All peripheral function inputs except the analog I/O port are available when the corresponding bit is set to "0". These inputs are indeterminate when the bit is set to "1". When the PSC_7 bit is set to "1", key input interrupt request remains unchanged regardless of $\overline{KI_0}$ to $\overline{KI_3}$ pin input level change.

Programmable I/O Ports



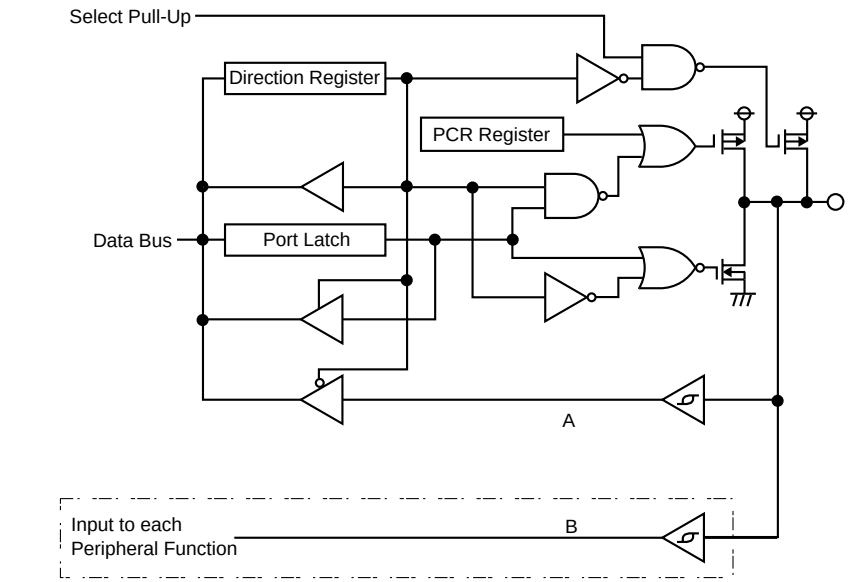
Port \ Option	(A) Hysteresis	Circuit (B) Peripheral Function Input	Circuit (C) Analog I/F
P0$_0$ to P0$_7$ P2$_0$ to P2$_7$	–	–	○
P3$_0$ to P3$_7$ P4$_0$ to P4$_7$ P5$_0$ to P5$_2$ P5$_4$	–	–	–
P5$_5$	–	○	–
P5$_6$	–	–	–
P5$_7$	–	○	–
P8$_3$, P8$_4$	○	○	–
P8$_6$	–	–	–
P8$_7$	–	○	○
P10$_0$ to P10$_3$	–	–	○
P10$_4$ to P10$_7$	○	○	○
(Note 1) P11$_4$ P14$_4$ to P14$_6$	–	–	–
(Note 1) P15$_2$, P15$_3$ P15$_6$, P15$_7$	–	○	○

○: Available, – : Not available

NOTES:
1. These ports are provided in the 144-pin package only.

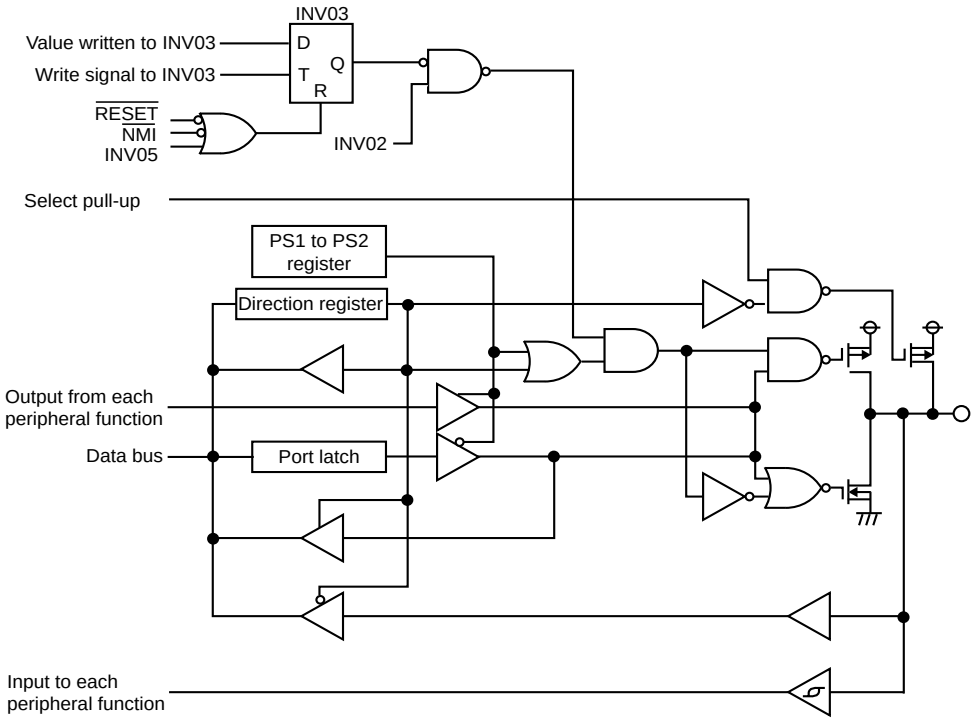
Figure 24.1 Programmable I/O Ports (1)

Programmable I/O Ports with the Port Control Register



Port \ Option	(A) Hysteresis	Circuit (B) Peripheral Function Input
P1$_0$ to P1$_4$	—	—
P1$_5$ to P1$_7$	○	○

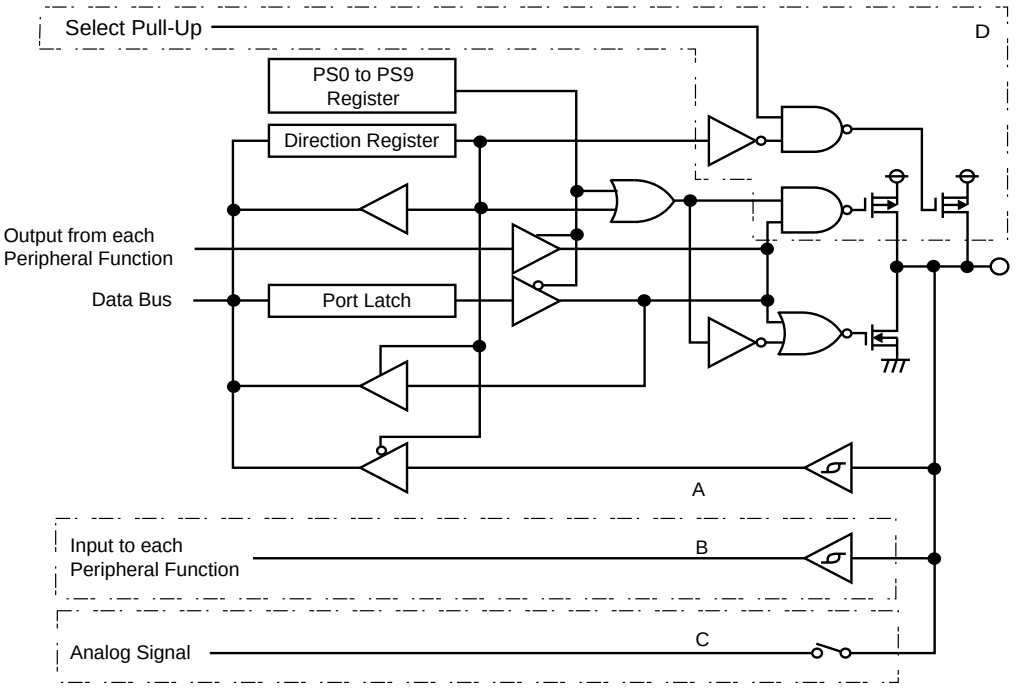
○ : Available, — : Not available



Port : P7$_2$, P7$_3$, P7$_4$, P7$_5$, P8$_0$, P8$_1$

Figure 24.2 Programmable I/O Ports (2)

Programmable I/O Ports with the Function Select Register



Port \ Option	(A) Hysteresis	Circuit (B) Peripheral Function Input	Circuit (C) Analog I/F	Circuit (D)
$P5_3$	–	–	–	○
$P6_0$ to $P6_7$	–	○	–	○
$P7_0$, $P7_1$ (Note 1)	–	○	–	–
$P7_6$, $P7_7$	–	○	–	○
$P8_2$	○	○	–	○
$P9_0$ to $P9_2$	–	○	–	○
$P9_3$ to $P9_6$	–	○	○	○
$P9_7$	–	○	–	○
(Note 2) $P11_0$	–	–	–	○
$P11_1$, $P11_2$	–	○	–	○
$P11_3$ $P12_0$	–	–	–	○
$P12_1$, $P12_2$	–	○	–	○
$P12_3$ to $P12_7$ $P13_0$ to $P13_4$	–	–	–	○
$P13_5$, $P13_6$	–	○	–	○
$P13_7$ $P14_0$, $P14_1$	–	–	–	○
$P14_2$, $P14_3$	–	○	–	○
$P15_0$, $P15_1$ $P15_4$, $P15_5$	–	○	○	○

○ : Available, – : Not available

NOTES:
1. $P7_0$ and $P7_1$ are ports for the N-channel open drain output.
2. These ports are provided in the 144-pin package only.

Figure 24.3 Programmable I/O Ports (3)

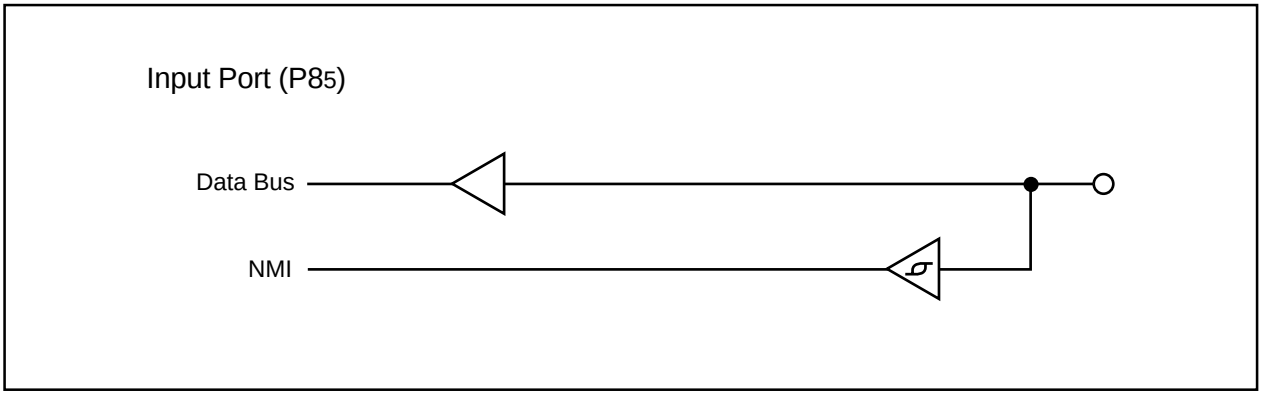


Figure 24.4 Programmable I/O Ports (4)

Port Pi Direction Register (i=0 to 15)(2)

b7 b6 b5 b4 b3 b2 b1 b0

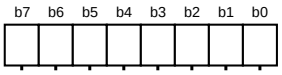
Symbol	Address	After Reset
PD0 to PD3	$03E2_{16}$, $03E3_{16}$, $03E6_{16}$, $03E7_{16}$	00_{16}
PD4 to PD7	$03EA_{16}$, $03EB_{16}$, $03C2_{16}$, $03C3_{16}$	00_{16}
PD8	$03C6_{16}$(4)	$00X0\ 0000_2$
PD9 to PD10	$03C7_{16}$(1), $03CA_{16}$	00_{16}
PD11	$03CB_{16}$(3,4)	$XXX0\ 0000_2$
PD12 to PD13	$03CE$, $03CF_{16}$	00_{16}
PD14	$03D2_{16}$(3,4)	$X000\ 0000_2$
PD15	$03D3_{16}$(3)	00_{16}

Bit Symbol	Bit Name	Function	RW
PDi_0	Port Pi0 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_1	Port Pi1 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_2	Port Pi2 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_3	Port Pi3 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_4	Port Pi4 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_5	Port Pi5 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_6	Port Pi6 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PDi_7	Port Pi7 Direction Register	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW

NOTES:
1. Set the PD9 register immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 register.
2. In memory expansion and microprocessor mode, the direction register of pins being used as bus control pins (A_0 to A_{22}, $\overline{A_{23}}$, D_0 to D_{15}, MA0 to MA12, $\overline{CS0}$ to $\overline{CS3}$, $\overline{WRL}/\overline{WR}/\overline{CASL}$, $\overline{WRH}/\overline{BHE}/\overline{CASH}$, $\overline{RD}/\overline{DW}$, BCLK/ALE/$CLK_{OUT}$, $\overline{HLDA}$/ALE, $\overline{HOLD}$, ALE/$\overline{RAS}$ and $\overline{RDY}$) cannot be changed.
3. Set the PD11 to PD15 registers to "FF_{16}" in the 100-pin package.
4. Nothing is assigned to the PD8_5 bit in the PD8 register, the PD11_5 to PD11_7 bits in the PD11 register and the P14_7 bit in the PD14 register. If write, set these bits to "0". When read, their contents are indeterminate.

Figure 24.5 PD0 to PD15 Registers

Port Pi Register (i=0 to 15)(1, 2)



Symbol	Address	After Reset
P0 to P5	03E0$_{16}$, 03E1$_{16}$, 03E4$_{16}$, 03E5$_{16}$, 03E8$_{16}$, 03E9$_{16}$	Indeterminate
P6 to P10	03C0$_{16}$, 03C1$_{16}$(3), 03C4$_{16}$(4), 03C5$_{16}$, 03C8$_{16}$	Indeterminate
P11 to P15	03C9$_{16}$(5), 03CC$_{16}$, 03CD$_{16}$, 03D0$_{16}$(5), 03D1$_{16}$	Indeterminate

Bit Symbol	Bit Name	Function	RW
Pi_0	Port Pi$_0$ Register	Pin levels can be read by reading bits corresponding to programmable ports in input mode. Pin levels can be controlled by writing to bits corresponding to programmable ports in output mode. 0 : "L" level 1 : "H" level	RW
Pi_1	Port Pi$_1$ Register		RW
Pi_2	Port Pi$_2$ Register		RW
Pi_3	Port Pi$_3$ Register		RW
Pi_4	Port Pi$_4$ Register		RW
Pi_5	Port Pi$_5$ Register		RW
Pi_6	Port Pi$_6$ Register		RW
Pi_7	Port Pi$_7$ Register		RW

NOTES:
1. In memory expansion and microprocessor mode, the direction register of pins being used as bus control pins (A$_0$ to A$_{22}$, $\overline{A_{23}}$, D$_0$ to D$_{15}$, MA0 to MA12, $\overline{CS0}$ to $\overline{CS3}$, $\overline{WRL}$/$\overline{WR}$/CASL, $\overline{WRH}$/$\overline{BHE}$/$\overline{CASH}$, $\overline{RD}$/$\overline{DW}$, BCLK/ALE/CLKOUT, $\overline{HLDA}$/ALE, $\overline{HOLD}$, ALE/$\overline{RAS}$, and $\overline{RDY}$) cannot be changed.
2. The P11 to P15 registers are provided in the 144-pin package only.
3. P7$_0$ and P7$_1$ are ports for the N-channel open drain output. The pins go into a high-impedance state when P7$_0$ and P7$_1$ output a high-level signal ("H").
4. The P8$_5$ bit is for read only.
5. Nothing is assigned to the P11_5 to P11_7 bits in the P11 register and the P14_7 bit in the P14 register. If write, set these bits to "0". When read, their contents are indeterminate.

Figure 24.6 P0 to P15 Registers

Function Select Register A0

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
								PS0	$03B0_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
PS0_0	Port $P6_0$ Output Function Select Bit	0 : I/O port 1 : $\overline{RTS0}$	RW
PS0_1	Port $P6_1$ Output Function Select Bit	0 : I/O port 1 : CLK0 output	RW
PS0_2	Port $P6_2$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL0_2 bit	RW
PS0_3	Port $P6_3$ Output Function Select Bit	0 : I/O port 1 : TxD0/SDA0 output	RW
PS0_4	Port $P6_4$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL0_4 bit	RW
PS0_5	Port $P6_5$ Output Function Select Bit	0 : I/O port 1 : CLK1 output	RW
PS0_6	Port $P6_6$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL0_6 bit	RW
PS0_7	Port $P6_7$ Output Function Select Bit	0 : I/O port 1 : TxD1/SDA1 output	RW

Function Select Register A1

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
								PS1	$03B1_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
PS1_0	Port $P7_0$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL1_0 bit	RW
PS1_1	Port $P7_1$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL1_1 bit	RW
PS1_2	Port $P7_2$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL1_2 bit	RW
PS1_3	Port $P7_3$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL1_3 bit	RW
PS1_4	Port $P7_4$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL1_4 bit	RW
PS1_5	Port $P7_5$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL1_5 bit	RW
PS1_6	Port $P7_6$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL1_6 bit	RW
PS1_7	Port $P7_7$ Output Function Select Bit	0 : I/O port 1 : OUTC01/ISCLK0 output	RW

Figure 24.7 PS0 Register and PS1 Register

Function Select Register A2

b7	b6	b5	b4	b3	b2	b1	b0
0	0	X	0	0			

Symbol	Address	After Reset
PS2	$03B4_{16}$	$00X0\ 0000_2$

Bit Symbol	Bit Name	Function	RW
PS2_0	Port $P8_0$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL2_0 bit	RW
PS2_1	Port $P8_1$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL2_1 bit	RW
PS2_2	Port $P8_2$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL2_2 bit	RW
____ (b4 - b3)	Reserved Bit	Set to "0"	RW
____ (b5)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
____ (b7 - b6)	Reserved Bit	Set to "0"	RW

Function Select Register A3(1)

b7	b6	b5	b4	b3	b2	b1	b0

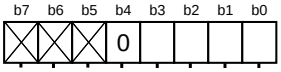
Symbol	Address	After Reset
PS3	$03B5_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
PS3_0	Port $P9_0$ Output Function Select Bit	0 : I/O port 1 : CLK3 output	RW
PS3_1	Port $P9_1$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL3_1 bit	RW
PS3_2	Port $P9_2$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL3_2 bit	RW
PS3_3	Port $P9_3$ Output Function Select Bit	0 : I/O port 1 : $\overline{RTS3}$	RW
PS3_4	Port $P9_4$ Output Function Select Bit	0 : I/O port 1 : $\overline{RTS4}$	RW
PS3_5	Port $P9_5$ Output Function Select Bit	0 : I/O port 1 : CLK4 output	RW
PS3_6	Port $P9_6$ Output Function Select Bit	0 : I/O port 1 : TxD4/SDA4 output	RW
PS3_7	Port $P9_7$ Output Function Select Bit	0 : I/O port 1 : Selected by the PSL3_7 bit	RW

NOTES:
1. Set the PD9 register immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 register.

Figure 24.8 PS2 Register and PS3 Register

Function Select Register A5(1)

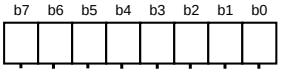


Symbol	Address	After Reset
PS5	03B9$_{16}$	XXX0 0000$_2$

Bit Symbol	Bit Name	Function	RW
PS5_0	Port P11$_0$ Output Function Select Bit	0 : I/O port 1 : OUTC1$_0$/ ISTxD1/BE1$_{OUT}$	RW
PS5_1	Port P11$_1$ Output Function Select Bit	0 : I/O port 1 : OUTC1$_1$/ ISCLK1 output	RW
PS5_2	Port P11$_2$ Output Function Select Bit	0 : I/O port 1 : OUTC1$_2$	RW
PS5_3	Port P11$_3$ Output Function Select Bit	0 : I/O port 1 : OUTC1$_3$	RW
—— (b4)	Reserved Bit	Set to "0"	RW
—— (b7 - b5)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. The PS5 register is provided in the 144-pin package only.

Function Select Register A6(1)



Symbol	Address	After Reset
PS6	03BC$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
PS6_0	Port P12$_0$ Output Function Select Bit	0 : I/O port 1 : OUTC3$_0$/ISTxD3	RW
PS6_1	Port P12$_1$ Output Function Select Bit	0 : I/O port 1 : OUTC3$_1$/ISCLK3 output	RW
PS6_2	Port P12$_2$ Output Function Select Bit	0 : I/O port 1 : OUTC3$_2$	RW
PS6_3	Port P12$_3$ Output Function Select Bit	0 : I/O port 1 : OUTC3$_3$	RW
PS6_4	Port P12$_4$ Output Function Select Bit	0 : I/O port 1 : OUTC3$_4$	RW
PS6_5	Port P12$_5$ Output Function Select Bit	0 : I/O port 1 : OUTC3$_5$	RW
PS6_6	Port P12$_6$ Output Function Select Bit	0 : I/O port 1 : OUTC3$_6$	RW
PS6_7	Port P12$_7$ Output Function Select Bit	0 : I/O port 1 : OUTC3$_7$	RW

NOTES:
1. The PS6 register is provided in the 144-pin package only.

Figure 24.9 PS5 Register and PS6 Register

Function Select Register A7(1)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
PS7	$03BD_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
PS7_0	Port P13$_0$ Output Function Select Bit	0 : I/O port 1 : OUTC2$_4$	RW
PS7_1	Port P13$_1$ Output Function Select Bit	0 : I/O port 1 : OUTC2$_5$	RW
PS7_2	Port P13$_2$ Output Function Select Bit	0 : I/O port 1 : OUTC2$_6$	RW
PS7_3	Port P13$_3$ Output Function Select Bit	0 : I/O port 1 : OUTC2$_3$	RW
PS7_4	Port P13$_4$ Output Function Select Bit	0 : I/O port 1 : OUTC20/ISTXD2/IE$_{OUT}$	RW
PS7_5	Port P13$_5$ Output Function Select Bit	0 : I/O port 1 : OUTC2$_2$	RW
PS7_6	Port P13$_6$ Output Function Select Bit	0 : I/O port 1 : OUTC2$_1$/ISCLK2 output	RW
PS7_7	Port P13$_7$ Output Function Select Bit	0 : I/O port 1 : OUTC2$_7$	RW

NOTES:
1. The PS7 register is provided in the 144-pin package only.

Function Select Register A8(1)

b7	b6	b5	b4	b3	b2	b1	b0
X	0	0	0				

Symbol	Address	After Reset
PS8	$03A0_{16}$	$X000\ 0000_2$

Bit Symbol	Bit Name	Function	RW
PS8_0	Port P14$_0$ Output Function Select Bit	0 : I/O port 1 : OUTC1$_4$	RW
PS8_1	Port P14$_1$ Output Function Select Bit	0 : I/O port 1 : OUTC1$_5$	RW
PS8_2	Port P14$_2$ Output Function Select Bit	0 : I/O port 1 : OUTC1$_6$	RW
PS8_3	Port P14$_3$ Output Function Select Bit	0 : I/O port 1 : OUTC1$_7$	RW
____ (b6 - b4)	Reserved Bit	Set to "0"	RW
____ (b7)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1: The PS8 register is provided in the 144-pin package only.

Figure 24.10 PS7 Register and PS8 Register

Function Select Register A9(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0			0	0		

Symbol	Address	After Reset
PS9	$03A1_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
PS9_0	Port P15$_0$ Output Function Select Bit	0 : I/O port 1 : OUTC0$_0$/ ISTxD0/BE0$_{OUT}$	RW
PS9_1	Port P15$_1$ Output Function Select Bit	0 : I/O port 1 : OUTC0$_1$/ ISCLK0 output	RW
—— (b3 - b2)	Reserved Bit	Set to "0"	RW
PS9_4	Port P15$_4$ Output Function Select Bit	0 : I/O port 1 : OUTC0$_4$	RW
PS9_5	Port P15$_5$ Output Function Select Bit	0 : I/O port 1 : OUTC0$_5$	RW
—— (b7 - b6)	Reserved Bit	Set to "0"	RW

NOTES:
1. The PS9 register is provided in the 144-pin package only.

Figure 24.11 PS9 Register

Function Select Register B0

b7	b6	b5	b4	b3	b2	b1	b0
0		0		0		0	0

Symbol	Address	After Reset
PSL0	$03B2_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
——— (b1 - b0)	Reserved Bit	Set to "0"	RW
PSL0_2	Port $P6_2$ Output Peripheral Function Select Bit	0 : SCL0 1 : STxD0	RW
——— (b3)	Reserved bit	Set to "0"	RW
PSL0_4	Port $P6_4$ Output Peripheral Function Select Bit	0 : $\overline{RTS1}$ 1 : $OUTC2_1$/ISCLK2 output	RW
——— (b5)	Reserved Bit	Set to "0"	RW
PSL0_6	Port $P6_6$ Output Peripheral Function Select Bit	0 : SCL1 output 1 : STxD1	RW
——— (b7)	Reserved Bit	Set to "0"	RW

Function Select Register B1

b7	b6	b5	b4	b3	b2	b1	b0
0							

Symbol	Address	After Reset
PSL1	$03B3_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
PSL1_0	Port $P7_0$ Output Peripheral Function Select Bit	0 : Selected by the PSC_0 bit 1 : $TA0_{OUT}$ output	RW
PSL1_1	Port $P7_1$ Output Peripheral Function Select Bit	0 : Selected by the PSC_1 bit 1 : STxD2	RW
PSL1_2	Port $P7_2$ Output Peripheral Function Select Bit	0 : Selected by the PSC_2 bit 1 : $TA1_{OUT}$ output	RW
PSL1_3	Port $P7_3$ Output Peripheral Function Select Bit	0 : Selected by the PSC_3 bit 1 : $\overline{V}$	RW
PSL1_4	Port $P7_4$ Output Peripheral Function Select Bit	0 : Selected by the PSC_4 bit 1 : W	RW
PSL1_5	Port $P7_5$ Output Peripheral Function Select Bit	0 : $\overline{W}$ 1 : $OUTC1_2$	RW
PSL1_6	Port $P7_6$ Output Peripheral Function Select Bit	0 : Selected by the PSC_6 bit 1 : $TA3_{OUT}$ output	RW
——— (b7)	Reserved Bit	Set to "0"	RW

NOTES:
1. Set the corresponding PSC_i bit in the PSC register to "0" when setting the PSL1_i bit (i=0 to 4, 6) to "1".

Figure 24.12 PSL0 Register and PSL1 Register

Function Select Register B2

b7	b6	b5	b4	b3	b2	b1	b0
0	0	X	0	0			

Symbol	Address	After Reset
PSL2	$03B6_{16}$	$00X0\ 0000_2$

Bit Symbol	Bit Name	Function	RW
PSL2_0	Port $P8_0$ Output Peripheral Function Select Bit	0 : $TA4_{OUT}$ output 1 : U	RW
PSL2_1	Port $P8_1$ Output Peripheral Function Select Bit	0 : $\overline{U}$ 1 : $OUTC3_0$/ISTxD3	RW
PSL2_2	Port $P8_2$ Output Peripheral Function Select Bit	0 : $OUTC3_2$ 1 : CAN_{OUT}	RW
____ (b4 - b3)	Reserved Bit	Set to "0"	RW
____ (b5)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
____ (b7 - b6)	Reserved Bit	Set to "0"	RW

Function Select Register B3

b7	b6	b5	b4	b3	b2	b1	b0
							0

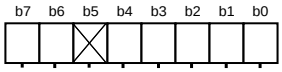
Symbol	Address	After Reset
PSL3	$03B7_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
____ (b0)	Reserved Bit	Set to "0"	RW
PSL3_1	Port $P9_1$ Output Peripheral Function Select Bit	0 : SCL3 output 1 : STxD3	RW
PSL3_2	Port $P9_2$ Output Peripheral Function Select Bit	0 : TxD3/SDA3 output 1 : $OUTC2_0$/ISTxD2/IE_{OUT}	RW
PSL3_3	Port $P9_3$ Output Peripheral Function Select Bit	0 : Other than DA0 1 : DA0(1)	RW
PSL3_4	Port $P9_4$ Output Peripheral Function Select Bit	0 : Other than DA1 1 : DA1(1)	RW
PSL3_5	Port $P9_5$ Output Peripheral Function Select Bit	0 : Other than ANEX0 1 : ANEX0(1)	RW
PSL3_6	Port $P9_6$ Output Peripheral Function Select Bit	0 : Other than ANEX1 1 : ANEX1(1)	RW
PSL3_7	Port $P9_7$ Output Peripheral Function Select Bit	0 : SCL4 output 1 : STxD4	RW

NOTES:
1. Although DA0, DA1, ANEX0 and ANEX1 can be used when this bit is set to "0", power consumption may increase.

Figure 24.13 PSL2 Register and PSL3 Register

Function Select Register C



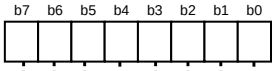
Symbol	Address	After Reset
PSC	$03AF_{16}$	$00X0\ 0000_2$

Bit Symbol	Bit Name	Function	RW
PSC_0	Port $P7_0$ Output Peripheral Function Select Bit	0 : TxD2/SDA2 output 1 : $OUTC2_0$/ISTxD2/IE_{OUT}	RW
PSC_1	Port $P7_1$ Output Peripheral Function Select Bit	0 : SCL2 output 1 : $OUTC2_2$	RW
PSC_2	Port $P7_2$ Output Peripheral Function Select Bit	0 : CLK_2 output 1 : V	RW
PSC_3	Port $P7_3$ Output Peripheral Function Select Bit	0 : $\overline{RTS2}$ 1 : $OUTC1_0$/ISTxD1/$BE1_{OUT}$	RW
PSC_4	Port $P7_4$ Output Peripheral Function Select Bit	0 : $TA2_{OUT}$ output 1 : $OUTC1_1$/ISCLK1 output	RW
(b5)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
PSC_6	Port $P7_6$ Output Peripheral Function Select Bit	0 : $OUTC0_0$/ISTxD0/$BE0_{OUT}$ 1 : CAN_{OUT}	RW
PSC_7	Key Input Interrupt Validity Select Bit	0 : $P10_4$ to $P10_7$ or $\overline{KI_0}$ to $\overline{KI_3}$ 1 : AN_4 to AN_7(1)	RW

NOTES:
1. Set the ILVL2 to ILVL0 bits in the KUPIC register to "000_2" (interrupt disabled) when changing the PSC_7 bit.
   Although the AN4 to AN7 pins can be used when this bit is set to "0", power consumption may increase.

Figure 24.14 PSC Register

Pull-Up Control Register 0(1)

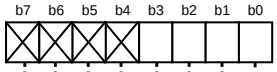


Symbol	Address	After Reset
PUR0	03F0$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
PU00	P0$_0$ to P0$_3$ Pull-Up	Pull-up setting for corresponding port 0 : Not pulled up 1 : Pulled up	RW
PU01	P0$_4$ to P0$_7$ Pull-Up		RW
PU02	P1$_0$ to P1$_3$ Pull-Up		RW
PU03	P1$_4$ to P1$_7$ Pull-Up		RW
PU04	P2$_0$ to P2$_3$ Pull-Up		RW
PU05	P2$_4$ to P2$_7$ Pull-Up		RW
PU06	P3$_0$ to P3$_3$ Pull-Up		RW
PU07	P3$_4$ to P3$_7$ Pull-Up		RW

NOTES:
1. Set each bit in the PUR0 register to "0" since P0 to P5 operate as the address bus in the memory expansion mode and microprocessor mode. Pull-up or no pull-up setting can be selected when using these ports as I/O ports.

Pull-Up Control Register 1(1)

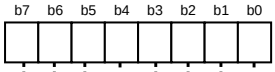


Symbol	Address	After Reset
PUR1	03F1$_{16}$	XXXX 0000$_2$

Bit Symbol	Bit Name	Function	RW
PU10	P4$_0$ to P4$_3$ Pull-Up	Pull-up setting for corresponding port 0 : Not pulled up 1 : Pulled up	RW
PU11	P4$_4$ to P4$_7$ Pull-Up		RW
PU12	P5$_0$ to P5$_3$ Pull-Up		RW
PU13	P5$_4$ to P5$_7$ Pull-Up		RW
____ (b7 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		___

NOTES:
1. Set each bit in the PUR1 register to "0" since P0 to P5 operate as the address bus in the memory expansion mode and microprocessor mode. Pull-up or no pull-up setting can be selected when using these ports as I/O ports.

Pull-Up Control Register 2



Symbol	Address	After Reset
PUR2	03DA$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
PU20	P6$_0$ to P6$_3$ Pull-Up	Pull-up setting for corresponding port 0 : Not pulled up 1 : Pulled up	RW
PU21	P6$_4$ to P6$_7$ Pull-Up		RW
PU22	P7$_2$ to P7$_3$ Pull-Up(1)		RW
PU23	P7$_4$ to P7$_7$ Pull-Up		RW
PU24	P8$_0$ to P8$_3$ Pull-Up		RW
PU25	P8$_4$ to P8$_7$ Pull-Up(2)		RW
PU26	P9$_0$ to P9$_3$ Pull-Up		RW
PU27	P9$_4$ to P9$_7$ Pull-Up		RW

NOTES:
1. P7$_0$ and P7$_1$ cannot be pulled up.
2. P8$_5$ cannot be pulled up.

Figure 24.15 PUR0 Register, PUR1 Register and PUR2 Register

Pull-Up Control Register 3

<144-pin package>

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
								PUR3	$03DB_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
PU30	$P10_0$ to $P10_3$ Pull-Up	Pull-up setting for corresponding port 0 : Not pulled up 1 : Pulled up	RW
PU31	$P10_4$ to $P10_7$ Pull-Up		RW
PU32	$P11_0$ to $P11_3$ Pull-Up		RW
PU33	$P11_4$ Pull-Up		RW
PU34	$P12_0$ to $P12_3$ Pull-Up		RW
PU35	$P12_4$ to $P12_7$ Pull-Up		RW
PU36	$P13_0$ to $P13_3$ Pull-Up		RW
PU37	$P13_4$ to $P13_7$ Pull-Up		RW

Pull-Up Control Register 3

<100-pin package>

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
0	0	0	0	0	0			PUR3	$03DB_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
PU30	$P10_0$ to $P10_3$ Pull-Up	Pull-up setting for corresponding port 0 : Not pulled up 1 : Pulled up	RW
PU31	$P10_4$ to $P10_7$ Pull-Up		RW
____ (b7 - b2)	Reserved Bit	Set to "0"	RW

Pull-Up Control Register 4(1)

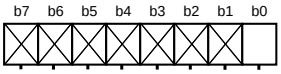
b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
X	X	X	X					PUR4	$03DC_{16}$	$XXXX\ 0000_2$

Bit Symbol	Bit Name	Function	RW
PU40	$P14_0$ to $P14_3$ Pull-Up	Pull-up setting for corresponding port 0 : Not pulled up 1 : Pulled up	RW
PU41	$P14_4$ to $P14_7$ Pull-Up		RW
PU42	$P15_0$ to $P15_3$ Pull-Up		RW
PU43	$P15_4$ to $P15_7$ Pull-Up		RW
____ (b7 - b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		___

NOTES:
1. Set the PUR4 register to "00_{16}" in the 100-pin package.

Figure 24.16 PUR3 Register and PUR4 Register

Port Control Register(1)



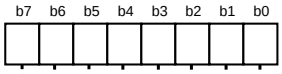
Symbol	Address	After Reset
PCR	$03FF_{16}$	XXXX $XXX0_2$

Bit Symbol	Bit Name	Function	RW
PCR0	Port P1 Control Bit	0 : CMOS output as P1 output format 1 : N-channel open drain output(2)	RW
——— (b7 - b1)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. Set the PUR0 bit to "0" since P1 operates as the data bus in memory expansion mode and microprocessor mode. When using the ports as I/O ports, CMOS port or N-channel open drain can be selected.
2. This function is designed, not to make port P1 a full open drain, but to turn off the P channel in the CMOS port.
   Absolute maximum rating of the input voltage is from -0.3V to V_{CC} + 3.0V.

Figure 23.17 PCR Register

Input Function Select Register



Symbol	Address	After Reset
IPS	0178_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
IPS0	Group 0 Input Pin Select Bit 0	Assigns each function of $INPC0_0$, $INPC0_1$/ISCLK0 and $INPC0_2$/ISRxD0 /$BE0_{IN}$ to the following ports. 0 : $P7_6$, $P7_7$, $P8_0$ 1 : $P15_0$, $P15_1$, $P15_2$	RW
IPS1	Group 1 Input Pin Select Bit 1	Assigns each function of $INPC1_1$ /ISCLK1 and $INPC1_2$/ISRxD1/$BE1_{IN}$ to the following ports. 0 : $P7_4$, $P7_5$ 1 : $P11_1$, $P11_2$	RW
IPS2	Port P15 Input Peripheral Function Select Bit	0 : Except AN15(1) 1 : AN15	RW
IPS3	CAN_{IN} Function Pin Select Bit	0 : $P7_7$ 1 : $P8_3$	RW
IPS4	ISRxD2/IE_{IN} Function Pin Select Bit	b5 b4 0 0 : $P7_1$ 0 1 : $P9_1$ 1 0 : $P13_5$ 1 1 : Do not set to this value	RW
IPS5			RW
IPS6	ISCLK2 Function Pin Select Bit	0 : $P6_4$ 1 : $P13_6$	RW
IPS7	ISRxD3 Function Pin Select Bit	0 : $P8_1$, $P8_2$ 1 : $P12_0$, $P12_2$	RW

NOTES:
1. Although $AN15_0$ to $AN15_7$ can be used when the IPS bit is set to "0", the power consumption may increase.

Figure 24.18 IPS Register

Table 24.1 Unassigned Pin Settings in Single-chip Mode

Pin Name	Setting
P0 to P15 (excluding P85)(1)	Enter input mode and connect each pin to VSS via a resistor (pull-down); or enter output mode and leave the pins open.
XOUT(2)	Leave pin open
$\overline{NMI}$(P85)	Connect pin to VCC via a resistor (pull-up)
AVCC	Connect pin to VCC
AVSS, VREF, BYTE	Connect pins to VSS

NOTES:
1. P11 to P15 are provided in the 144-pin package only.
2. When the external clock is applied to the XIN pin, set the pin as written above.

Table 24.2 Unassigned Pin Setting in Memory Expansion Mode and Microprocessor Mode

Pin Name	Setting
P6 to P15 (excluding P85)(1)	Enter input mode and connect each pin to VSS via a resistor (pull-down); or enter output mode and leave pins open.
$\overline{BHE}$, ALE, $\overline{HLDA}$, XOUT(2), BCLK	Leave pins open
$\overline{HOLD}$, $\overline{RDY}$, $\overline{NMI}$(P85)	Connect pins to VCC via a resistor (pull-up)
AVCC	Connect pin to VCC
AVSS, VREF	Connect pins to VSS

NOTES:
1. P11 to P15 are provided in the 144-pin package only.
2. When the external clock is applied to the XIN pin, set the pin as written above.

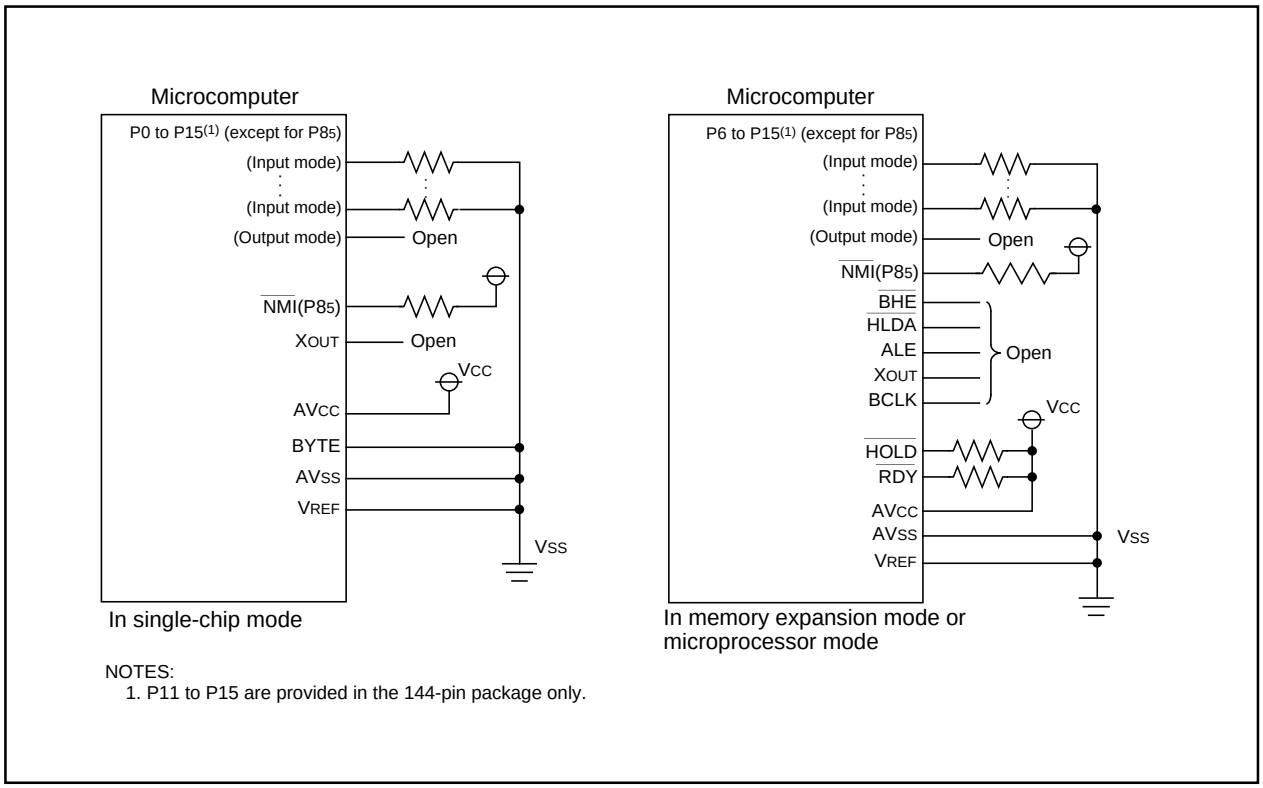


Figure 24.19 Unassigned Pin Handling

Table 24.3 Port P6 Peripheral Function Output Control

	PS0 Register	PSL0 Register
Bit 0	0: P60/CTS0/SS0 1: RTS0	Set to "0"
Bit 1	0: P61/CLK0 (input) 1: CLK0 (output)	Set to "0"
Bit 2	0: P62/RxD0/SCL0 (input) 1: Selected by the PSL0 register	0: SCL0 (output) 1: STxD0
Bit 3	0: P63/SRxD0/SDA0 (input) 1: TxD0/SDA0 (output)	Set to "0"
Bit 4	0: P64/CTS1/SS1/ISCLK2 (input) 1: Selected by the PSL0 register	0: RTS1 1: OUT21/ISCLK2(output)
Bit 5	0: P65/CLK1(input) 1: CLK1(output)	Set to "0"
Bit 6	0: P66/RxD1/SCL1 (input) 1: Selected by the PSL0 register	0: SCL1(output) 1: STxD1
Bit 7	0: P67/SRxD1/SDA1 (input) 1: TxD1/SDA1 (output)	Set to "0"

Table 24.4 Port P7 Peripheral Function Output Control

	PS1 Register	PSL1 Register	PSC Register(1)
Bit 0	0: P70/SRxD2/TA0OUT(input)/ SDA2(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: TA0OUT(output)	0: TxD2/SDA2(output) 1: OUTC20/ISTxD2/IEOUT
Bit 1	0: P71/TB5IN/TA0IN/RxD2/ISRxD2/IEIN/ SCL2(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: STxD2	0: SCL2(output) 1: OUTC22
Bit 2	0: P72/TA1OUT(input)/CLK2(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: TA1OUT(output)	0: CLK2(output) 1: V
Bit 3	0: P73/TA1IN/CTS2/SS2 1: Selected by the PSL1 register	0: Selected by the PSC register 1: V	0: RTS2 1: OUTC10/ISTxD1/BE1OUT
Bit 4	0: P74/INPC11/ISCLK1(input)/TA2OUT(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: W	0: TA2OUT(output) 1: OUTC11/ISCLK1(output)
Bit 5	0: P75/TA2IN/INPC12/ISRxD1/BE1IN 1: Selected by the PSL1 register	0: W 1: OUTC12	Set to "0"
Bit 6	0: P76/INPC00/TA3OUT(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: TA3OUT(output)	0: OUTC00/ISTxD0/BE0OUT 1: CAN0OUT
Bit 7	0: P77/TA3IN/CANIN/ISCLK0(input)/INPC01 1: OUTC01/ISCLK0(output)	Set to "0"	0: P104 to P107 or KI0 to KI3 1: AN4 to AN7 (No relation to P77)

NOTES:

1. Set the corresponding PSC_i bit to "0" when setting the PSL1_i bit (i=0 to 4, 6) to "1".

Table 24.5 Port P8 Peripheral Function Output Control

	PS2 Register	PSL2 Register
Bit 0	0: P80/INPC02/ISRxD0/BE0OUT/TA4OUT(input) 1: Selected by the PSL2 register	0: TA4OUT(output) 1: U
Bit 1	0: P81/TA4IN 1: Selected by the PSL2 register	0: U 1: OUTC32/ISTxD3
Bit 2	0: P82/INT0/ISRxD3 1: Selected by the PSL2 register	0: OUTC32 1: CANOUT
Bit 3 to 7	Set to "0"	

Table 24.6 Port P9 Peripheral Function Output Control

	PS3 Register	PSL3 Register
Bit 0	0: P90/TB0IN/CLK3(input) 1: CLK3(output)	Set to "0"
Bit 1	0: P91/TB1IN/RxD3/ISRxD2/SCL3(input)/IEIN 1: Selected by the PSL3 register	0: SCL3(output) 1: STxD3
Bit 2	0: P92/TB2IN/SRxD3/SDA3(input) 1: Selected by the PSL3 register	0: TxD3/SDA3(output) 1: OUTC20/ISTxD2/IEIN
Bit 3	0: P93/TB3IN/$\overline{CTS3}$/$\overline{SS3}$/DA0(output) 1: $\overline{RTS3}$	0: Except DA0 1: DA0
Bit 4	0: P94/TB4IN/$\overline{CTS4}$/$\overline{SS4}$/DA1(output) 1: $\overline{RTS4}$	0: Except DA1 1: DA1
Bit 5	0: P95/ANEX0/CLK4(input) 1: CLK4(output)	0: Except ANEX0 1: ANEX0
Bit 6	0: P96/SRxD4/ANEX1/SDA4(input) 1: TxD4/SDA4(output)	0: Except ANEX1 1: ANEX1
Bit 7	0: P97/RxD4/$\overline{ADTRG}$/SCL4(input) 1: Selected by the PSL3 register	0: SCL4(output) 1: STxD4

Table 24.7 Port P10 Peripheral Function Input Control

	PSC Register
Bit 7	0: P104 to P107 or $\overline{KI0}$ to $\overline{KI3}$ 1: AN4 to AN7

Table 24.8 Port P11 Peripheral Function Output Control

	PS5 Register
Bit 0	0: P110 1: OUTC10/ISTxD1/BE1OUT
Bit 1	0: P111/INPC11/ISCLK1(input) 1: OUTC11/ISCLK1(output)
Bit 2	0: P112/INPC12/ISRxD1/BE1IN 1: OUTC12
Bit 3	0: P113 1: OUTC13
Bit 4 to 7	Set to "0"

Table 24.9 Port P12 Peripheral Function Output Control

	PS6 Register
Bit 0	0: P120 1: OUTC30/ISTxD3
Bit 1	0: P121/ISCLK3(input) 1: OUTC31/ISCLK3(output)
Bit 2	0: P122/ISRxD3 1: OUTC32
Bit 3	0: P123 1: OUTC33
Bit 4	0: P124 1: OUTC34
Bit 5	0: P125 1: OUTC35
Bit 6	0: P126 1: OUTC36
Bit 7	0: P127 1: OUTC37

Table 24.10 Port P13 Peripheral Function Output Control

	PS7 Register
Bit 0	0: $P13_0$ 1: $OUTC2_4$
Bit 1	0: $P13_1$ 1: $OUTC2_5$
Bit 2	0: $P13_2$ 1: $OUTC2_6$
Bit 3	0: $P13_3$ 1: $OUTC2_3$
Bit 4	0: $P13_4$ 1: $OUTC2_0$/ISTxD2/IE_{OUT}
Bit 5	0: $P13_5$/ISRxD2/IE_{IN} 1: $OUTC2_2$
Bit 6	0: $P13_6$/ISCLK2(input) 1: $OUTC2_1$/ISCLK2(output)
Bit 7	0: $P13_7$ 1: $OUTC2_7$

Table 24.11 Port P14 Peripheral Function Output Control

	PS8 Register
Bit 0	0: $P14_0$ 1: $OUTC1_4$
Bit 1	0: $P14_1$ 1: $OUTC1_5$
Bit 2	0: $P14_2$/$INPC1_6$ 1: $OUTC1_6$
Bit 3	0: $P14_3$/$INPC1_7$ 1: $OUTC1_7$
Bit 4 to 7	Set to " 0"

Table 24.12 Port P15 Peripheral Function Output Control

	PS9 Register
Bit 0	0: $P15_0$/$INPC0_0$/$AN15_0$ 1: $OUTC0_0$/ISTxD0/$BE0_{OUT}$
Bit 1	0: $P15_1$/$INPC0_1$/$AN15_1$/ISCLK0(input) 1: $OUTC0_1$/ISCLK0(output)
Bit 2 to 3	Set to "0"
Bit 4	0: $P15_4$/$INPC0_4$/$AN15_4$ 1: $OUTC0_4$
Bit 4	0: $P15_5$/$INPC0_5$/$AN15_5$ 1: $OUTC0_5$
Bit 6 to 7	Set to " 0"

25. Flash Memory Version

Aside from the built-in flash memory, the flash memory version microcomputer has the same functions as the masked ROM version.

In the flash memory version, rewrite operations to the flash memory can be performed in three modes: CPU rewrite mode, standard serial I/O mode and parallel I/O mode.

Table 25.1 lists specifications of the flash memory version. See **Tables 1.1 and 1.2** for the items not listed in Table 25.1.

Table 25.1 Flash Memory Version Specifications

Item		Specification
Supply Voltage		4.2V to 5.5V (f(XIN) = 32MHz, no wait) 3.0V to 5.5V (f(XIN) = 20MHz, no wait)
Program and Erase Voltage		4.2V to 5.5V (through VDC), 3.0V to 3.6V (not through VDC) CPU clock=12.5MHz (1 wait state), CPU clock=6.25MHz (no wait)
Flash Memory Rewrite Mode		3 modes (CPU rewrite, standard serial I/O, parallel I/O)
Erase Block	User ROM Area	See Figure 25.1
	Boot ROM Area	1 block (8 Kbytes)(1)
Program Method		Per page (256 bytes)
Erase Method		All block erase, erase per block
Program and Erase Control Method		Software commands control programming and erasing on the flash memory
Protect Method		The lock bit protects each block in the flash memory
Number of Commands		8 commands
Program and Erase Endurance		100 cycles(3)
Data Retention		10 years
ROM Code Protection		Standard serial I/O mode and parallel I/O mode supported

NOTES:

1. The rewrite control program for standard serial I/O mode is stored in the boot ROM area before shipment. This space can be rewritten in parallel I/O mode only.

Table 25.2 Flash Memory Rewrite Mode Overview

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	Software command execution by CPU rewrites the user ROM area.	A dedicated serial programmer rewrites the user ROM area. Standard serial I/O mode 1: Clock synchronous serial I/O Standard serial I/O mode 2: UART	A dedicated parallel programmer rewrites the boot ROM area and user ROM area.
Space which can be Rewritten	User ROM area	User ROM area	User ROM area Boot ROM area
Operating Mode	Single-chip mode Memory expansion mode Boot mode	Boot mode	Parallel I/O mode
Programmer	None	Serial programmer	Parallel programmer

25.1 Memory Map

The flash memory contains a user ROM area, with space to store microcomputer operating programs in single-chip mode or memory expansion mode, and a separate 8-Kbyte boot ROM area. Figure 25.1 shows a block diagram of the flash memory.

The user ROM area is divided into several blocks, each of which can be protected (locked) from program and erase. The user ROM area can be rewritten in CPU rewrite, standard serial I/O and parallel I/O modes.

The boot ROM area is allocated in the same addresses as the user ROM area. It can only be rewritten in parallel I/O mode (refer to **25.5 Parallel I/O Mode**). A program in the boot ROM area is executed after a hardware reset occurs while an "H" signal is applied to the CNVSS and P50 pins and an "L" signal is applied to the P55 pin (refer to **25.1.1 Boot Mode**). A program in the user ROM area is executed after a hardware reset occurs while an "L" signal is applied to the CNVSS pin. Consequently, the boot ROM area cannot be read.

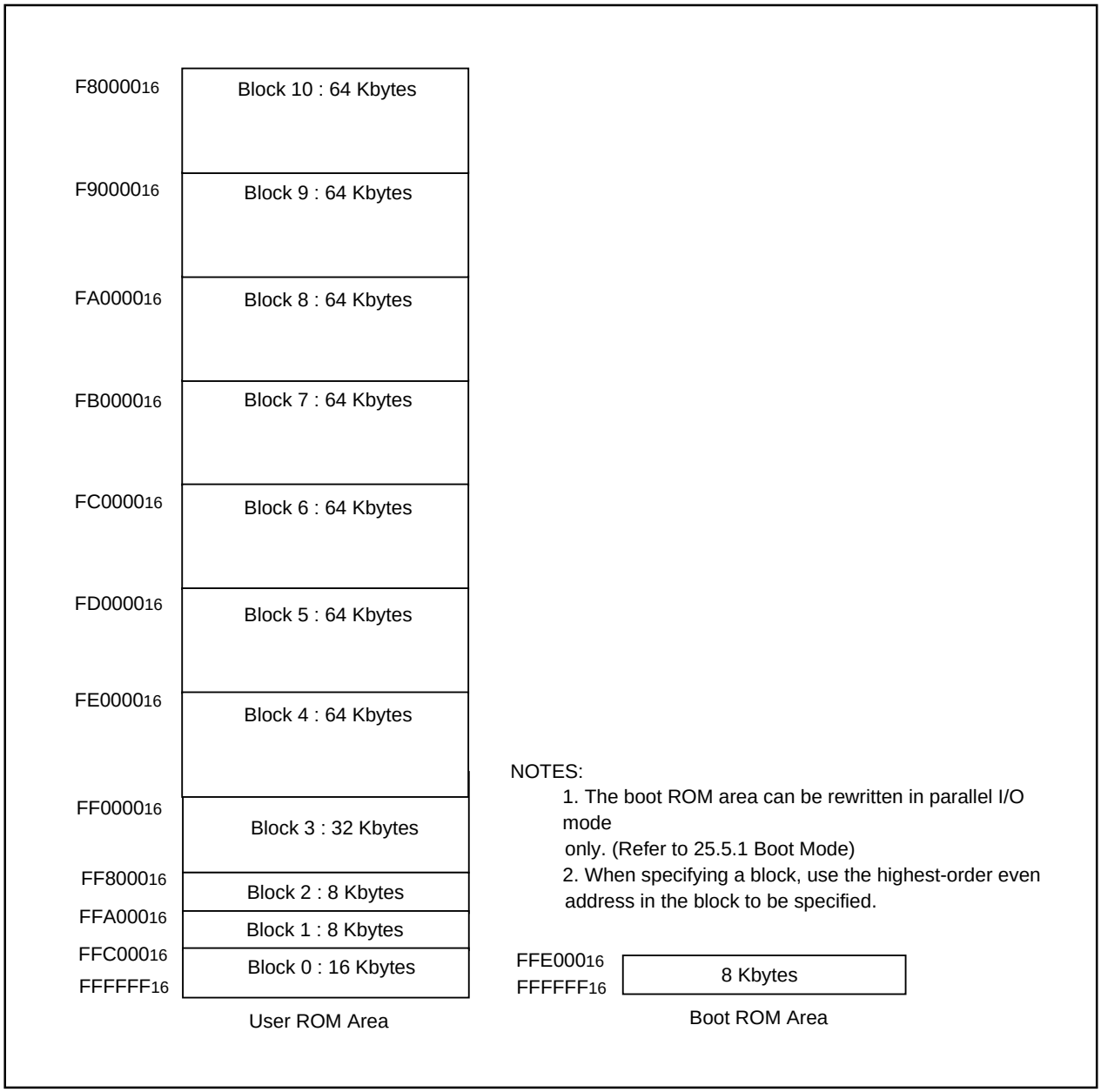


Figure 25.1 Flash Memory Block Diagram

25.1.1 Boot Mode

The microcomputer enters boot mode when a hardware reset is performed while an "H" signal is applied to the CNV_{SS} and $P5_0$ pins and an "L" signal is applied to the $P5_5$ pin. The program in the boot ROM area is executed.

In boot mode, the FMR05 bit in the FMR0 register selects access to either the boot ROM area or the user ROM area.

The rewrite control program for standard serial I/O mode (refer to **25.4 Standard Serial I/O Mode**) is stored in the boot ROM area before shipment.

The boot ROM area can be rewritten in parallel I/O mode only. If any rewrite control program using erase-write mode is written in the boot ROM area, the flash memory can be rewritten according to the system implemented.

25.2 Functions to Prevent the Flash Memory from Rewriting

The flash memory has a built-in ROM code protect function for parallel I/O mode and a built-in ID code check function for standard I/O mode to prevent the flash memory from reading or rewriting.

25.2.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from reading and rewriting in parallel I/O mode. Figure 25.2 shows the ROMCP register. The ROMCP register is located in the user ROM area.

The ROM code protect function is enabled when the ROMCP1 bit is set to 00_2". The ROM code protect function is disabled when the ROMCR bit is set to "00_2", regardless of the ROMCP1 bit setting.

Therefore, set the ROMCR bit to "11_2" and the ROMCP1 bit to "00_2" when setting up the ROM code protect function.

Once the ROM code protect function is enabled, the ROMCR bit cannot be changed in parallel I/O mode. Rewrite the ROMCR bit to "00_2" in standard serial I/O mode or CPU rewrite mode when disabling the ROM code protect function.

25.2.2 ID Code Check Function

Use the ID code check function in standard serial I/O mode. The ID code sent from the serial programmer is compared with the ID code written in the flash memory for a match. If the ID codes do not match, commands sent from the serial programmer are not accepted. However, if the four bytes of the reset vector are "$FFFFFFFF_{16}$", ID codes are not compared, and all commands are accepted.

The ID codes are 7-byte data stored consecutively, starting with the first byte, into addresses $0FFFFDF_{16}$, $0FFFFE3_{16}$, $0FFFFEB_{16}$, $0FFFFEF_{16}$, $0FFFFF3_{16}$, $0FFFFF7_{16}$ and $0FFFFFB_{16}$. Write a program with the ID codes set in these addresses to the flash memory.

ROM Code Protect Control Address(3)

b7	b6	b5	b4	b3	b2	b1	b0
				1	1	1	1

Symbol: ROMCP
Address: 0FFFFFF16
After Reset: FF16

Bit Symbol	Bit Name	Function	RW
——— (b3 - b0)	Reserved Bit	Set to "1"	RW
ROMCR	ROM Code Protect Reset Bit(1)	b5 b4 0 0 : Disables ROM code protection 0 1 : Enables the ROMCP bit 1 0 : Enables the ROMCP bit 1 1 : Enables the ROMCP bit	RW RW
ROMCP1	ROM Code Protect Level 1 Set Bit(2)	b7 b6 0 0 : Enables ROM code protection 0 1 : Enables ROM code protection 1 0 : Enables ROM code protection 1 1 : ROM code protection inactive	RW RW

NOTES:
1. When the ROMCR bit is set to "002", the ROM code protect level 1 is disabled. When the ROM code protect level 1 is enabled, the ROMCR bit cannot be changed in parallel I/O mode. Change the ROMCR bit in standard serial I/O mode, etc.
2. When the ROM code protect level 1 is enabled, the flash memory is protected against reading or rewriting in parallel I/O mode.
3. The ROMCP register can be written with the page program command.

Figure 25.2 ROMCP Register

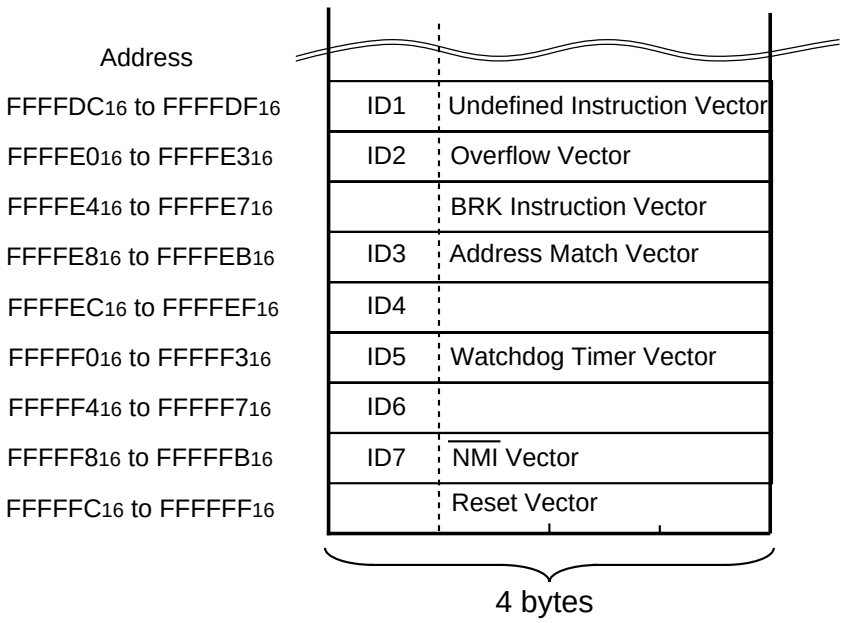


Figure 25.3 Address to Store ID Code

25.3 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten when the CPU executes software commands. The user ROM area can be rewritten with the microcomputer mounted on a board, without using a parallel or serial programmer,.

Write the rewrite control program to either the user ROM area or the boot ROM area, beforehand. No program in the flash memory can be executed in CPU rewrite mode. Therefore, transfer rewrite control program to an area other than flash memory (internal RAM, etc.), and execute.

CPU rewrite mode can be entered when the microcomputer is in single-chip, memory expansion, and boot mode.

Software commands, listed in Table 25.3, can be used in CPU rewrite mode. Refer to **25.3.3 Software Command** for details of each command.

Read or write commands and data from or to even addresses in the user ROM area, in 16-bit units. The 8 high-order bits (D_{15} to D_8) are ignored when writing command codes.

Table 25.3 Software Commands

Software Command	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
	Mode	Address	Data (D_{15} to D_0)	Mode	Address	Data (D_{15} to D_0)	Mode	Address	Data (D_{15} to D_0)
Read Array	Write	X	$xxFF_{16}$						
Read Status Register	Write	X	$xx70_{16}$	Read	X	SRD			
Clear Status Register	Write	X	$xx50_{16}$						
Page Program	Write	X	$xx41_{16}$	Write	WA	WD	Write	WA+2	WD
Block Erase	Write	X	$xx20_{16}$	Write	BA	$xxD0_{16}$			
Erase All Unlocked Block	Write	X	$xxA7_{16}$	Write	X	$xxD0_{16}$			
Lock Bit Program	Write	X	$xx77_{16}$	Write	BA	$xxD0_{16}$			
Read Lock Bit Status	Write	X	$xx71_{16}$	Read	BA	D_6			

SRD: Data in the SRD register (D_7 to D_0)
WA: Address to be written (Increment A_7 to A_0 by 2 from "00_{16}" to "FE_{16}".)
WD: 16-bit write data
BA: Highest-order block address (A_0 = 0)
D_6: Lock bit (D_6=1: unlock, D_6=0: locked)
X: Any even address in the user ROM area (A_0 = 0)
xx: 8 high-order bits of command code (ignored)

25.3.1 Flash Memory Control Register 0 (FMR0 Register)

Figure 25.4 shows the FMR0 register.

Flash Memory Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
X	X		0				

Symbol: FMR0 | Address: 0057$_{16}$ | After Reset: XX00 0001$_2$

Bit Symbol	Bit Name	Function	RW
FMR00	RY/$\overline{BY}$ Signal Status Bit	0 : BUSY (auto-writing, auto-erasing) 1 : READY (auto-write completed, auto-erase completed)	RO
FMR01	CPU Rewrite Mode Select Bit(1, 6)	0 : Disables CPU rewrite mode 1 : Enables CPU rewrite mode	RW
FMR02	Lock Bit Disable Bit(1, 3, 4)	0 : Enables the lock bit 1 : Disables the lock bit	RW
FMR03	Flash Memory Reset Bit(5)	By setting the bit to "1" just after setting it to "0", a flash memory access is interrupted to reset the flash memory control circuit	RW
——— (b4)	Reserved Bit	Set to"0"	RW
FMR05	User ROM Area Select Bit (Available in boot mode only)(2, 6)	0: Access the boot ROM area 1: Access the user ROM area	RW
——— (b7 - b6)	Noting is assigned. When write, set to "0". When read, its content is indeterminate.		—

NOTES:
1. Set this bit to "1" immediately after setting it to "0". Do not generate an interrupt or a DMA transfer between setting the bit to "0" and setting it to "1". Write "0" to this bit when setting it to "0".
2. Set the FMR05 bit by program in a space other than the flash memory.
3. When the FMR01 bit is set to "0", the FMR02 bit is also set to "0" simultaneously.
4. The FMR02 bit can be set only when the FMR01 bit is set to "1".
5. When the FMR01 bit is set "0", set the FMR03 bit to "0".
   Access the FMR03 bit when the FMR01 bit is set to "1".
6. Set the FMR05 bit while applying "H" to the $\overline{NMI}$ pin.

Figure 25.4 FMR0 Register

25.3.1.1 FMR00 Bit

The FMR00 bit indicates the write status machine (WSM) operation state during an auto write and auto erase operation. The FMR00 bit is set to "0" during an auto write or auto erase operation and is set to "1" when an auto write or auto erase operation is completed. The FMR00 bit changes while executing the page program, block erase, erase all unlocked block or lock bit program command. Determine whether the auto write or erase operation is completed by reading the FMR00 bit . The FMR00 bit is changed by the above commands only.

25.3.1.2 FMR01 Bit

Commands can be accepted when the FMR01 bit is set to "1" (CPU rewrite mode). To set the FMR01 bit to "1", set to "1" immediately after setting it to "0". To set the FMR01 bit to "0", set it to "0".

CPU rewrite mode is entered by setting the FMR01 bit to "1" and programs in the flash memory cannot be executed. Execute an instruction written to this bit in a space (internal RAM, etc.) other than the flash memory.

If a command for CPU rewrite mode is executed in boot mode, set the FMR05 bit to "1" (user ROM area access).

25.3.1.3 FMR02 Bit

The lock bit set for each block can be disabled by setting the FMR02 bit to "1" (lock bit disabled). (Refer to **25.3.3 Data Protect Function**.) The lock bit is enabled by setting the FMR02 bit to "0" (lock bit enabled). The FMR02 bit can be set when the FMR01 bit is set to "1". To set the FMR02 bit to "1", set it to "1" immediately after setting it to "0". To set the FMR02 bit to "0", set it to "0".

The FMR02 bit does not change the lock bit state, but disables the lock bit function. If the block erase or erase all unlocked block command is executed while the FMR02 bit is set to "1", the lock bit state changes "0" (locked) to "1" (unlocked) after command execution is completed.

25.3.1.4 FMR03 Bit

By setting the FMR03 bit to "0" following "1", access to the user ROM area is interrupted to reset the flash memory control circuit. The flash memory enters read array mode after reset. The FMR00 bit is set to "1" (READY) and the Status register is set to "80$_{16}$". (Refer to **25.3.2 Status Register**.)

When the FMR03 bit resets the flash memory control circuit during an auto write or auto erase operation, an auto write or auto erase operation is interrupted. Data in the block is invalid.

To set the FMR03 bit to "0", set it to "0" immediately after setting it to "1".

25.3.1.5 FMR05 Bit

The FMR05 bit selects the boot ROM or user ROM area in boot mode. Set to "0" to access (read) the boot ROM area or to "1" (user ROM access) to access (read, write or erase) the user ROM area. Execute an instruction written to the FMR05 bit in a space (internal RAM, etc.) other than the flash memory.

In modes other than boot mode, the user ROM area is accessed (read) regardless of the FMR05 bit setting.

25.3.2 Status Register

The write state machine (WSM) in the flash memory controls programming and erasing of the flash memory. The status register indicates whether or not the WSM is operating as expected, and whether or not a program or erase operation is completed as expected. Refer to **25.3.6 Full Status Check** for details on each error.

Table 25.4 lists the status register.

The status register can be read by the read status command (Refer to **25.3.5 Software Command**).

Table 25.4 Status Register

Symbol	Status Name	Definition	
		0	1
SR0 (D_0)	Reserved bit	-	-
SR1 (D_1)	Reserved bit	-	-
SR2 (D_2)	Reserved bit	-	-
SR3 (D_3)	Block status after program	Completed as expected	Error (excessive write error)
SR4 (D_4)	Program status	Completed as expected	Error (program error)
SR5 (D_5)	Erase status	Completed as expected	Error (erase error)
SR6 (D_6)	Reserved bit	-	-
SR7 (D_7)	Write state machine (WSM) status	BUSY	READY

D_7 to D_0 : These data bus are read when the read status register command is executed.

25.3.2.1 Block Status After Program (SR3)

The SR3 bit is set to "1" when a page program command execution is completed with an excessive write error. The SR3 bit is set to "0" when the clear status command is executed.

The SR3 bit is set to "0" after reset or after setting the FMR03 bit to "0" following "1".

25.3.2.2 Program Status (SR4)

The SR4 bit is set to "1" when a program error occurs while the page program or lock bit program command is being executed. The SR4 bit is set to "0" when the clear status command is executed.

The SR4 bit is set to "0" after reset or after setting the FMR03 bit to "0" following "1".

25.3.2.3 Erase Status (SR5)

The SR5 bit is set to "1" when an erase error occurs while the block erase or erase all unlocked block command is being executed. The SR5 bit is set to "0" when the clear status command is executed.

The SR5 bit is set to "0" after reset or after setting the FMR03 bit to "0" following "1".

25.3.2.4 Write State Machine (WSM) Status (SR7)

The SR7 bit indicates the WSM operation state. The SR7 bit is set to "0" during auto write or auto erase and to "1" when an auto write or auto erase operation is completed. The SR7 bit changes while the page program, block erase, erase all unlocked block or lock bit program command is being executed. The SR7 bit changes with the above commands only. The SR7 bit is set to "1" after reset or after setting the FMR03 bit to "0" following "1",.

The FMR00 bit indicates the WSM status. Read the FMR00 bit to determine whether the auto write or erase operation is completed.

25.3.3 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR02 bit to "0" (lock bit enabled). The lock bit individually protects (locks) each block against program and erase. This prevents data from being inadvertently written to or erased from the flash memory.

- When the lock bit status is set to "0", the block is locked (block is protected against program and erase).
- When the lock bit status is set to "1", the block is not locked (block can be programmed or erased).

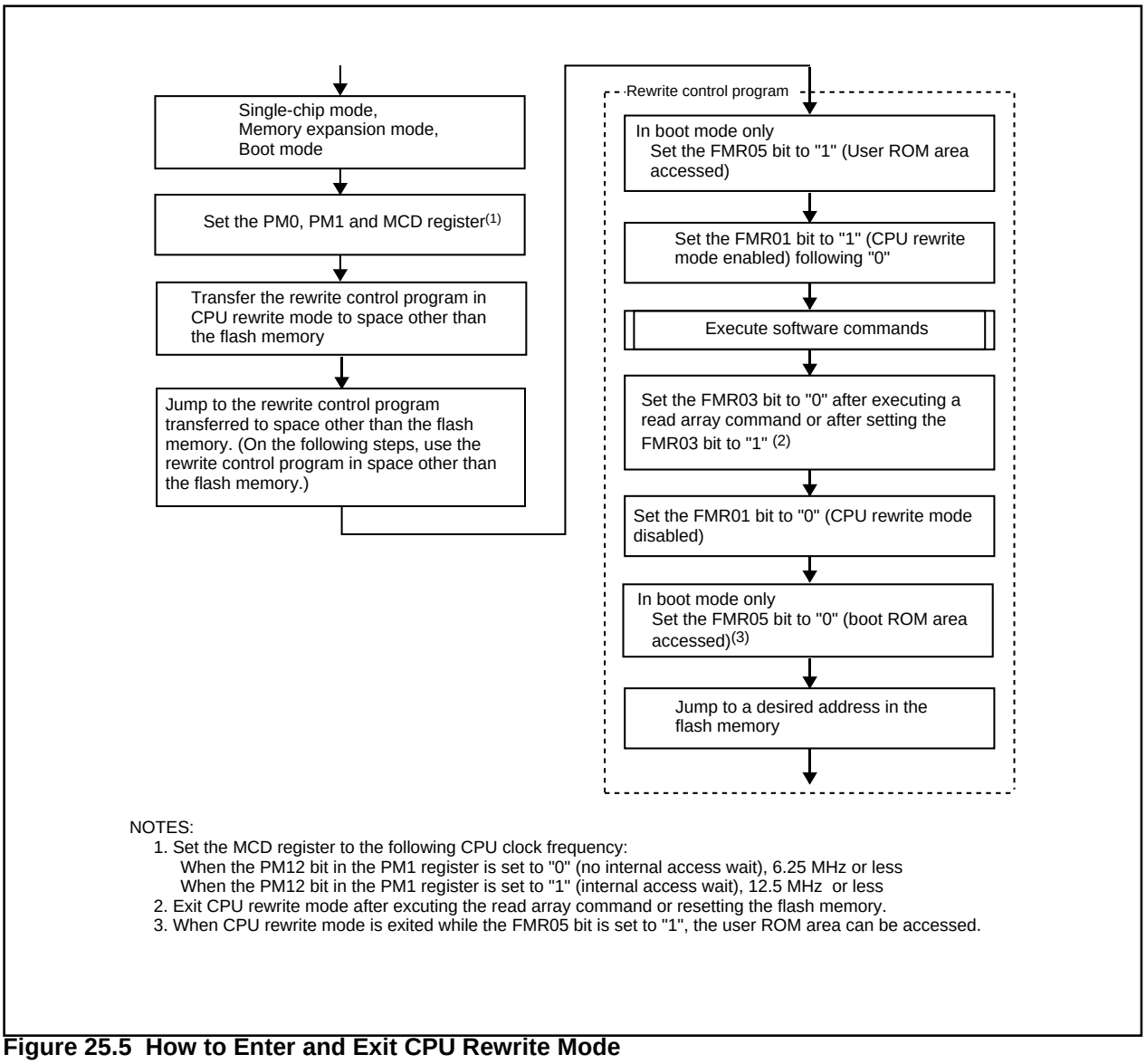
The lock bit status is set to "0" (locked) by executing the lock bit program command and to "1" (unlocked) by erasing the block. The lock bit status cannot be set to "1" by any commands.
The lock bit status can be read by the read lock bit status command.

The lock bit function is disabled by setting the FMR02 bit to "1". All blocks are unlocked. However, individual lock bit status remains unchanged. The lock bit function is enabled by setting the FMR02 bit to "0". Lock bit status is retained.
If the block erase or erase all unlocked block command is executed while the FMR02 bit is set to "1", the target block or all blocks are erased regardless of lock bit status. The lock bit status of each block is set to "1" after an erase operation has been completed.
Refer to **25.3.5 Software Commands** for details on each command.

25.3.4 How to Enter and Exit CPU Rewrite Mode

Figure 25.5 shows how to enter and exit CPU rewrite mode.

No program in the flash memory can be executed in CPU rewrite mode. Execute rewrite control program in a space other than the flash memory (internal RAM, etc.) after transferring the program to that space.



NOTES:
1. Set the MCD register to the following CPU clock frequency:
   When the PM12 bit in the PM1 register is set to "0" (no internal access wait), 6.25 MHz or less
   When the PM12 bit in the PM1 register is set to "1" (internal access wait), 12.5 MHz or less
2. Exit CPU rewrite mode after excuting the read array command or resetting the flash memory.
3. When CPU rewrite mode is exited while the FMR05 bit is set to "1", the user ROM area can be accessed.

Figure 25.5 How to Enter and Exit CPU Rewrite Mode

25.3.5 Software Commands

Read or write commands and data from or to even addresses in the user ROM area, in 16-bit units. When writing a command code, 8 high-order bits (D_{15} to D_8) are ignored.

25.3.5.1 Read Array Command

The read array command reads the flash memory.

Read array mode is entered by writing command code "xxFF$_{16}$" in the first bus cycle. Content of a specified address can be read after the next bus cycle.

The microcomputer remains in read array mode until another command is written. Therefore, contents from multiple addresses can be read consecutively.

25.3.5.2 Read Status Register Command

The read status register command reads the status register (refer to **25.3.7 Status Register** for details).

By writing command code "xx70$_{16}$" in the first bus cycle, the status register can be read in the second bus cycle. Read an even address in the user ROM area.

25.3.5.3 Clear Status Register Command

The clear status register command clears the status register. By writing "xx50$_{16}$" in the first bus cycle, the SR5 to SR3 bits in the status register (see Table 25.4) are set to "0".

25.3.5.4 Page Program Command

The page program command executes programs in 128-word (256-byte) units.

After writing command code "xx41$_{16}$" in the first bus cycle, write data to the 2nd through 129th bus cycles in 16-bit units. Increment by two, from "00$_{16}$" to "FE$_{16}$", the 8 low-order bits of the write address.

Auto write, programming and verification of data, is performed when 128 word data has been written.

Do not access the flash memory or execute the next command during auto write operation.

The FMR00 bit in the FMR0 register indicates whether an auto program operation is completed.

After an auto write operation is completed, the Status register indicates whether the auto write operation is completed as expected or not. (Refer to **25.3.6 Full Status Check**.)

Figure 25.6 shows a flow chart of the page program command programming. When programming a space which is already programmed, execute erase (block erase) before programming. If the page program command is executed to a space already programmed, no program error occurs but the page is indeterminate.

The lock bit can prevent blocks from being programmed. (Refer to **25.3.3 Data Protect Function**.)

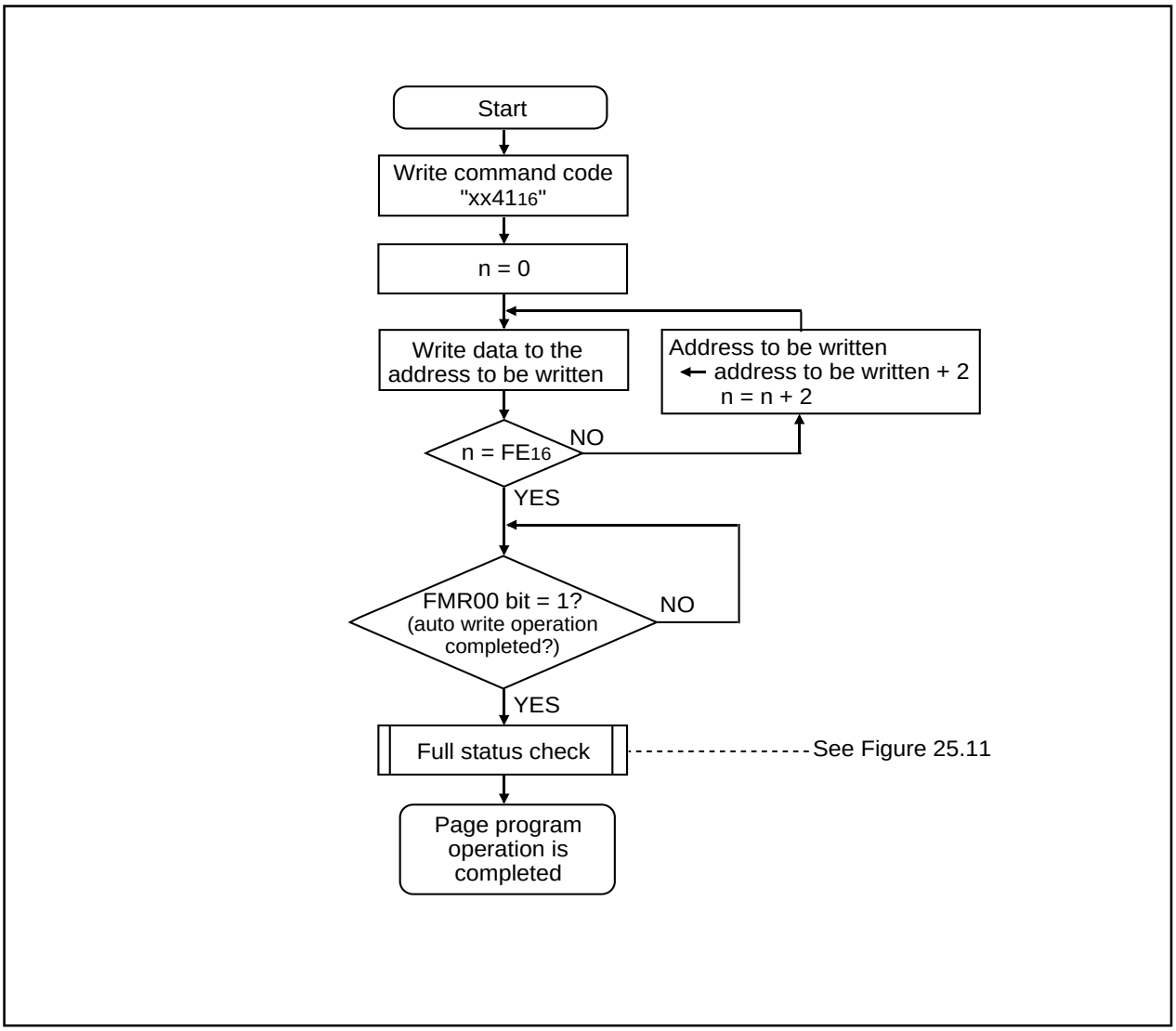


Figure 25.6 Program Command

25.3.5.5 Block Erase Command

The block erase command erases each block.

By writing "xx20$_{16}$" in the first bus cycle and "xxD0$_{16}$" to the highest-order even address of a block in the second bus cycle, an auto erase operation (erase and verify) starts in the specified block. Do not access the flash memory or execute the next command during auto erase operations.

The FMR00 bit in the FMR0 register indicates whether an auto erase operation has been completed.

After the completion of an auto erase operation, the Status register indicates whether or not the auto erase operation has been completed as expected. (Refer to **25.3.6 Full Status Check**.)

Figure 25.7 shows a flow chart of the block erase command programming.

The lock bit prevents blocks from being erased. (Refer to **25.3.6 Data Protect Function**.)

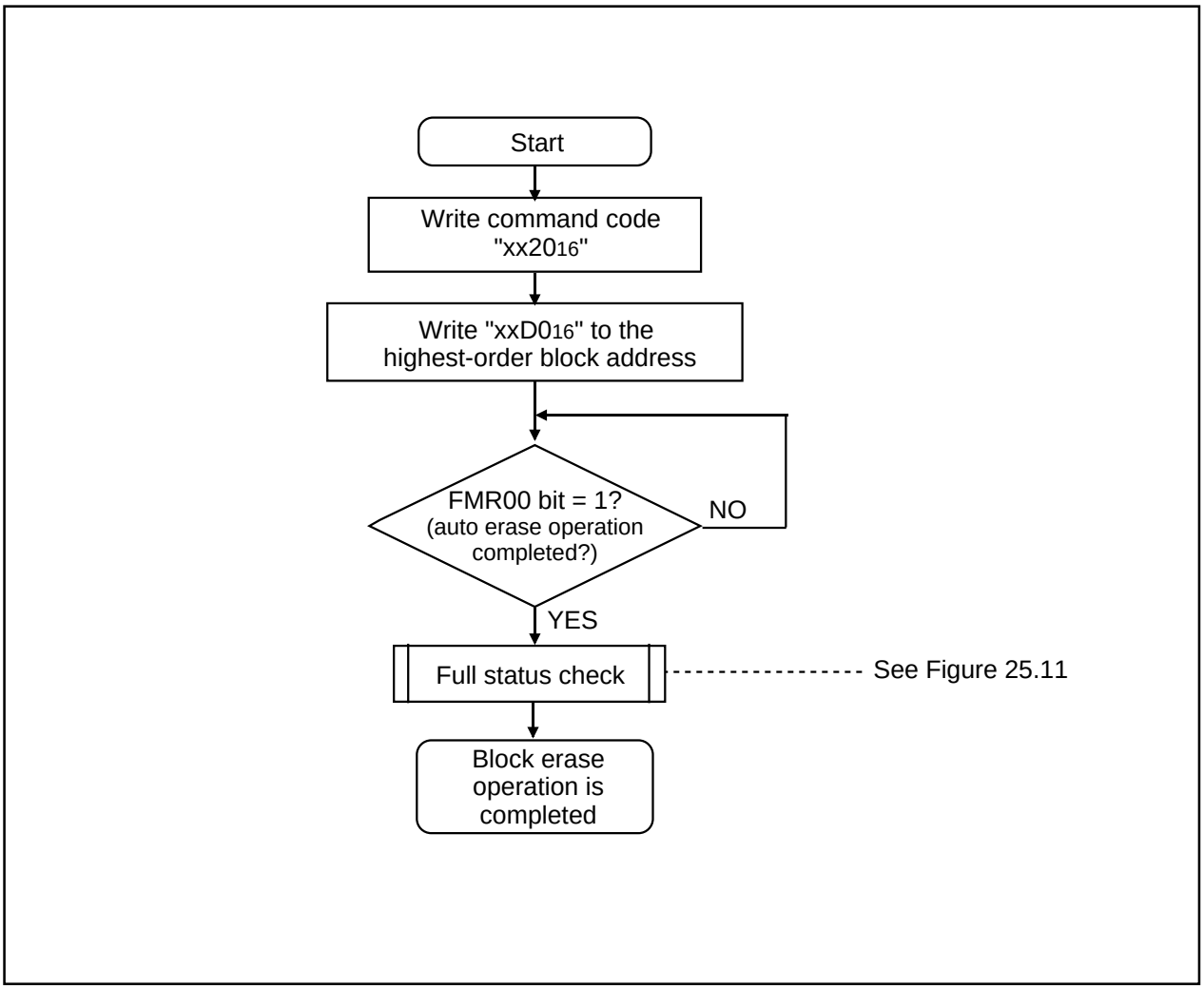


Figure 25.7 Block Erase Command

25.3.5.6 Erase All Unlocked Block Command

By writing "xxA7$_{16}$" in the first bus cycle and "xxD0$_{16}$" in the second bus cycle, an auto erase (erase and verify) operation will run in all blocks. Do not access the flash memory or execute the next command during auto erase operations.

The FMR00 bit in the FMR0 register indicates whether an auto erase operation is completed.

After the completion of an auto erase operation, the Status register indicates whether or not the auto erase operation is completed as expected.

Figure 25.8 shows a flow chart of the erase all unlocked block command programming.

The lock bit can protect each block from being erased. (Refer to **25.3.6 Data Protect Function**.)

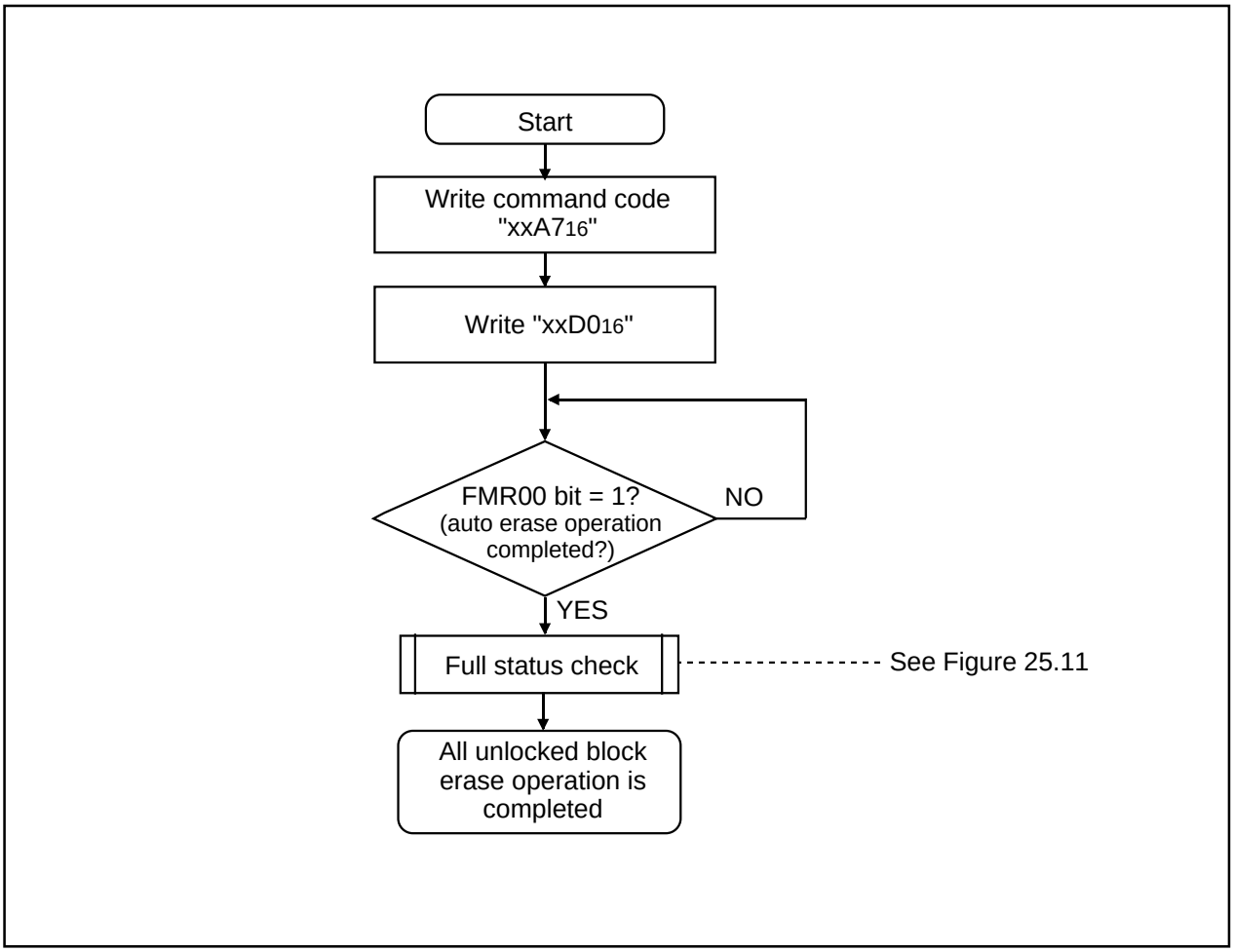


Figure 25.8 Erase All Unlocked Block Command

25.3.5.7 Lock Bit Program Command

The lock bit program command sets the lock bit for a specified block to "0" (locked).
By writing "xx77$_{16}$" in the first bus cycle and "xxD0$_{16}$" to the highest-order even address of a block in the second bus cycle, auto write operation starts, and the lock bit for the specified block is set to "0".
Do not access the flash memory or execute the next instructions during the lock bit program operation.
The FMR00 bit in the FMR0 register indicates whether or not the lock bit program operation has been completed. After the completion of a lock bit program operation, the Status register indicates whether or not the operation has been completed as expected. (Refer to **25.3.6 Full Status Check**.)
Figure 25.9 shows a flow chart of the lock bit program command programming.
Refer to **25.3.6 Data Protect Function** for details on how to set the lock bit function to "0" (unlocked).

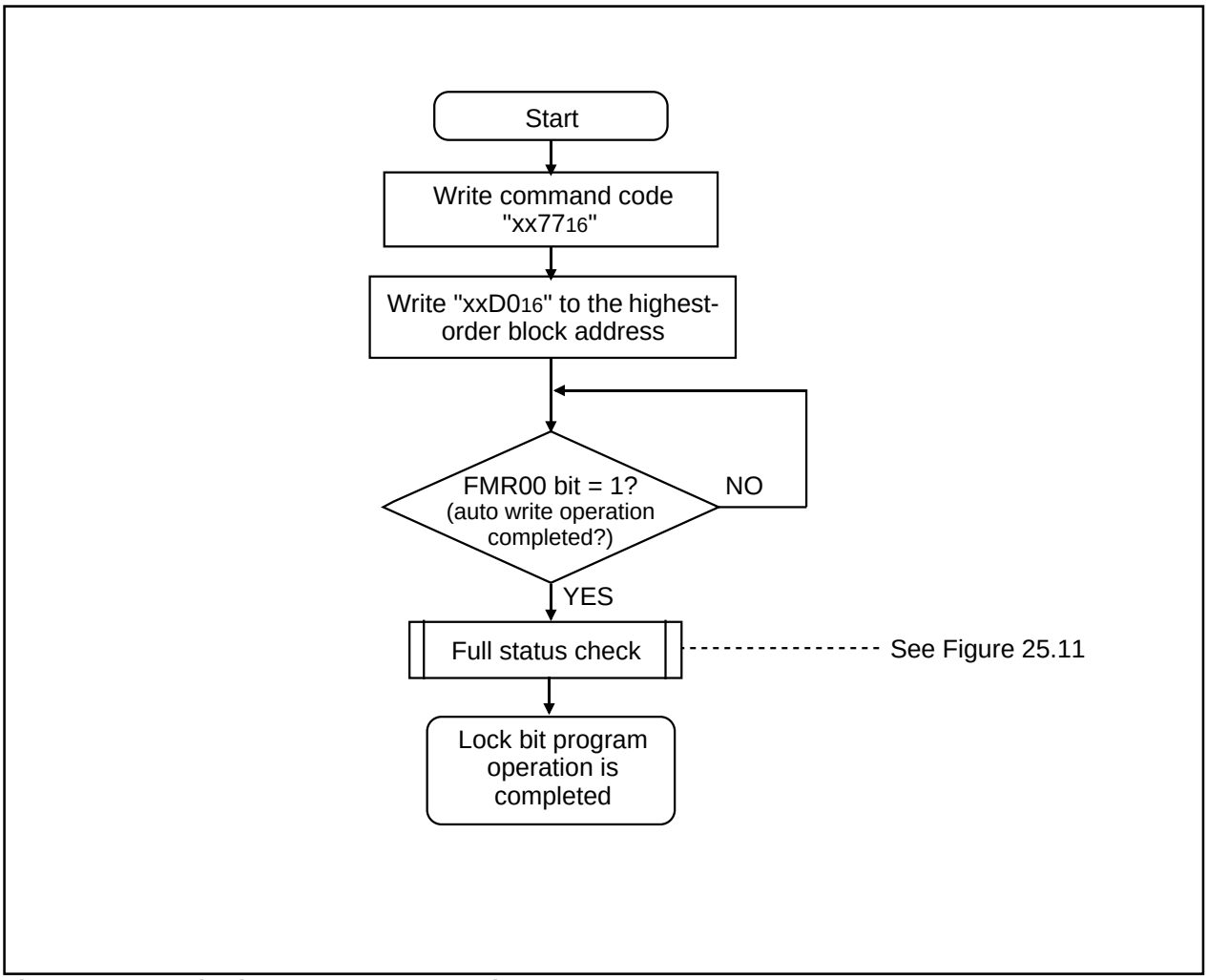


Figure 25.9 Lock Bit Program Command

25.3.5.8 Read Lock Bit Status Command

The read lock bit status command reads the lock bit state of a specified block.

By writing "xx71$_{16}$" in the first bus cycle and reading the highest-order address (however, A_0=0) of a block in the second bus cycle, the lock bit state information of a specified block is read out to the data bus (D_6).

Figure 25.10 shows a flow chart of the read lock bit status command programming.

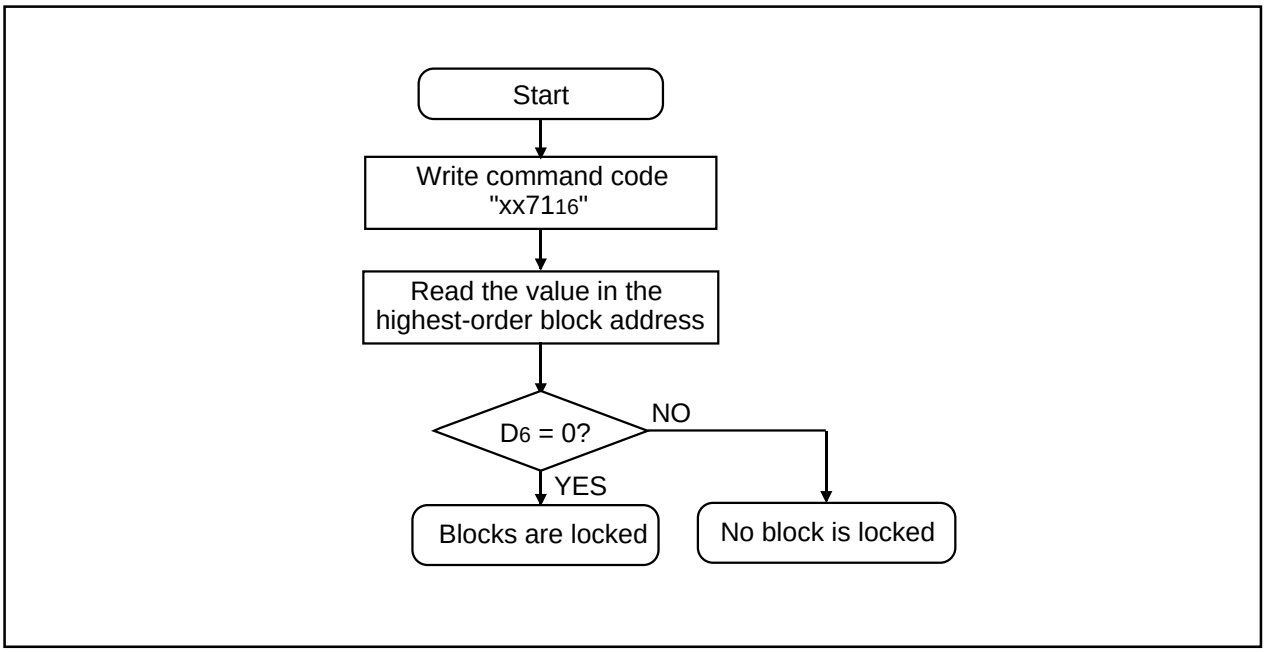


Figure 25.10 Read Lock Bit Status Command

25.3.6 Full Status Check

If an error occurs when a program or erase operation is completed, the SR3 to SR5 bits in the status register are set to "1", indicating a specific error. Therefore, execution results can be confirmed by checking these bits (full status check).

Table 25.5 lists errors and status register state. Figure 25.12 shows a flow chart of the full status check and handling procedure for each error.

Table 25.5 Errors and Status Register State

Status Register			Error	Error Occurrence Conditions
SR5	SR4	SR3		
1	1	0	Command sequence error	• An incorrect command is written • A value other than "xxD0$_{16}$" or "xxFF$_{16}$" is written in the second bus cycle of the lock bit program, block erase or erase all unlocked block command(1)
1	0	0	Erase error	• The block erase command is executed on a locked block2 • The block erase or erase all unlocked block command is executed on an unlock block but the erase operation is not completed as expected
0	1	0	Program error	• The page program command is executed in a locked block(2) • The page program command is executed in an unlocked block but the program operation is not completed as expected • The lock bit program command is executed but the program operation is not completed as expected
0	0	1	Excessive write error	Excessive write occurs after the page program command is executed

NOTES:

1. The flash memory enters read array mode when command code "xxFF$_{16}$" is written in the second bus cycle of these commands. The command code written in the first bus cycle becomes invalid.
2. If the FMR02 bit is set to "1" (lock bit disabled), no error occurs even under the conditions listed above.

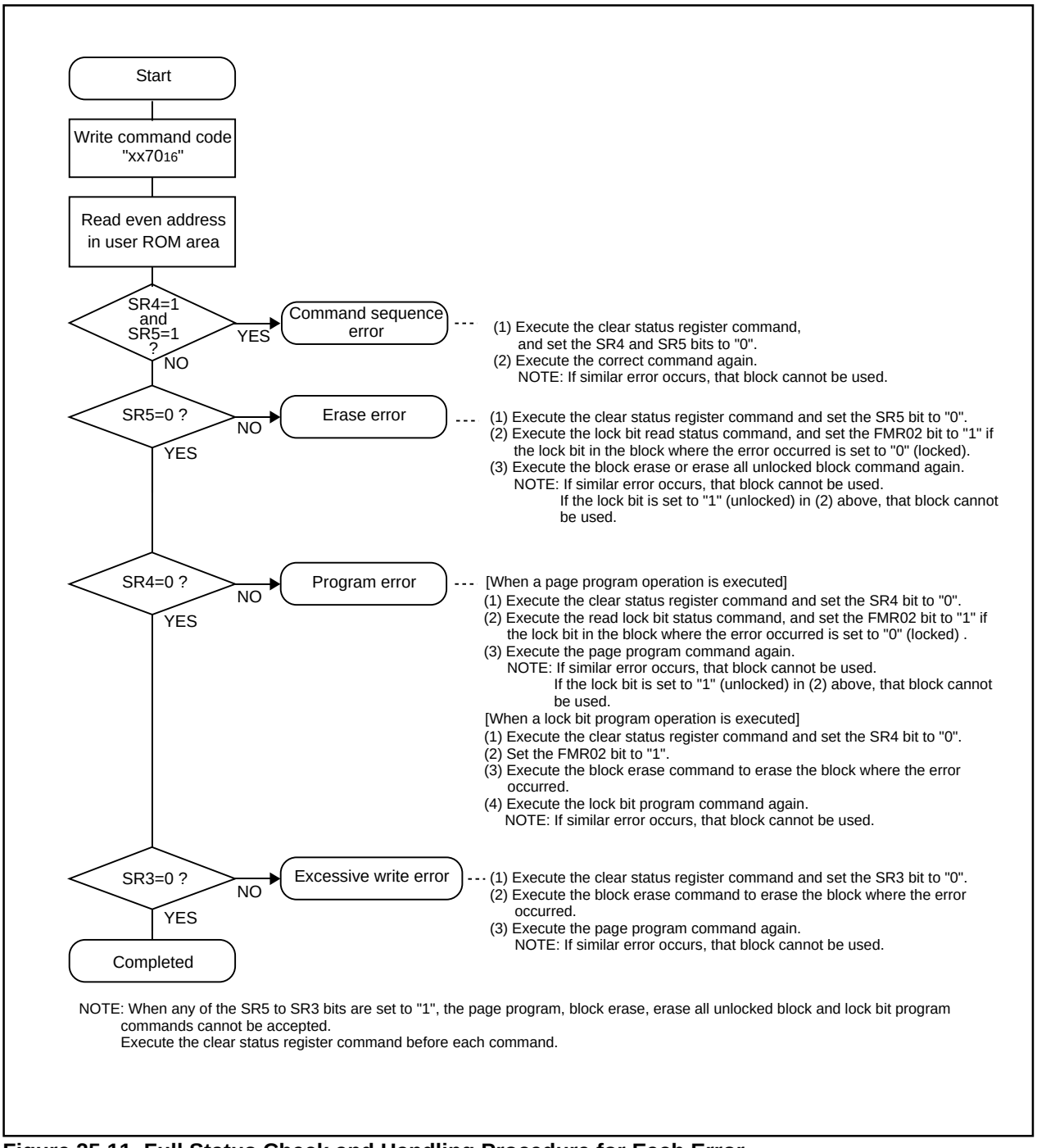


Figure 25.11 Full Status Check and Handling Procedure for Each Error

25.3.7 Precautions in CPU Rewrite Mode

25.3.7.1 Operating Speed

Set the MCD register to the following CPU clock before entering CPU rewrite mode .
When the PM12 bit in the PM register is set to "0" (no wait state), 6.25MHz or less
When the PM12 bit in the PM register is set to "1" (wait state), 12.5MHz or less

25.3.7.2 Prohibited Instructions

In CPU rewrite mode, programs cannot be executed, nor can interrupt vectors be read in the flash memory. Execute the rewrite control program after the program is transferred to a space other than the flash memory. (See **Figure 25.5**.)
The following instructions cannot be used because the CPU tries to read data in the flash memory: the UND instruction, INTO instruction, JMPS instruction, JSRS instruction and BRK instruction.

25.3.7.3 Interrupts

- To use interrupts having vectors in a relocatable vector table, the vectors must be relocated to the RAM area.
- The $\overline{\text{NMI}}$ and watchdog timer interrupts are available since the FMR01 is forcibly reset when either interrupt occurs. Allocate the jump addresses for each interrupt service routine and write to the fixed vector table. Flash memory rewrite operation is aborted when the $\overline{\text{NMI}}$ or watchdog timer interrupt occurs. Execute the rewrite program again after exiting the interrupt routine.
- The address match interrupt is not available since the CPU tries to read data in the flash memory.

25.3.7.4 Reading and Writing Commands and Data

Read or write 16-bit commands and data from or to even addresses in the user ROM area.

25.3.7.5 Reset

Reset is always enabled.

25.3.7.6 Access Prohibited

Write the FMR01 bit and FMR05 bit in a space other than the flash memory.

25.3.7.7 How to Access

To set the FMR01 bit and FMR02 bits to "1", set to "1" immediately after setting to "0". Do not generate an interrupt or a DMA transfer between the instruction to set to the bits to "1" and the instruction to set the bits to "0". Set the FMR01 bit to "1" after an "H" signal is applied to the P8$_5$/$\overline{\text{NMI}}$ pin.

25.3.7.8 Rewriting in the User ROM Area

If the supply voltage drops while in CPU rewrite mode, when rewriting the block where the rewrite control program is stored, the flash memory cannot be rewritten because the rewrite control program is not correctly rewritten. If this error occurs, rewrite the user ROM area while in standard serial I/O mode or parallel I/O mode.

25.4 Standard Serial I/O Mode

In standard serial I/O mode, the serial programmer supporting the M32C/83 group can be used to rewrite the flash memory user ROM area, while the microcomputer is mounted on a board. For more information about the serial programmer, contact your serial programmer manufacturer. Refer to the user's manual included with your serial programmer for instructions.

Standard serial I/O mode includes:

- Standard serial I/O mode 1 (clock synchronous)
- Standard serial I/O mode 2 (clock asynchronous)

25.4.1 Pin Function

Table 25.6 lists pin descriptions (flash memory standard serial I/O mode). Figures 2.12 to 25.14 show pin connections in serial I/O mode.

25.4.2 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer matches those written in the flash memory. (Refer to **25.2 Functions to Prevent Flash Memory from Rewriting**.)

Table 25.6 Pin Description (Flash Memory Standard Serial I/O Mode)

Symbol	Function	I/O Type	Description
VCC VSS	Power Supply Input	I	Apply 4.2 V to 5.5 V to the VCC pin Apply 0 V to the VSS pin
CNVSS	CNVSS	I	Connect this pin to VCC
$\overline{\text{RESET}}$	Reset Input	I	Reset input pin. Apply 20 or more clock cycles to the XIN pin while "L" is applied to the $\overline{\text{RESET}}$ pin.
XIN XOUT	Clock Input Clock Output	I O	Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use the external clock, input the clock from XIN and leave XOUT open.
BYTE	BYTE Input	I	Connect this pin to VSS or VCC
AVCC AVSS	Analog Power Supply Input	I I	Connect AVCC to VCC Connect AVSS to VSS
VREF	Reference Voltage Input	I	Reference voltage input pin for the A/D converter.
P00 to P07	Input Port P0	I	Apply "H" or "L" to this pin, or leave open
P10 to P17	Input Port P1	I	Apply "H" or "L" to this pin, or leave open
P20 to P27	Input Port P2	I	Apply "H" or "L" to this pin, or leave open
P30 to P37	Input Port P3	I	Apply "H" or "L" to this pin, or leave open
P40 to P47	Input port P4	I	Apply "H" or "L" to this pin, or leave open
P50	$\overline{\text{CE}}$ Input	I	Apply "H" to this pin.
P55	$\overline{\text{EPM}}$ Input	I	Apply "L" to this pin.
P51 to P54 P56, P57	Input Port P5	I	Apply "H" or "L" to this pin, or leave open
P60 to P63	Input Port P6	I	Apply "H" or "L" to this pin, or leave open
P64	BUSY Output	O	Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Program running check monitor
P65	SCLK Input	I	Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Apply "L" to this pin
P66	RxD	I	Serial data input pin
P67	TxD	O	Serial data output pin(1)
P70 to P77	Input Port P7	I	Apply "H" or "L" to this pin, or leave open
P80 to P84 P86, P87	Input Port P8	I	Apply "H" or "L" to this pin, or leave open
P85	$\overline{\text{NMI}}$ Input	I	Connect this pin to VCC
P90 to P97	Input Port P9	I	Apply "H" or "L" to this pin, or leave open
P100 to P107	Input Port P10	I	Apply "H" or "L" to this pin, or leave open
P110 to P114(2)	Input Port P11	I	Apply "H" or "L" to this pin, or leave open
P120 to P127(2)	Input Port P12	I	Apply "H" or "L" to this pin, or leave open
P130 to P137(2)	Input Port P13	I	Apply "H" or "L" to this pin, or leave open
P140 to P146(2)	Input Port P14	I	Apply "H" or "L" to this pin, or leave open
P150 to P157(2)	Input Port P15	I	Apply "H" or "L" to this pin, or leave open

NOTES:

1. In standard serial I/O mode 1, apply an "L" signal to the TxD pin while applying "L" to the RESET pin. Connect P67 to VSS via a resistor. P67 becomes a data output pin after reset. Adjust the value of the pull-down resistor on your system so as not to affect data transfer.
2. These pins are provided in the 144-pin package only.

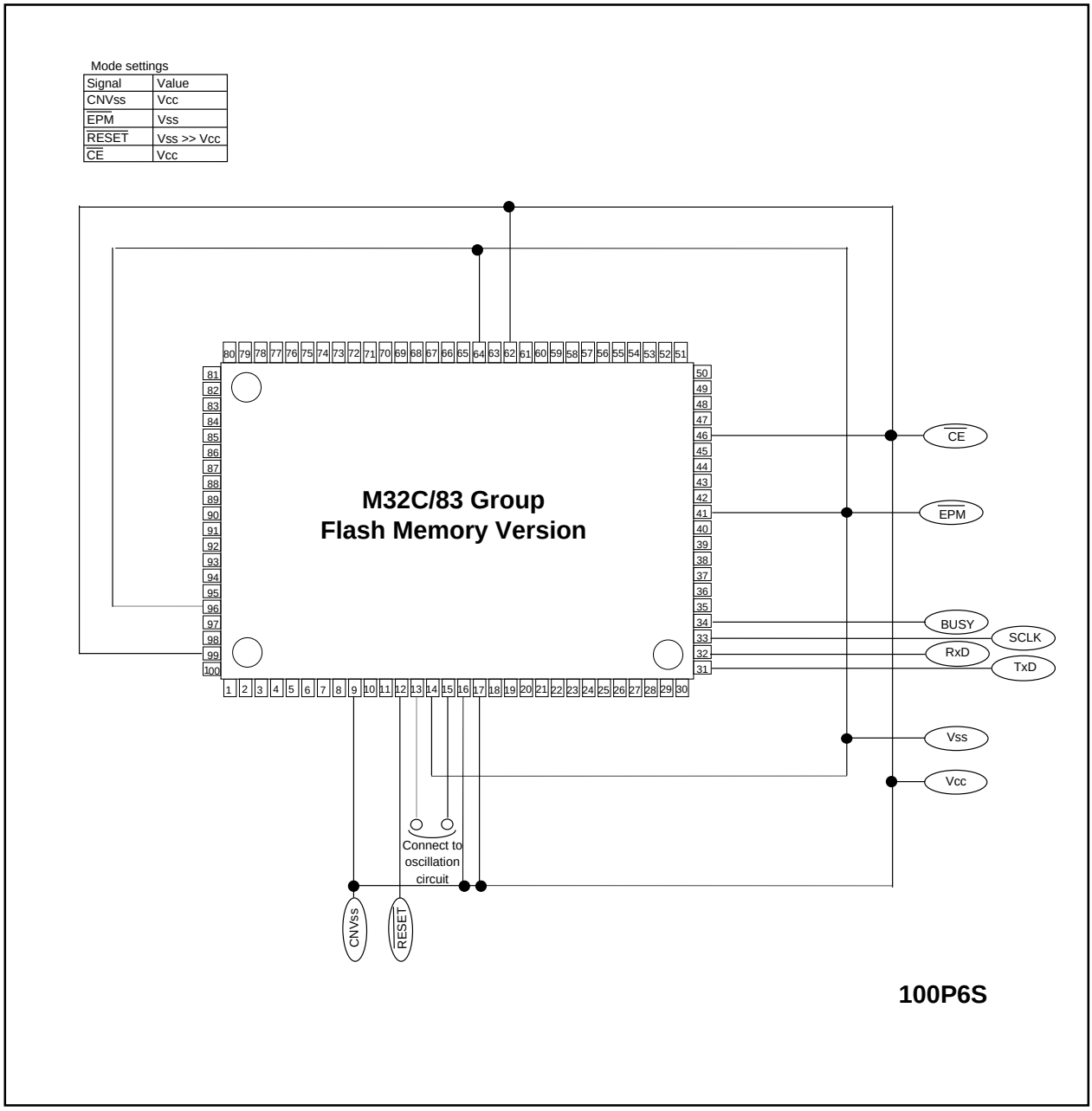


Figure 25.12 Pin Connections in Standard Serial I/O Mode (1)

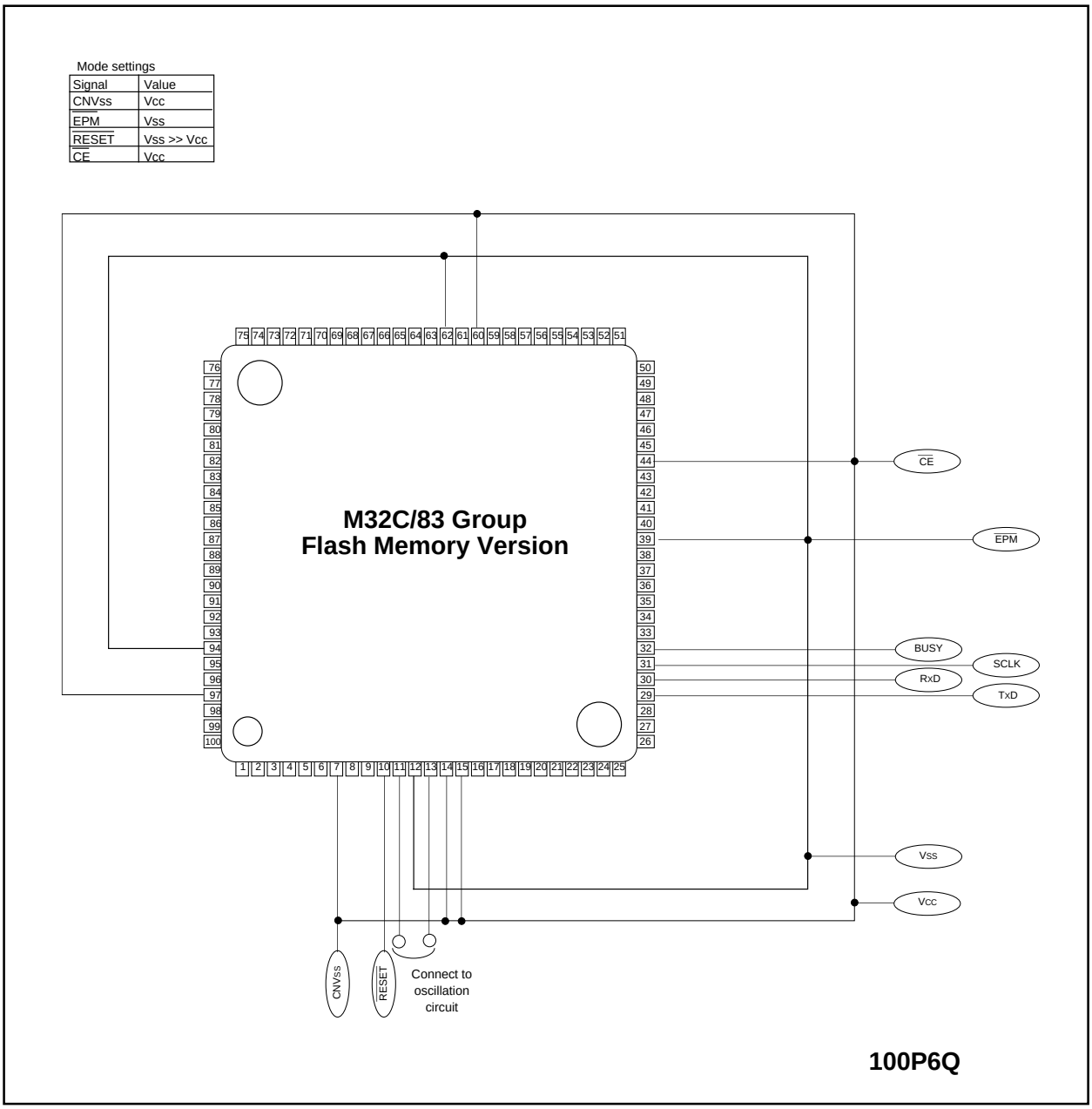


Figure 25.13 Pin Connections in Standard Serial I/O Mode (2)

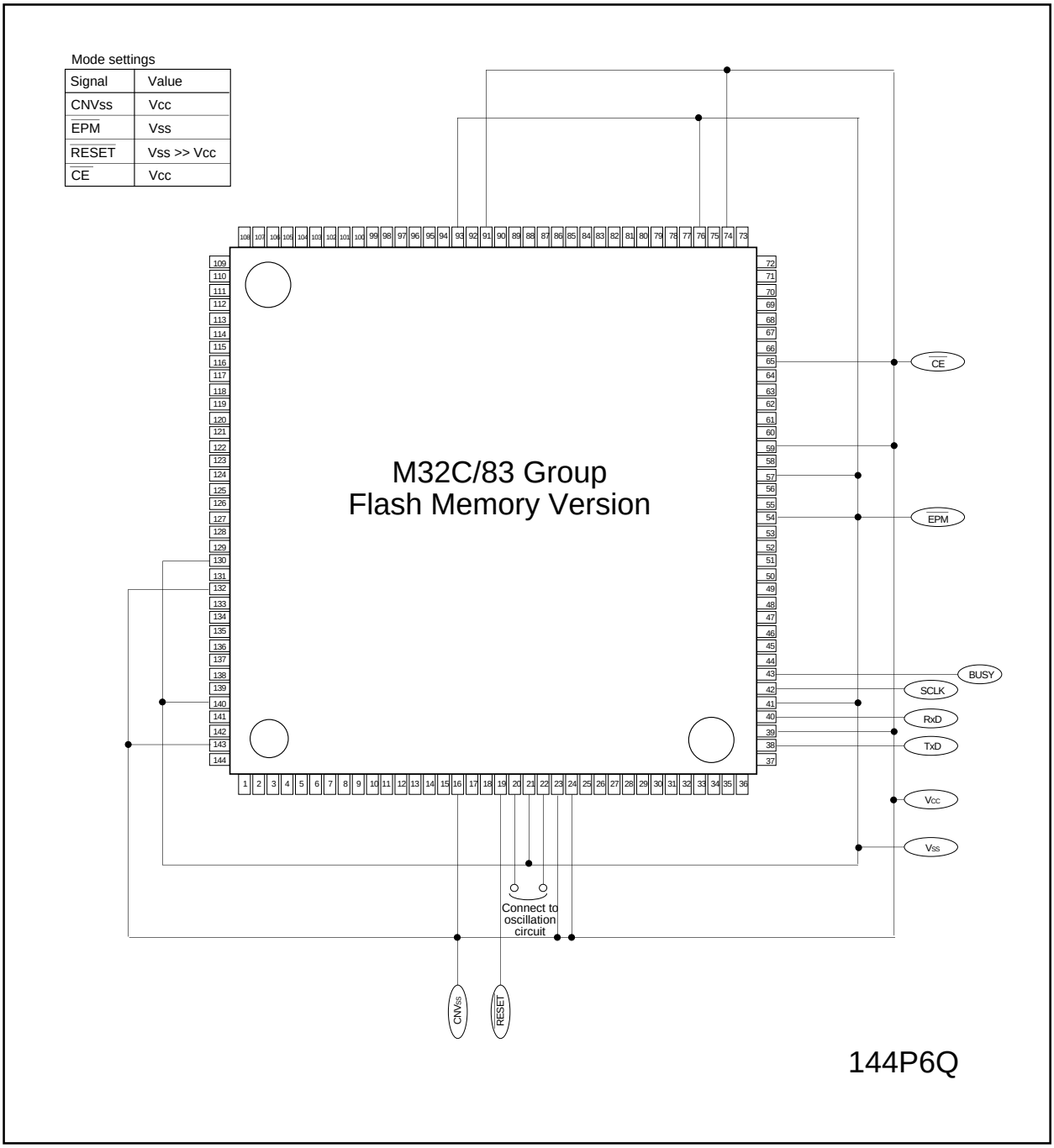


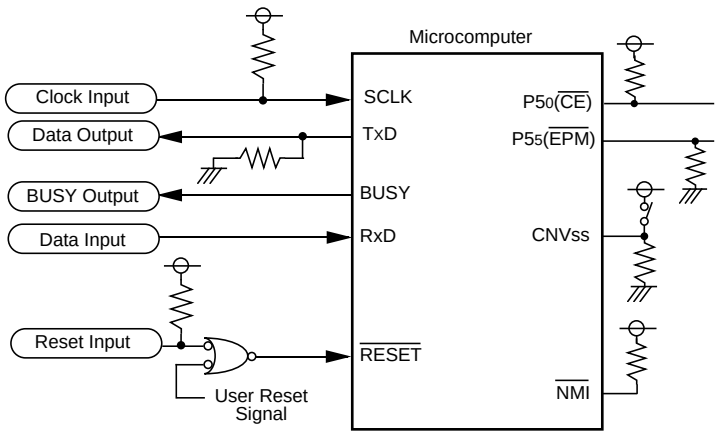
Figure 25.14 Pin Connections in Standard Serial I/O Mode (3)

25.4.3 Precautions in Standard Serial I/O Mode

- Serial I/O mode cannot be used after boot ROM area is written in parallel I/O mode.
- If an user reset signal becomes "L" in serial I/O mode, break connection between the user reset signal and the $\overline{\text{RESET}}$ pin by using, for example, a jumper selector.

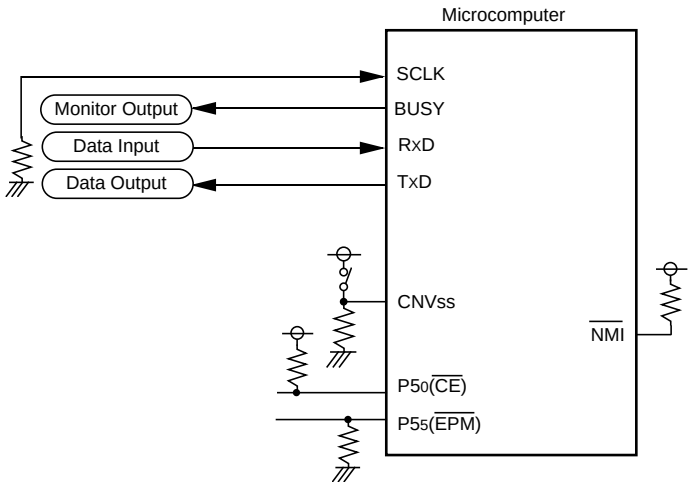
25.4.4 Circuit Application in Standard Serial I/O Mode

Figure 25.15 shows an example of a circuit application in standard serial I/O mode 1. Figure 25.16 shows an example of a circuit application in serial I/O mode 2. Refer to the user's manual of your serial programmer to handle pins controlled by the serial programmer.



NOTES:
1. Control pins and external circuitry vary with serial programmer. Refer to the user's manual included with the serial programmer.
2. In this example, a selector is used to switch between single-chip mode and standard serial I/O mode.
3. In standard serial I/O mode 1, if the user reset signal becomes "L" while in serial I/O mode, break connection between the user reset signal and the RESET pin using, for example, a jumper selector.

Figure 25.15 Circuit Application in Standard Serial I/O Mode 1



NOTES:
1. In this example, a selector is used to switch between single-chip mode and standard serial I/O mode.

Figure 25.16 Circuit Application in Standard Serial I/O Mode 2

25.5 Parallel I/O Mode

In parallel I/O mode, the user ROM area and the boot ROM area (see Figure 25.1) can be rewritten by a parallel programmer supporting the M32C/83 Group. Contact your parallel programmer manufacturer for more information on the parallel programmer. Refer to the user's manual included with your parallel programmer for instructions.

25.5.1 Boot ROM Area

Within the boot ROM area, 8K bytes equal one block.
The rewrite control program in standard serial I/O mode is written in the boot ROM area before shipment. Do not rewrite the boot ROM area if using a serial programmer.
In parallel I/O mode, the boot ROM area is allocated to addresses $0FFE000_{16}$ to $0FFFFFF_{16}$. Rewrite only this address range when rewriting the boot ROM area. (Do not access addresses other than addresses $0FFE000_{16}$ to $0FFFFFF_{16}$.)

25.5.2 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten in parallel I/O mode. (Refer to **25.2 Functions to Prevent Flash Memory from Rewriting**.)

25.5.3 Precautions on Parallel I/O Mode

Standard serial I/O mode cannot be used if rewriting the boot ROM area in parallel I/O mode, . (Refer to **25.4 Standard Serial I/O Mode**.)

26. Electrical Characteristics

Table 26.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC}	Supply Voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
AV_{CC}	Analog Supply Voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$		-0.3 to 6.0	V
V_O	Output Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}		-0.3 to V_{CC}+0.3	V
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating Ambient Temperature			-20 to 85	° C
Tstg	Storage Temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package.

Table 26.2 Recommended Operating Conditions (V_{CC} = 3.0V to 5.5V at Topr = – 20 to 85°C)

Symbol	Parameter			Standard			Unit
				Min	Typ	Max	
V_{CC}	Supply Voltage (Through VDC)			3.0	5.0	5.5	V
	Supply Voltage (Not through VDC)			3.0	3.3	3.6	V
AV_{CC}	Analog Supply Voltage				V_{CC}		V
V_{SS}	Supply Voltage				0		V
AV_{SS}	Analog Supply Voltage				0		V
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$[3], $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4], X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		0.8V_{CC}		V_{CC}	V
		$P7_0$, $P7_1$		0.8V_{CC}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)		0.8V_{CC}		V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)		0.5V_{CC}		V_{CC}	V
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$[3], $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4], X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		0		0.2V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)		0		0.2V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)		0		0.16V_{CC}	V
$I_{OH(peak)}$	Peak Output High ("H") Current[2]	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4]				-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current[1]	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4]				-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current[2]	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4]				10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current[1]	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4]				5.0	mA
$f(X_{IN})$	Main Clock Input Frequency	Through VDC	V_{CC}=4.2 to 5.5V	0		32	MHz
			V_{CC}=3.0 to 4.3V	0		20	MHz
		Not through VDC	V_{CC}=3.0 to 3.6	0		20	MHz
$f(X_{CIN})$	Sub Clock Oscillation Frequency				32.768	50	kHz

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be -80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P6, $P7_2$ to $P7_7$, $P8_0$ to $P8_4$, P12 and P13 must be -80mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply to $P8_7$ used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

V_{CC}=5V

Table 26.3 Electrical Characteristics (V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr= –20 to 85°C, f(X_{IN})=30MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-5mA	3.0			V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-200µA	4.7			
		X_{OUT}	I_{OH}=-1mA	3.0			V
		X_{COUT}	No load applied		3.3		V
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=5mA			2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=200µA			0.45	V
		X_{OUT}	I_{OL}=1mA			2.0	V
		X_{COUT}	No load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V	30	50	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			10		MΩ
V_{RAM}	RAM Standby Voltage	Through VDC		2.5			V
I_{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(X_{IN})=32 MHz, square wave, no division		41	58	mA
			f(X_{IN})=30 MHz, square wave, no division		38	54	mA
			f(X_{CIN})=32 kHz, with a wait state, Topr=25° C		470		µA
			Topr=25° C when the clock stops		0.4	20	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

V_{CC}=5V

Table 26.4 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5V, Vss = AV_{SS} = 0V at Topr = –20 to 85°C, f(X_{IN}) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min	Typ	Max	
-	Resolution	V_{REF}=V_{CC}				10	Bits
INL	Integral Nonlinearity Error	V_{REF}=V_{CC}=5V	AN_0 to AN_7 AN_{EX0}, AN_{EX1}			±3	LSB LSB
			External op-amp connection mode			±7	LSB LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	V_{REF}=V_{CC}		8		40	kΩ
t_{CONV}	10-bit Conversion Time			2.1			µs
t_{CONV}	8-bit Conversion Time			1.8			µs
t_{SAMP}	Sample Time			0.2			µs
V_{REF}	Reference Voltage			2		V_{CC}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.

Table 26.5 D/A Conversion Characteristics (V_{CC} = V_{REF} = 4.2 to 5.5V, V_{SS} = AV_{SS} = 0V at Topr = –20 to 85°C, f(X_{IN}) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter not being used is set to "00$_{16}$". The resistor ladder in the A/D converter is exclued. I_{VREF} flows even if the VCUT bit in the ADiCON1 register is set to "0" (no V_{REF} connection).

Table 26.6 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:
1. V_{CC}= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at Topr= 0 to 60° C, unless otherwise specified

VCC=5V

Timing Requirements (VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.7 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External Clock Input Cycle Time	33		ns
tw(H)	External Clock Input High ("H") Pulse Width	13		ns
tw(L)	External Clock Input Low ("L") Pulse Width	13		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 26.8 Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min	Max	
tac1(RD-DB)	Data Input Access Time (RD standard, with no wait state)		(Note 1)	ns
tac1(AD-DB)	Data Input Access Time (AD standard, CS standard, with no wait state)		(Note 1)	ns
tac2(RD-DB)	Data Input Access Time (RD standard, with a wait state)		(Note 1)	ns
tac2(AD-DB)	Data Input Access Time (AD standard, CS standard, with a wait state)		(Note 1)	ns
tac3(RD-DB)	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac3(AD-DB)	Data Input Access Time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac4(RAS-DB)	Data Input Access Time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAS-DB)	Data Input Access Time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAD-DB)	Data Input Access Time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
tsu(DB-BCLK)	Data Input Setup Time	26		ns
tsu(RDY-BCLK)	$\overline{RDY}$ Input Setup Time	26		ns
tsu(HOLD-BCLK)	$\overline{HOLD}$ Input Setup Time	30		ns
th(RD-DB)	Data Input Hold Time	0		ns
th(CAS-DB)	Data Input Hold Time	0		ns
th(BCLK-RDY)	$\overline{RDY}$ Input Hold Time	0		ns
th(BCLK-HOLD)	$\overline{HOLD}$ Input Hold Time	0		ns
td(BCLK-HLDA)	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequecncy. Insert a wait state or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \text{ (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states)}$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns] \text{ (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states)}$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \text{ (m=3 with 2 wait states and m=5 with 3 wait states)}$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \text{ (n=5 with 2 wait states and n=7 with 3 wait states)}$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \text{ (m=3 with 1 wait state and m=5 with 2 wait states)}$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \text{ (n=1 with 1 wait state and n=3 when 2 wait states)}$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns] \text{ (l=1 with 1 wait state and l=2 with 2 wait states)}$$

VCC=5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.9 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	40		ns

Table 26.10 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	200		ns

Table 26.11 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 26.12 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 26.13 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

VCC=5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.14 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 26.15 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width	200		ns

Table 26.16 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width	200		ns

Table 26.17 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ Input Cycle Time (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Pulse Width	125		ns

Table 26.18 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Pulse Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Set Up Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 26.19 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Pulse Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Pulse Width	250		ns

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.20 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 26.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-2		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-3		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.21 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 26.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-2		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-3		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9 \times n}{f(BCLK)} - 20 \quad [ns]$$ (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)

$$t_{h(WR-DB)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \quad [ns]$$ (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.22 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 26.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		(Note 1)		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-AD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-3		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time (BCLK standard)		-2		ns
$t_{d(AD-ALE)}$	ALE Signal Output Delay Time (address standard)		(Note 1)		ns
$t_{h(ALE-AD)}$	ALE Signal Output Hold Time (address standard)		(Note 1)		ns
$t_{dz(RD-AD)}$	Address Output High-Impedance Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{d(AD-ALE)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(ALE-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.23 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting the DRAM Space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Row Address Output Delay Time	See Figure 26.1		18	ns
$t_{h(BCLK-AD)}$	Row Address Output Hold Time (BCLK standard)		-3		ns
$t_{d(BCLK-CAD)}$	Column Address Output Delay Time			18	ns
$t_{h(BCLK-CAD)}$	Column Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RAS-RAD)}$	Row Address Output Hold Time after RAS Output		(Note 1)		ns
$t_{d(BCLK-RAS)}$	RAS Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-RAS)}$	RAS Output Hold Time (BCLK standard)		-3		ns
t_{RP}	RAS High ("H") Hold Time		(Note 1)		ns
$t_{d(BCLK-CAS)}$	CAS Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-CAS)}$	CAS Output Hold Time (BCLK standard)		-3		ns
$t_{d(BCLK-DW)}$	DW Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-DW)}$	DW Output Hold Time (BCLK standard)		-5		ns
$t_{su(DB-CAS)}$	CAS Output Setup Time after DB Output		(Note 1)		ns
$t_{h(BCLK-DB)}$	DB Signal Output Hold Time (BCLK standard)		-7		ns
$t_{su(CAS-RAS)}$	CAS Output Setup Time before RAS Output (refresh)		(Note 1)		ns

NOTES:

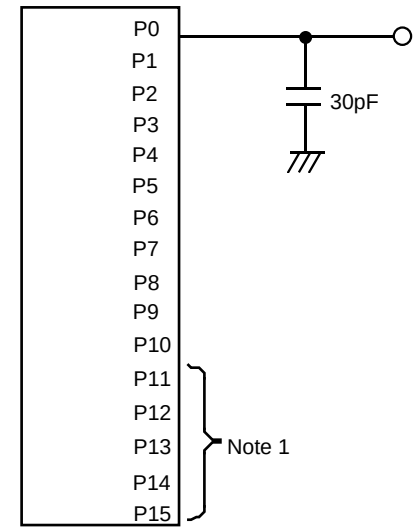
1. Values can be obtained from the following equation, according to BCLK frequency.

$$t_{h(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{su(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{su(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$



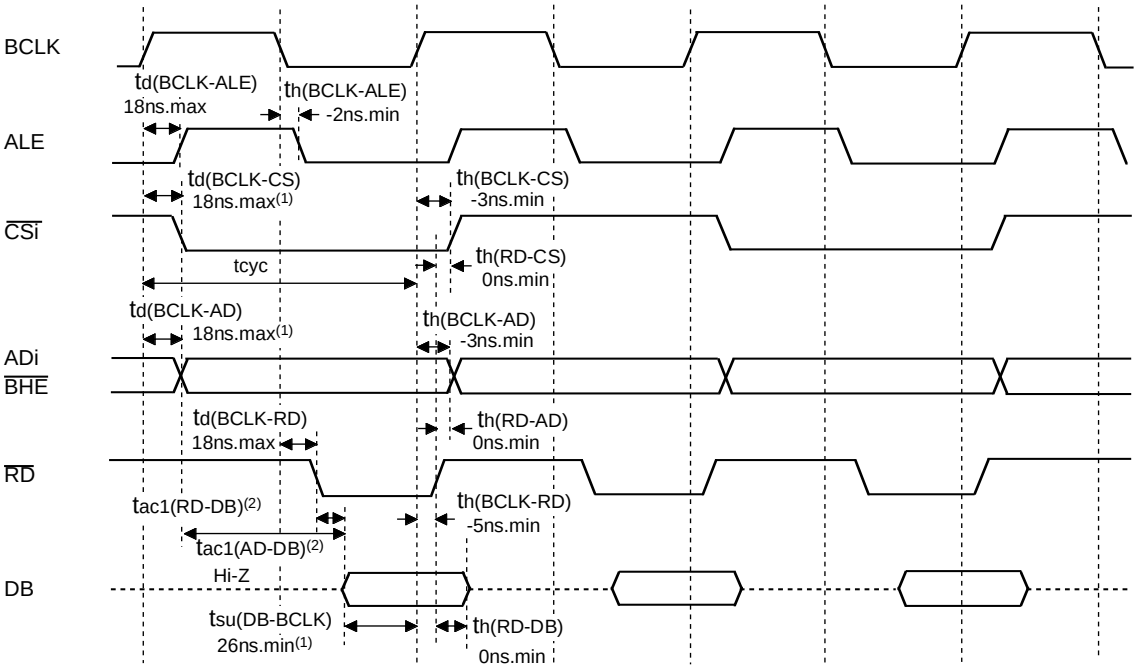
NOTES:
1. P11 to P15 are provided in the 144-pin package only.

Figure 26.1 P0 to P15 Measurement Circuit

Vcc=5V

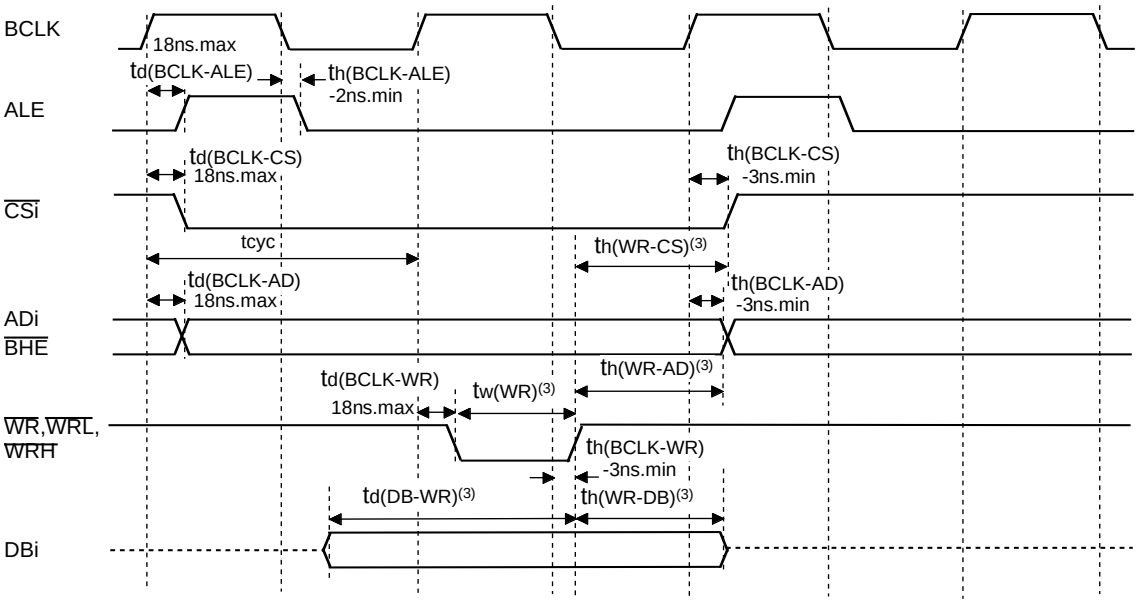
Memory Expansion Mode and Microprocessor Mode (with no wait state)

Read Timing



NOTES:
1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:
   $t_{ac1(RD-DB)}$=(tcyc/2-35)ns.max
   $t_{ac1(AD-DB)}$=(tcyc-35)ns.max

Write Timing (written in 2 cycles with no wait state)



NOTES:
3. Varies with operation frequency:
   $t_{d(DB-WR)}$=(tcyc-20)ns.min
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2-15)ns.min

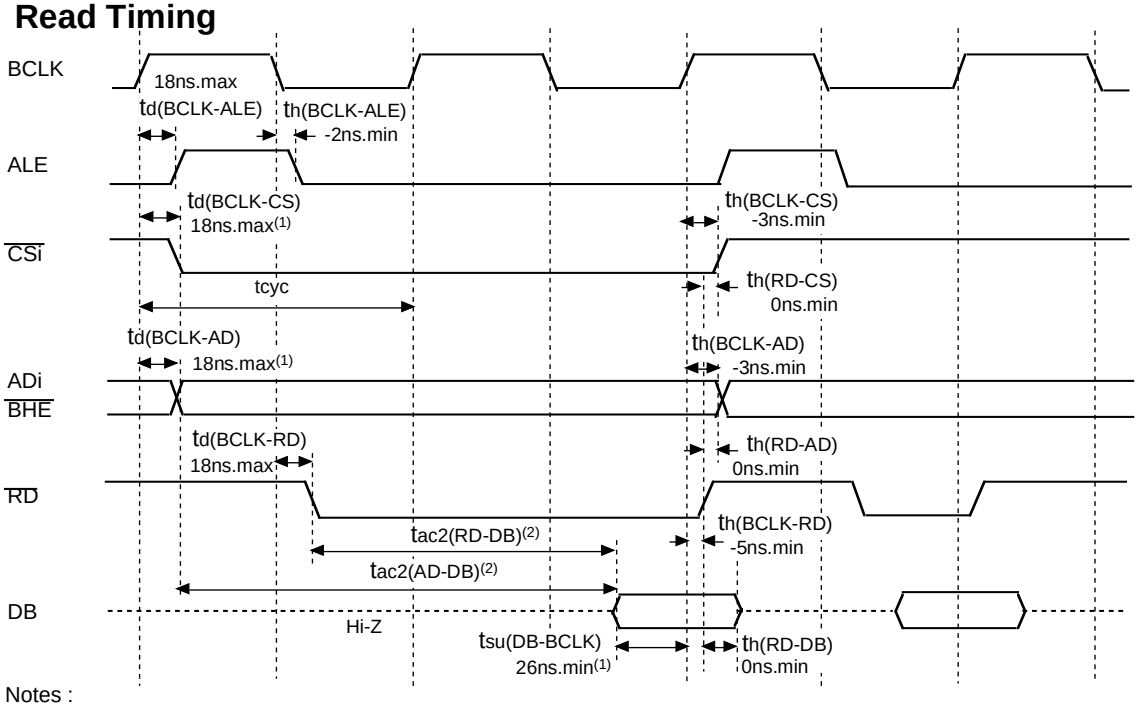
Measurement Conditions:
- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 26.2 Vcc=5V Timing Diagram (1)

Vcc=5V

Memory Expansion Mode and Microprocessor Mode (with a wait state)

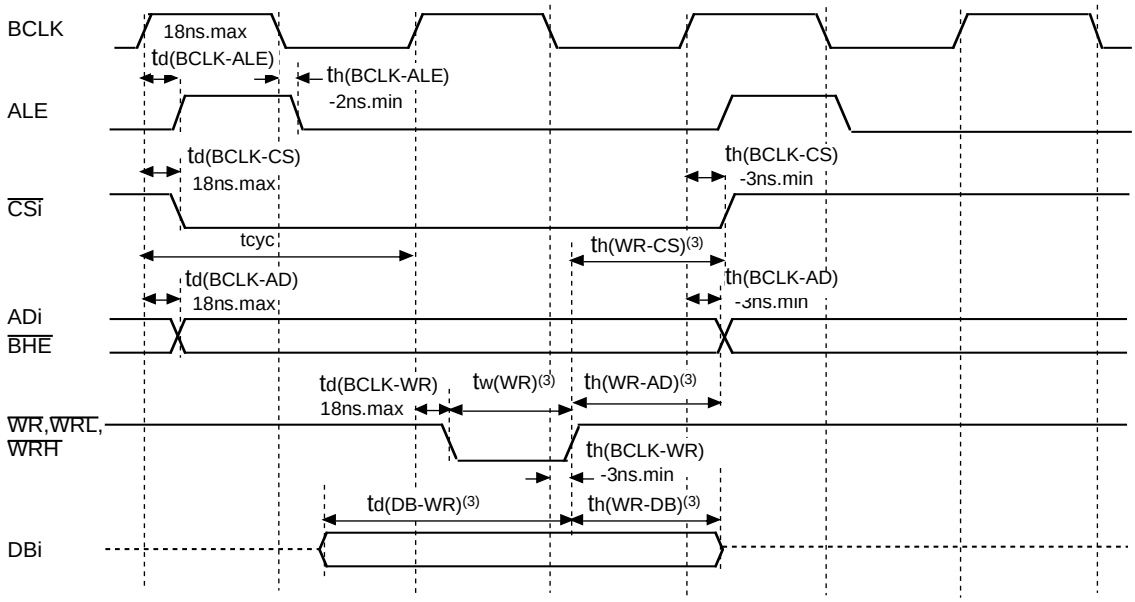
Read Timing



Notes :

1. Value guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:
   $t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states.)
   $t_{ac2(AD-DB)}$=(tcyc x n-35)ns.max (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states.)

Write Timing (written in 2 cycles with no wait state)



NOTES:

3. Varies with operation frequency:
   $t_{d(DB-WR)}$=(tcyc x n-20)ns.min
   (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min
   (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

Measurement conditions
- V_{CC}=4.2 to 5.5V
- Input high and low voltage:
  V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage:
  V_{OH}=2.0V, V_{OL}=0.8V

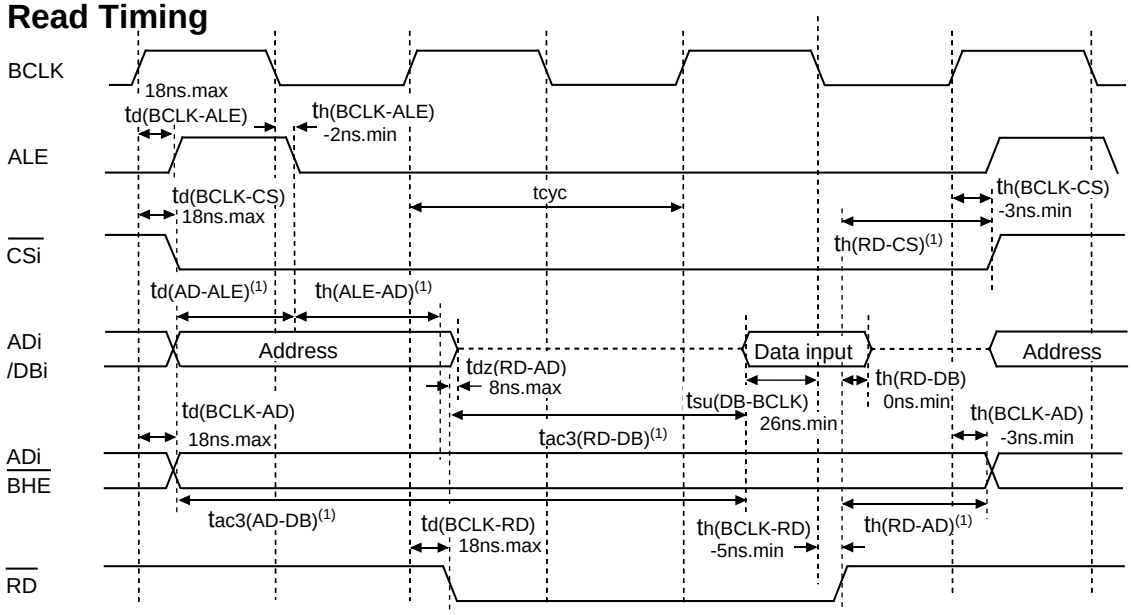
Figure 26.3 Vcc=5V Timing Diagram (2)

Vcc=5V

Memory Expansion Mode and Microprocessor Mode

(with a wait state, when accessing an external memory and using the multiplexed bus)

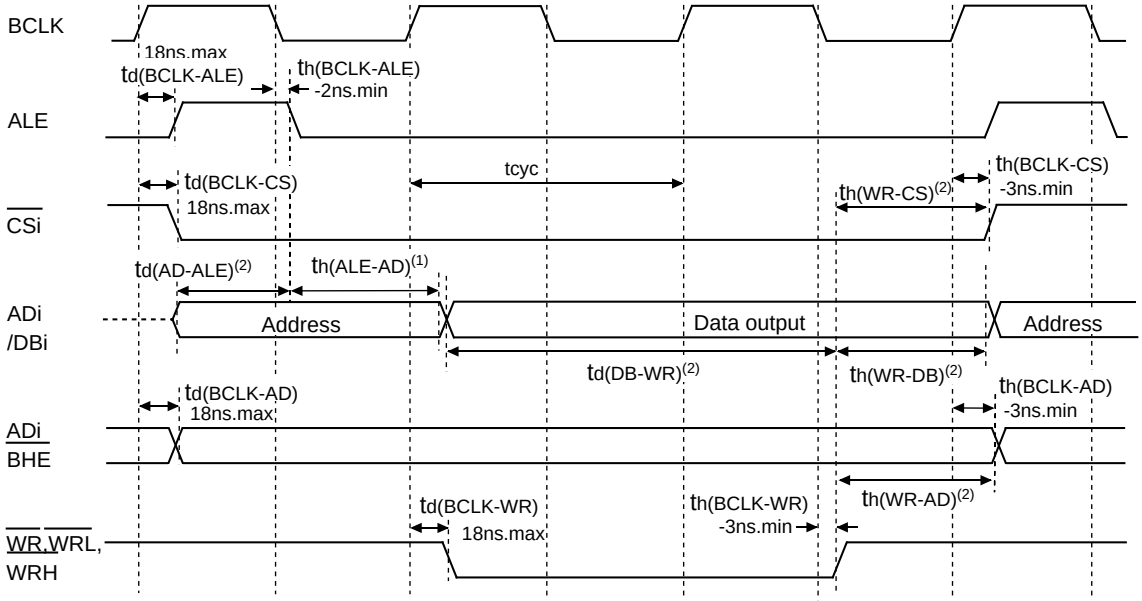
Read Timing



NOTES:

1. Varies with operation frequency:
   $t_{d(AD-ALE)}$=(tcyc/2-20)ns.min
   $t_{h(ALE-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min
   $t_{ac3(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 2 wait states and m=5 with 3 wait states)
   $t_{ac3(AD-DB)}$=(tcyc/2 x n-35)ns.max (n=5 with 2 wait states and n=7 with 3 wait states)

Write Timing (written in 2 cycles with no wait state)



NOTES:

2. Varies with operation frequency:
   $t_{d(AD-ALE)}$=(tcyc/2-20)ns.min
   $t_{h(ALE-AD)}$=(tcyc/2-10)ns.min, $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

Measurement Conditions:

- V_{CC}=4.2 to 5.5V
- Input high and low voltage:
  V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage:
  V_{OH}=2.0V. V_{OL}=0.8V

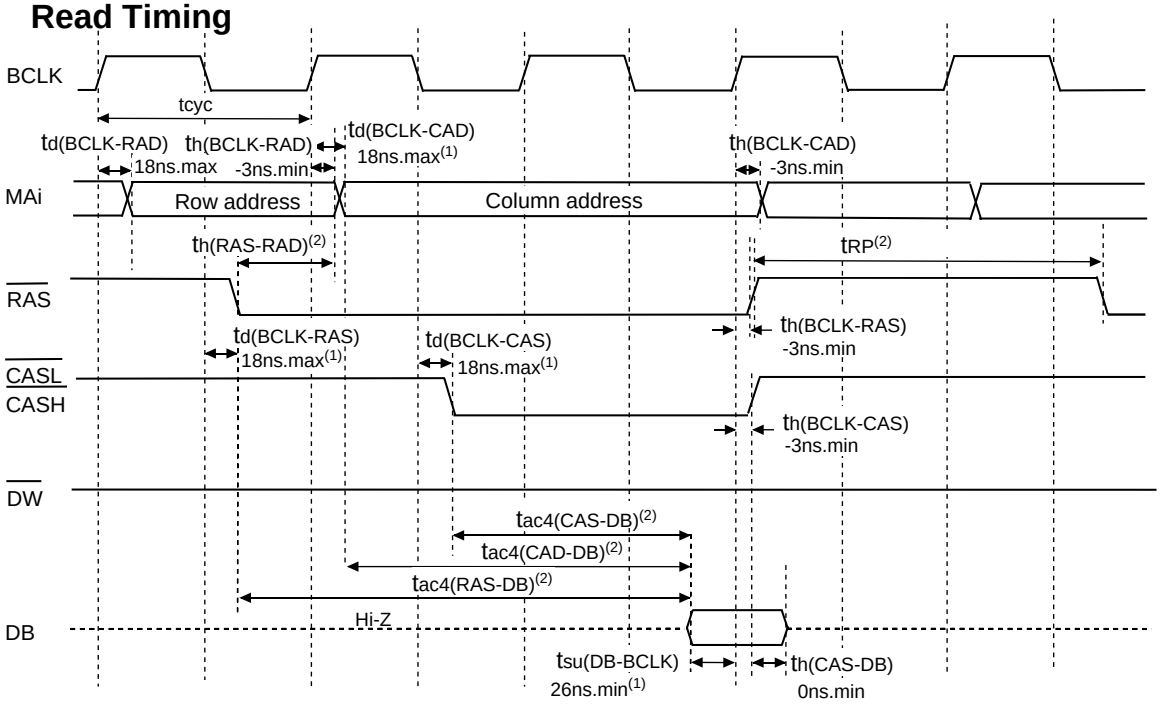
Figure 26.4 Vcc=5V Timing Diagram (3)

Vcc=5V

Memory Expansion Mode and Microprocessor Mode

(When accessing the DRAM area)

Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for the following combinations.
   - $t_{d(BCLK-RAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAD)} + t_{su(DB-BCLK)}$
2. Varies with operation frequency:
   - $t_{ac4(RAS-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state and m=5 with 2 wait states)
   - $t_{ac4(CAS-DB)}$=(tcyc/2 x n-35)ns.max (n=1 with 1 wait state and n=3 with 2 wait states)
   - $t_{ac4(CAD-DB)}$=(tcyc x l-35)ns.max (l=1 with 1 wait state and l=2 with 2 wait states)
   - $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   - t_{RP}=(tcyc/2 x 3-20)ns.min

Measurement Conditions:

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

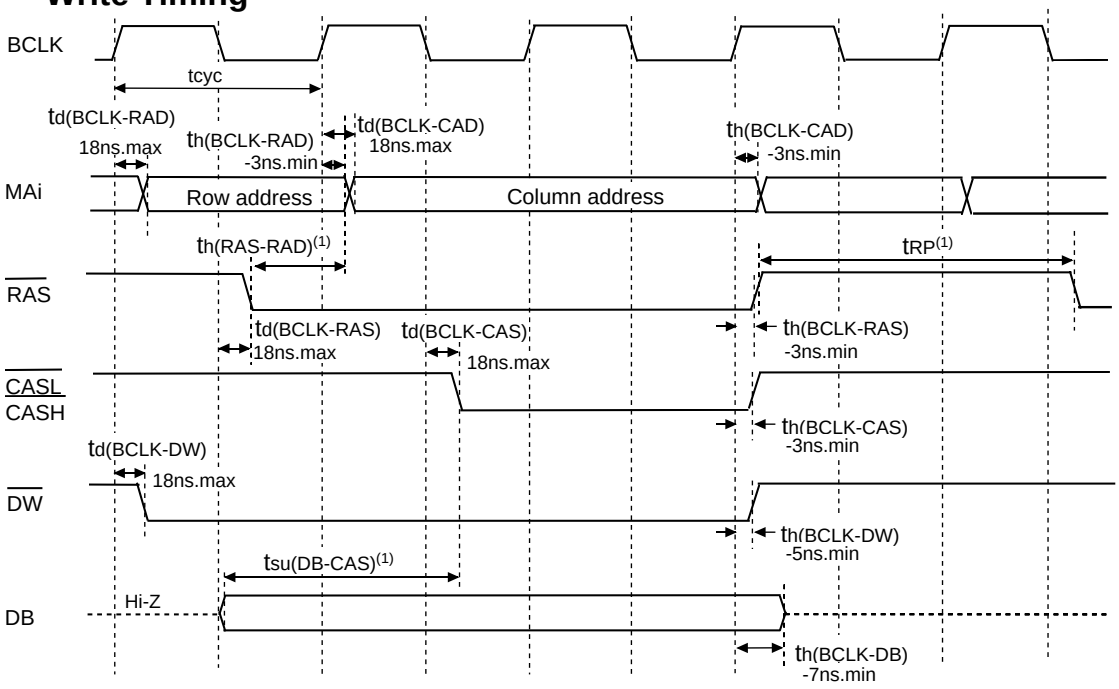
Figure 26.5 V_{CC}=5V Timing Diagram (4)

Memory Expansion Mode and Microprocessor Mode

Vcc=5V

(When accessing the DRAM area)

Write Timing



NOTES:

1. Varies with operation frequency:
   $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   t_{RP}=(tcyc/2 x 3-20)ns.min
   $t_{su(DB-CAS)}$=(tcyc-20)ns.min

Measurement Conditions:

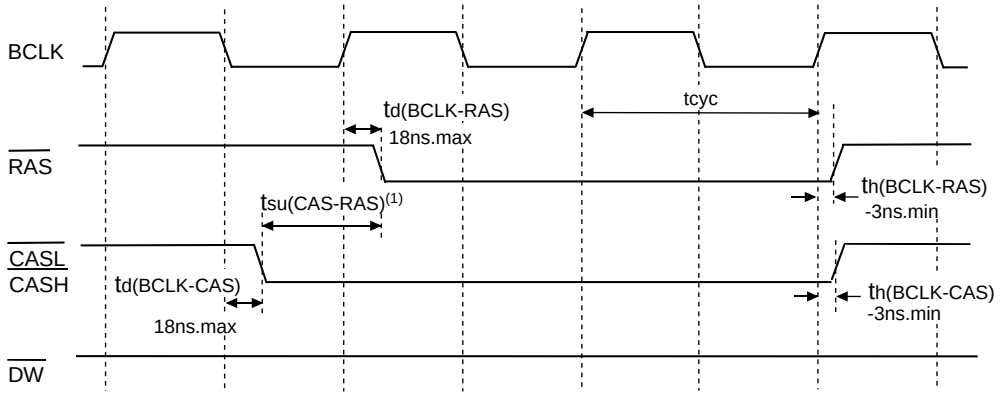
- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 26.6 Vcc=5V Timing Diagram (5)

Memory Expansion Mode and Microprocessor Mode

Vcc=5V

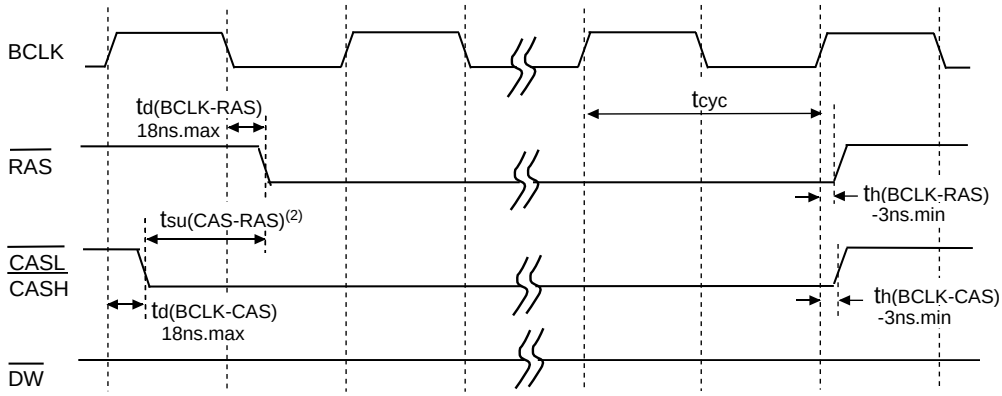
Refresh Timing (CAS-before-RAS refresh)



NOTES :

1. Varies with operation frequency:
   $t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Refresh Timing (Self-refresh)



NOTES:

2. Varies with operation frequency:
   $t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Measurement Conditions:

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 26.7 Vcc=5V Timing Diagram (6)

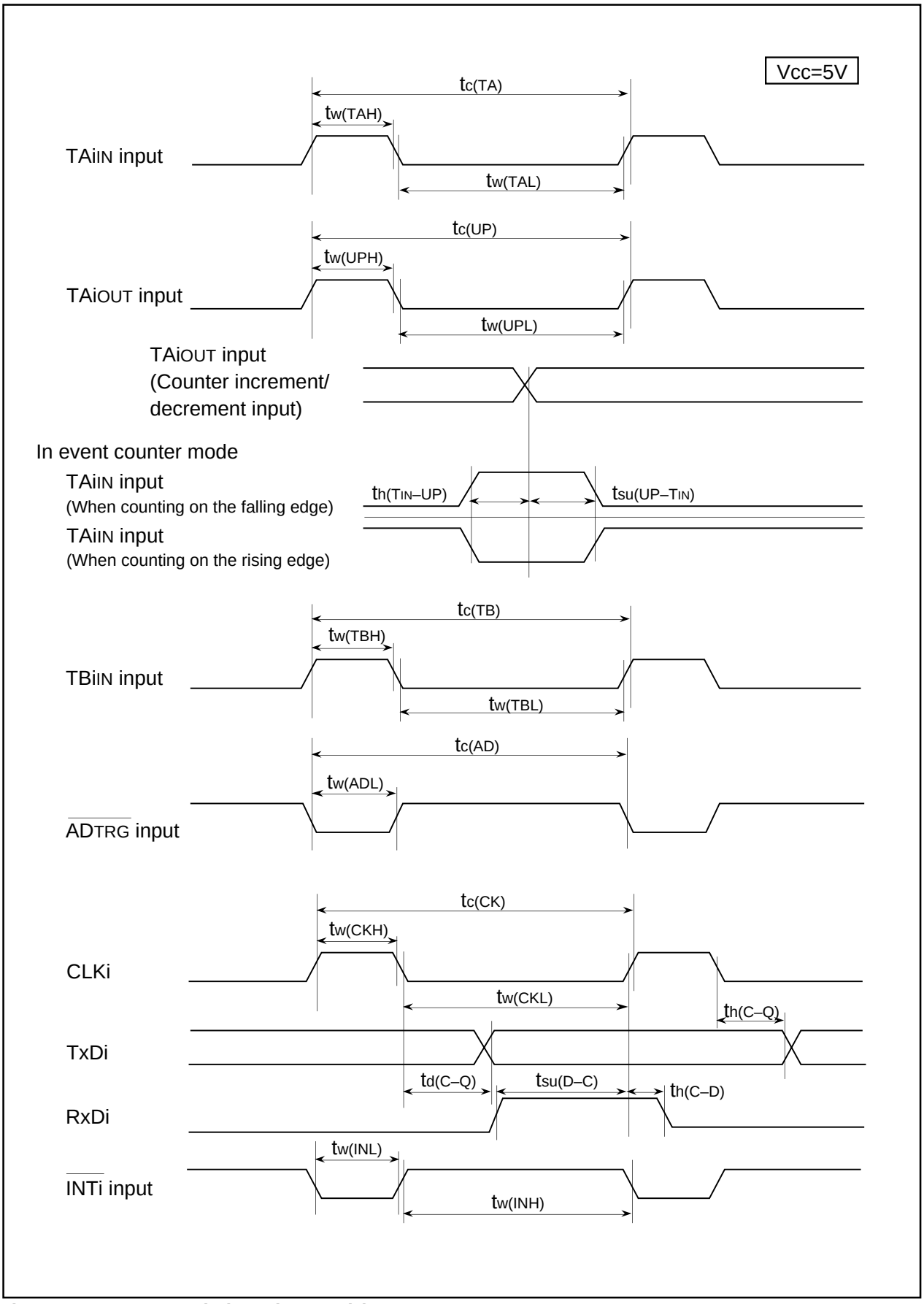
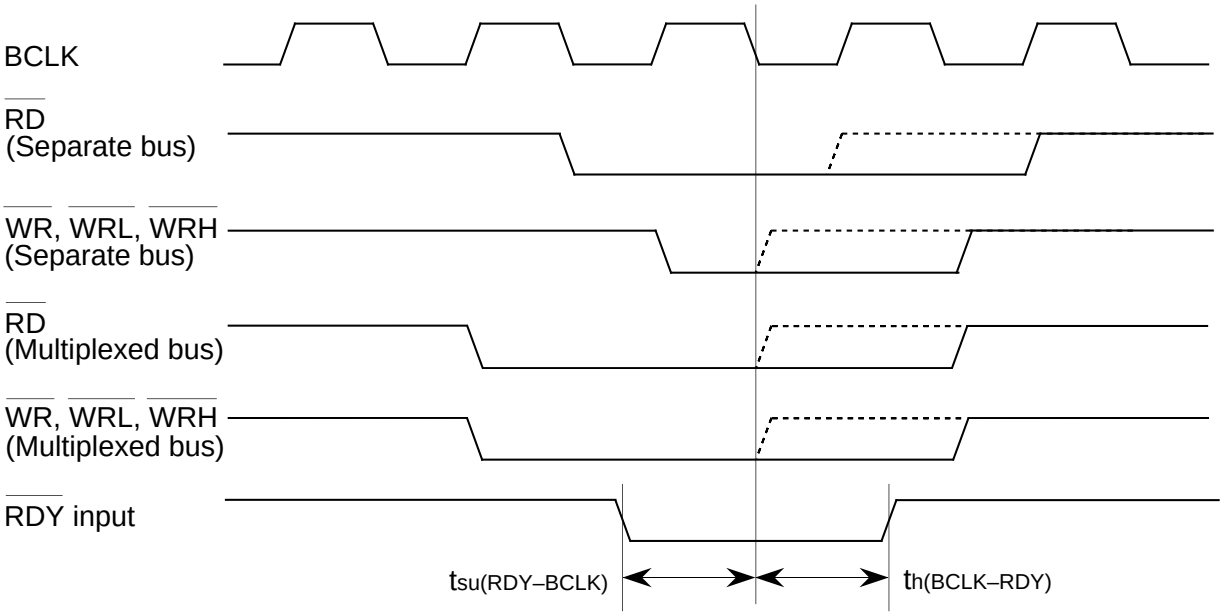


Figure 26.8 Vcc=5V Timing Diagram (7)

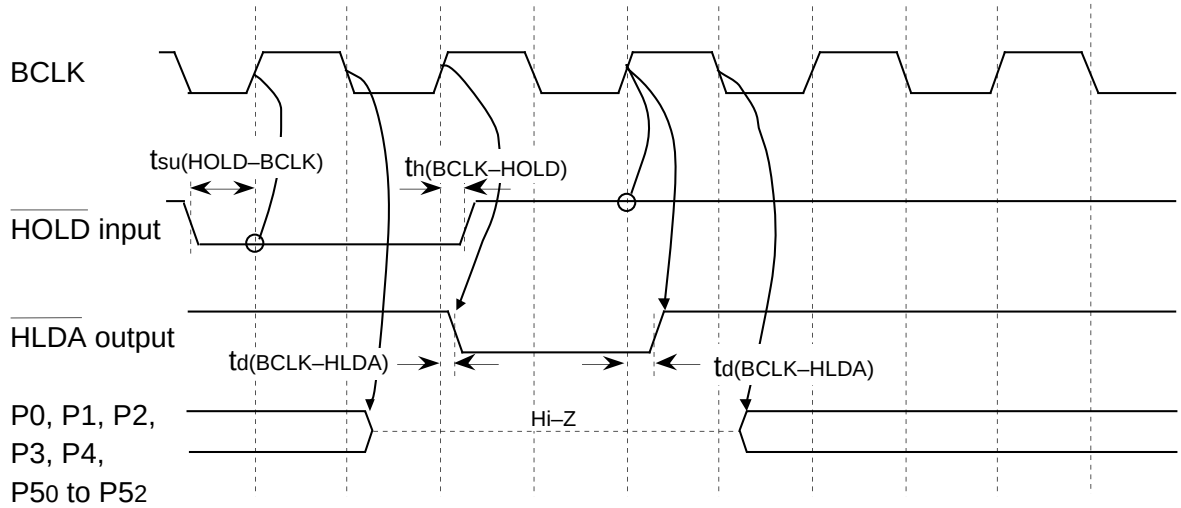
Vcc=5V

Memory Expansion Mode and Microprocessor Mode

(Valid only with a wait state)



(Valid with a wait state or with no wait state)



Measurement Conditions:
- VCC=4.2 to 5.5V
- Input high and low voltage: VIH=4.0V, VIL=1.0V
- Output high and low voltage: VOH=2.5V, VOL=2.5V

Figure 26.9 Vcc=5V Timing Diagram (8)

V_{CC}=3.3V

Table 26.24 Electrical Characteristics (V_{CC}=3.0 to 3.6V, V_{SS}=0V at Topr = –20 to 85°C, f(X_{IN})=20MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-1mA	2.7			V
		X_{OUT}	I_{OH}=-0.1mA	2.7			V
		X_{COUT}	No load applied		3.3		V
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=1mA			0.5	V
		X_{OUT}	I_{OL}=0.1mA			0.5	V
		X_{COUT}	No load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{AD_{TRG}}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=3V			4.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			-4.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V	66	120	500	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			3.0		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			20.0		MΩ
V_{RAM}	RAM Standby Voltage	Through VDC		2.5			V
		Not through VDC		2.0			V
I_{CC}	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(X_{IN})=20 MHz, square wave, no division		26	38	mA
			f(X_{CIN})=32 kHz, with a wait state, not through VDC, Topr=25° C		5.0		µA
			f(X_{CIN})=32 kHz, with a wait state, through VDC, Topr=25° C		340		µA
			Topr=25° C when the clock stops		0.4	20	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

VCC=3.3V

Table 26.25 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 3.0 to 3.6V, V_{SS} = AV_{SS} = 0V at Topr = –20 to 85°C, f(X_{IN}) = 20MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min	Typ	Max	
-	Resolution		V_{REF}=V_{CC}			10	Bits
INL	Integral Nonlinearity Error	No S&H function (8-bit)	V_{CC}=V_{REF}=3.3V			±2	LSB
DNL	Differential Nonlinearity Error	No S&H function (8-bit)				±1	LSB
-	Offset Error	No S&H function (8-bit)				±2	LSB
-	Gain Error	No S&H function (8-bit)				±2	LSB
R_{LADDER}	Resistor Ladder		V_{REF}=V_{CC}	8		40	kΩ
t_{CONV}	8-bit Conversion Time			4.9			µs
V_{REF}	Reference Voltage			3.0		V_{CC}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and hold

NOTES:
1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.

Table 26.26 D/A Conversion Characteristics (V_{CC} = V_{REF} = 3.0 to 3.6V, V_{SS} = AV_{SS} = 0V at Topr = –20 to 85°C, f(X_{IN}) = 20MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter not being used is set to "00_{16}". The resistor ladder in the A/D converter is exclued.
I_{VREF} flows even if the VCUT bit in the ADiCON1 register is set to "0" (no V_{REF} connection).

Table 26.27 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:
1. V_{CC}= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at Topr= 0 to 60° C, unless otherwise specified

VCC=3.3V

Timing Requirements (Vcc = 3.0 to 3.6V, Vss = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.28 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External Clock Input Cycle Time	50		ns
tw(H)	External Clock Input High ("H") Pulse Width	22		ns
tw(L)	External Clock Input Low ("L") Pulse Width	22		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 26.29 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min	Max	
tac1(RD-DB)	Data Input Access Time (RD standard, with no wait state)		(Note 1)	ns
tac1(AD-DB)	Data Input Access Time (AD standard, CS standard, with no wait state)		(Note 1)	ns
tac2(RD-DB)	Data Input Access Time (RD standard, with a wait state)		(Note 1)	ns
tac2(AD-DB)	Data Input Access Time (AD standard, CS standard, with a wait state)		(Note 1)	ns
tac3(RD-DB)	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac3(AD-DB)	Data Input Access Time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac4(RAS-DB)	Data Input Access Time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAS-DB)	Data Input Access Time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAD-DB)	Data Input Access Time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
tsu(DB-BCLK)	Data Input Setup Time	30		ns
tsu(RDY-BCLK)	RDY Input Setup Time	40		ns
tsu(HOLD-BCLK)	HOLD Input Setup Time	60		ns
th(RD-DB)	Data Input Hold Time	0		ns
th(CAS-DB)	Data Input Hold Time	0		ns
th(BCLK-RDY)	RDY Input Hold Time	0		ns
th(BCLK-HOLD)	HOLD Input Hold Time	0		ns
td(BCLK-HLDA)	HLDA Output Delay Time		25	ns

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequency. Insert a wait state or lower operation frequency, f(BCLK), if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]$$ (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states)

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns]$$ (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states)

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]$$ (m=3 with 2 wait states and m=5 with 3 wait states)

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns]$$ (n=5 with 2 wait states and n=7 with 3 wait states)

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]$$ (m=3 with 1 wait state and m=5 with 2 wait states)

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns]$$ (n=1 with 1 wait state and n=3 when 2 wait states)

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns]$$ (l=1 with 1 wait state and l=2 with 2 wait states)

VCC=3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.30 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Pulse Width	40		ns

Table 26.31 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Pulse Width	200		ns

Table 26.32 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Pulse Width	100		ns

Table 26.33 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAiIN Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Pulse Width	100		ns

Table 26.34 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

VCC=3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.35 Timer B input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 26.36 Timer B input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width	200		ns

Table 26.37 Timer B input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width	200		ns

Table 26.38 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ Input High ("H") Pulse Width (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Pulse Width	125		ns

Table 26.39 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Pulse Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Set Up Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 26.40 External Interrupt $\overline{INTi}$ input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(INH)}$	INTi Input High ("H") Pulse Width	250		ns
$t_{w(INL)}$	INTi Input Low ("L") Pulse Width	250		ns

VCC=3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C, unless otherwise specified)

Table 26.41 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 26.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-2		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$

VCC=3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.42 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 26.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-2		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9 \times n}{f_{(BCLK)}} - 20 \quad [ns]$$ (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$ (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

VCC=3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.43 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 26.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		0		ns
th(RD-AD)	Address Output Hold Time (RD standard)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-AD)	RD Signal Output Hold Time		-3		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 1)		ns
tdz(RD-AD)	Address Output High-Impedance Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$th(RD-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(AD-ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

VCC=3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 26.44 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting the DRAM Area)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Row Address Output Delay Time	See Figure 26.1		18	ns
$t_{h(BCLK-AD)}$	Row Address Output Hold Time (BCLK standard)		0		ns
$t_{d(BCLK-CAD)}$	Column Address Output Delay Time			18	ns
$t_{h(BCLK-CAD)}$	Column Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RAS-RAD)}$	Row Address Output Hold Time after RAS Output		(Note 1)		ns
$t_{d(BCLK-RAS)}$	RAS Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-RAS)}$	RAS Output Hold Time (BCLK standard)		0		ns
t_{RP}	RAS High ("H") Hold Time		(Note 1)		ns
$t_{d(BCLK-CAS)}$	CAS Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-CAS)}$	CAS Output Hold Time (BCLK standard)		0		ns
$t_{d(BCLK-DW)}$	DW Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-DW)}$	DW Output Hold Time (BCLK standard)		-3		ns
$t_{su(DB-CAS)}$	CAS Output Setup Time after DB output		(Note 1)		ns
$t_{h(BCLK-DB)}$	DB Signal Output Hold Time (BCLK standard)		-7		ns
$t_{su(CAS-RAS)}$	CAS Output Setup Time before RAS Output (refresh)		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to the BCLK frequency.

$$t_{h(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

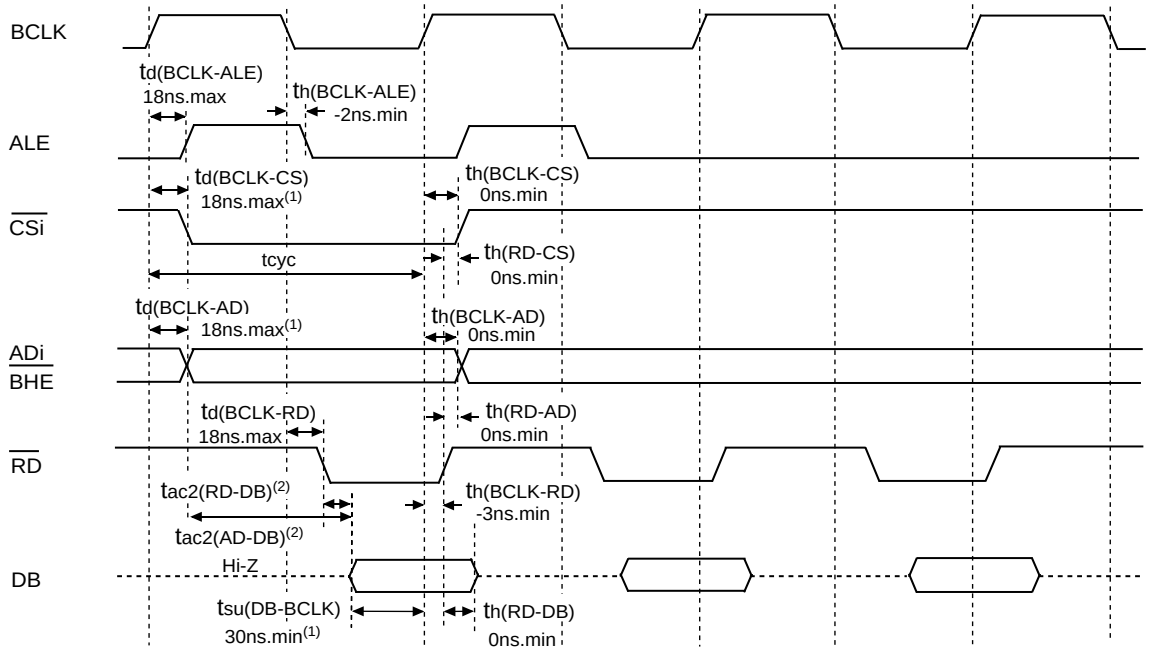
$$t_{su(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{su(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode (with no wait state)

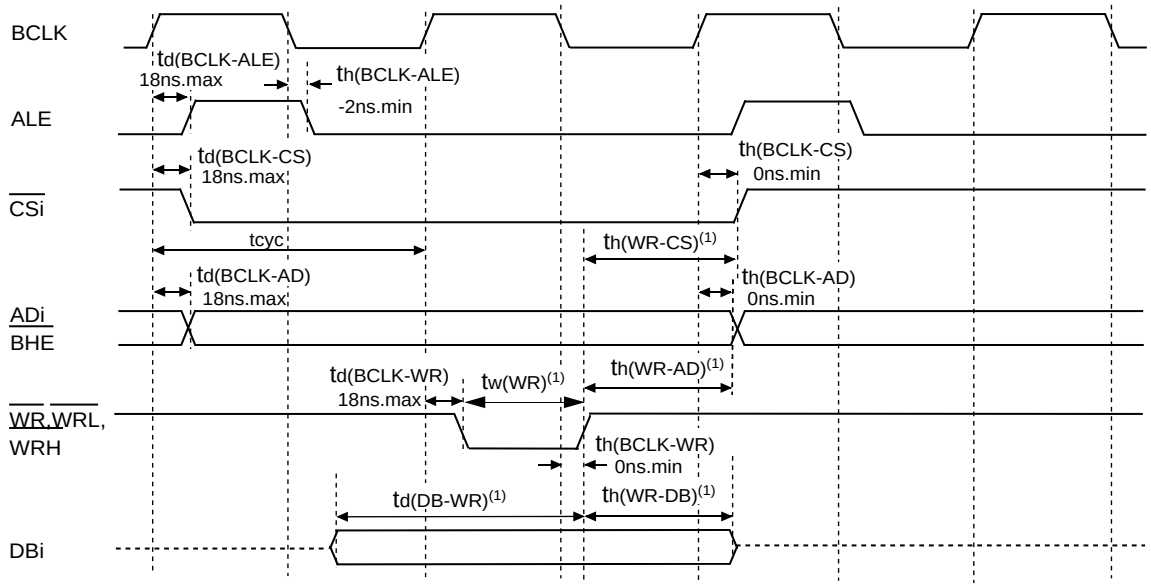
Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:
   $t_{ac2(RD-DB)}$=(tcyc/2-35)ns.max
   $t_{ac2(AD-DB)}$=(tcyc-35)ns.max

Write Timing



NOTES:

1. Varies with operation frequency.
   $t_{d(DB-WR)}$=(tcyc-20)ns.min
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2-15)ns.min

Measurement Conditions:

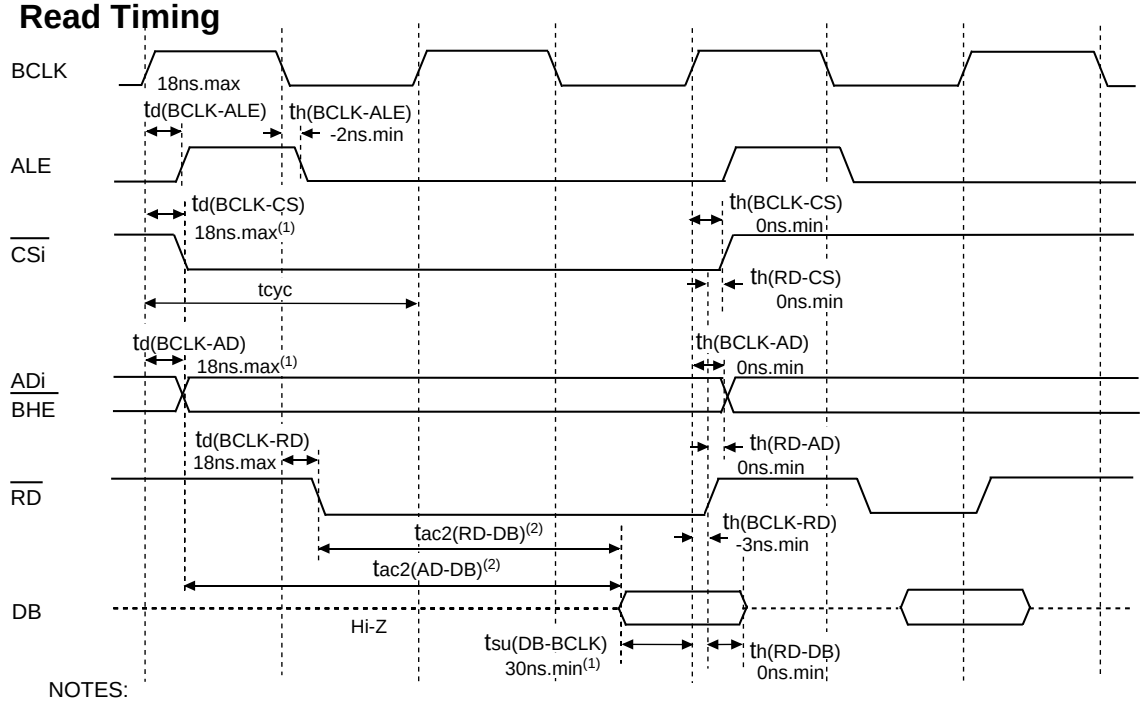
- V_{CC}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

Figure 26.10 V_{CC}=3.3V Timing Diagram (1)

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode (with a wait state)

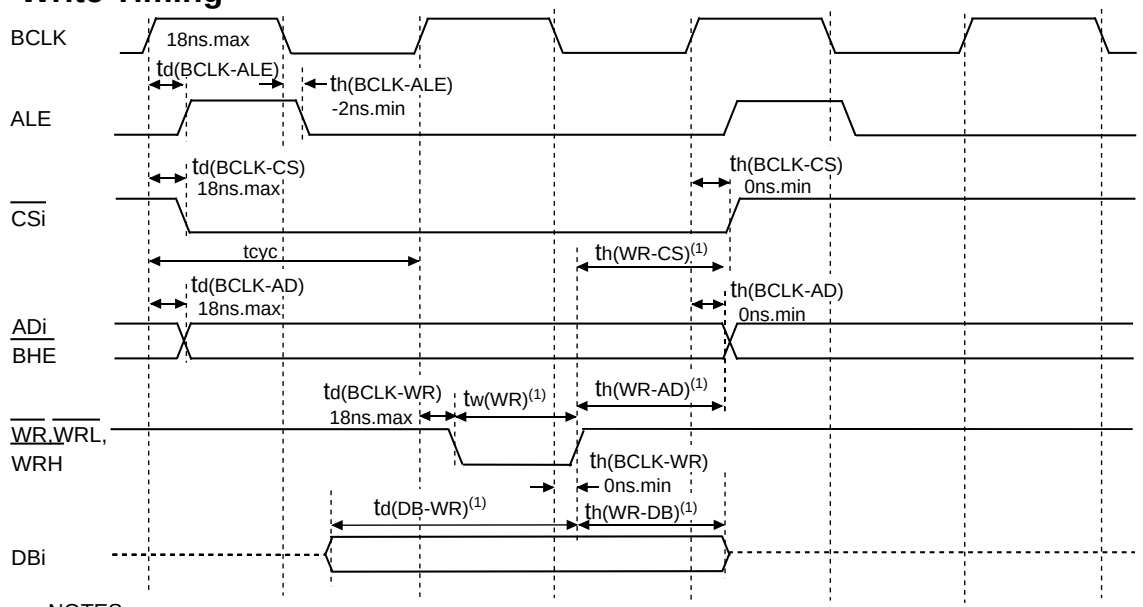
Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently. A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency.
   $t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states)
   $t_{ac2(AD-DB)}$=(tcyc x n-35)ns.max (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states)

Write Timing



NOTES:

1. Varies with operation frequency.
   $t_{d(DB-WR)}$=(tcyc x n-20)ns.min
   (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min
   (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

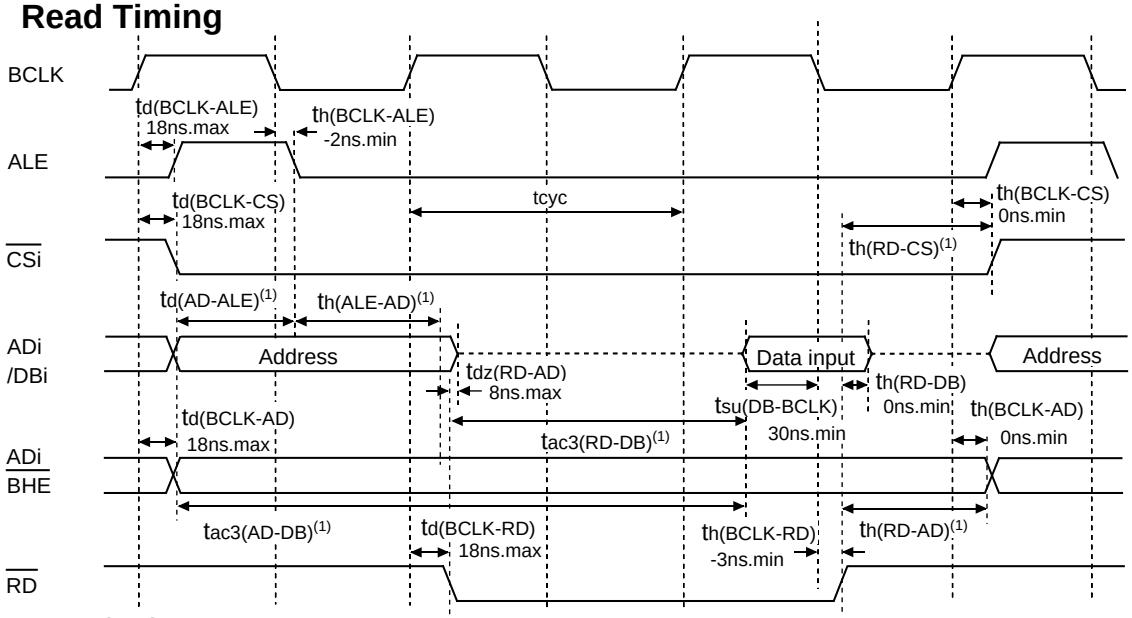
Figure 26.11 V_{CC}=3.3V Timing Diagram (2)

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode

(with a wait state, when accessing an external memory and using the multiplexed bus)

Read Timing



NOTES:

1. Varies with operation frequency.

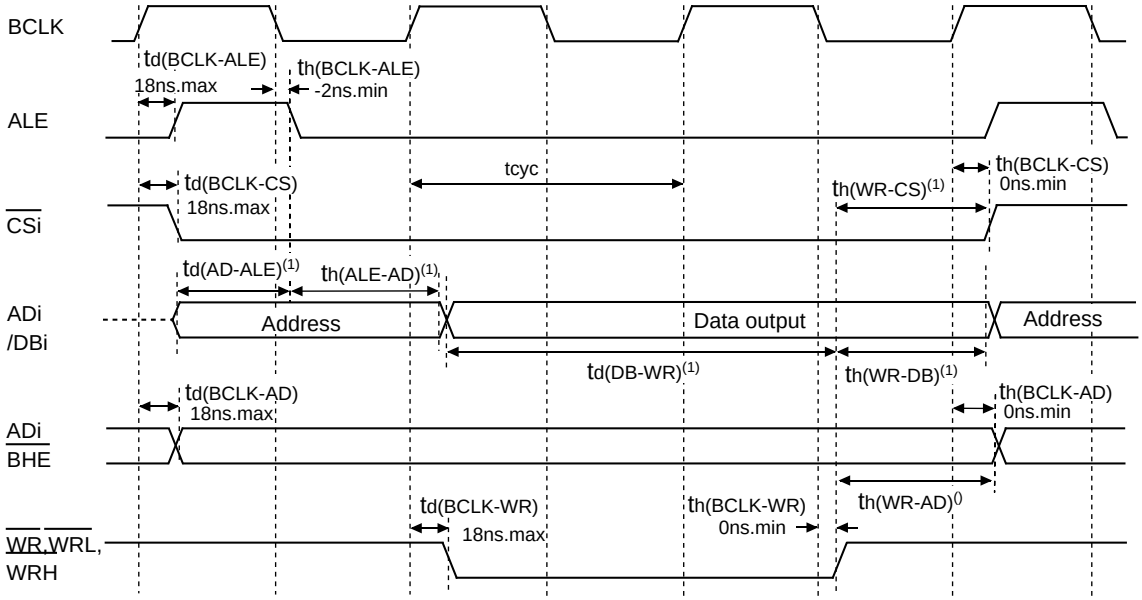
$t_{d(AD-ALE)}$=(tcyc/2-20)ns.min

$t_{h(ALE-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac3(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 2 wait states and m=5 with 3 wait states)

$t_{ac3(AD-DB)}$=(tcyc/2 x n-35)ns.max (n=5 with 2 wait states and n=7 with 3 wait states)

Write Timing



NOTES:

1. Varies with operation frequency.

$t_{d(AD-ALE)}$=(tcyc/2-20)ns.min

$t_{h(ALE-AD)}$=(tcyc/2-10)ns.min, $t_{h(WR-AD)}$=(tcyc/2-10)ns.min

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(m=3 with 2 wait states and m=5 with 3 wait states)

Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

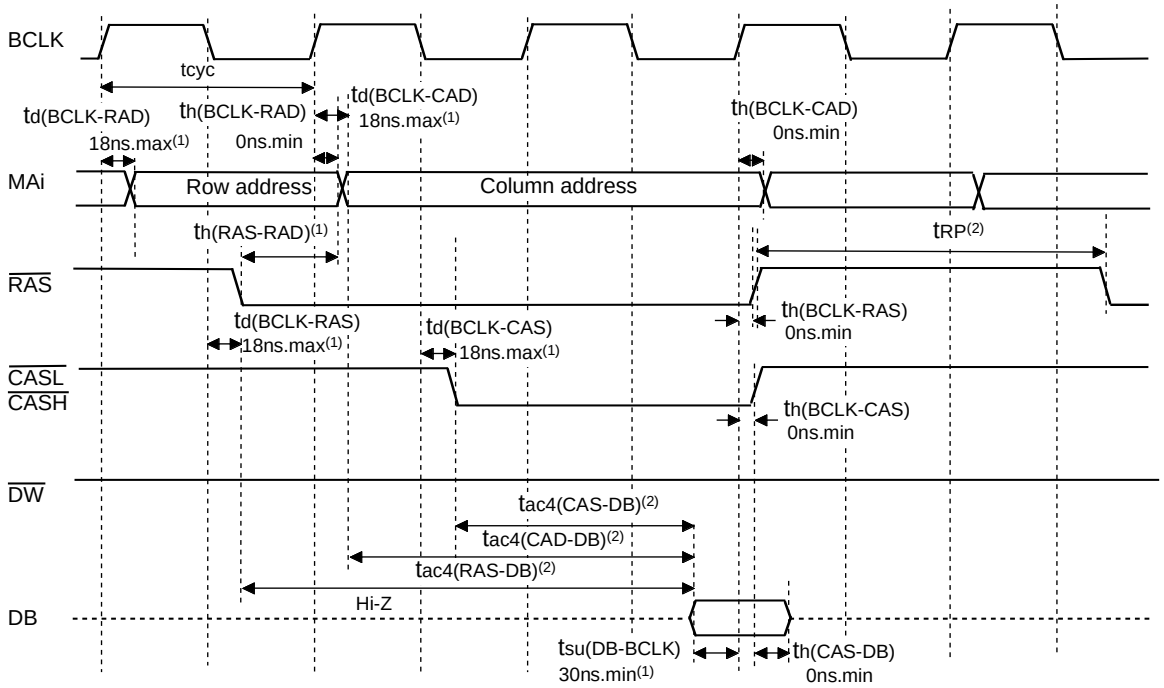
Figure 26.12 V_{CC}=3.3V Timing Diagram (3)

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode

(With 2 wait states, when accessing the DRAM area)

Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently. A maximum of 35ns is guaranteed for the followings:
   $t_{d(BCLK-RAS)} + t_{su(DB-BCLK)}$
   $t_{d(BCLK-CAS)} + t_{su(DB-BCLK)}$
   $t_{d(BCLK-CAD)} + t_{su(DB-BCLK)}$
2. It varies with the operation frequency.
   $t_{ac4(RAS-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state and m=5 with 2 wait states)
   $t_{ac4(CAS-DB)}$=(tcyc/2 x n-35)ns.max (n=1 with 1 wait state and n=3 with 2 wait states)
   $t_{ac4(CAD-DB)}$=(tcyc x l-35)ns.max (l=1 with 1 wait state and l=2 with 2 wait states)
   $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   t_{RP}=(tcyc/2 x 3-20)ns.min

Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

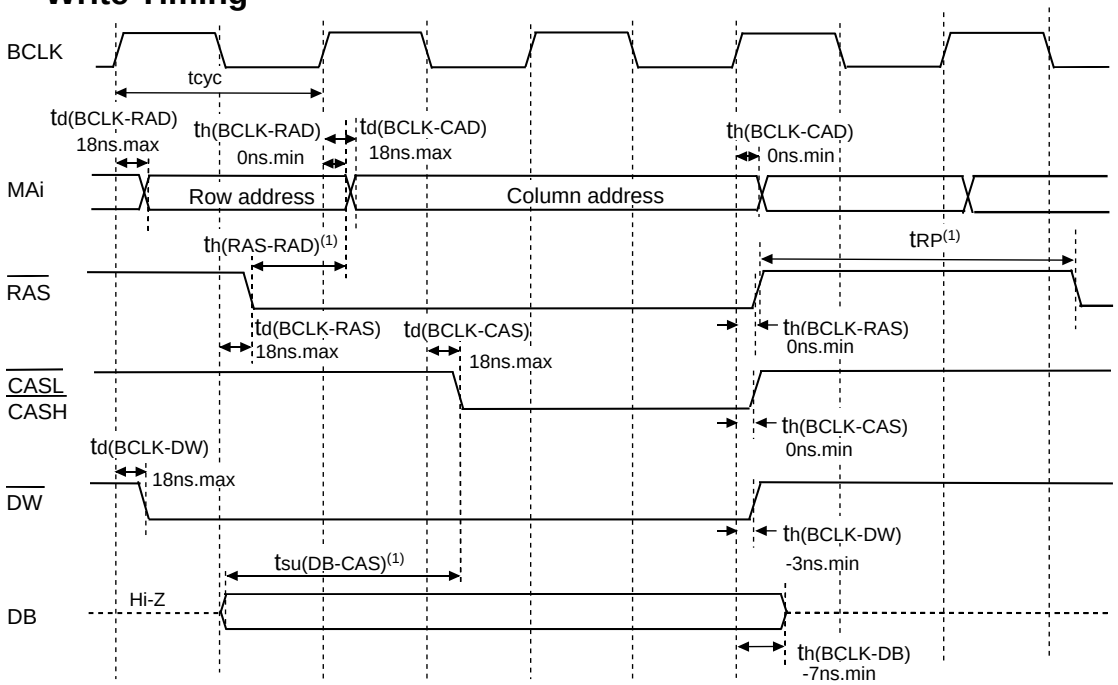
Figure 26.13 V_{CC}=3.3V Timing Diagram (4)

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode

(With 2 wait states, when accessing the DRAM area)

Write Timing



NOTES:

1. Varies with operation frequency.
   $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   t_{RP}=(tcyc/2 x 3-20)ns.min
   $t_{su(DB-CAS)}$=(tcyc-20)ns.min

Measurement Conditions:

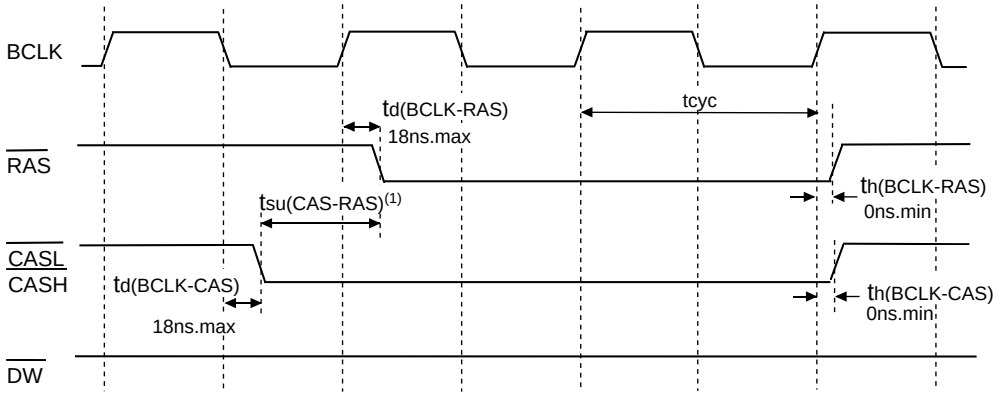
- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

Figure 26.14 V_{CC}=3.3V Timing Diagram (5)

Vcc=3.3V

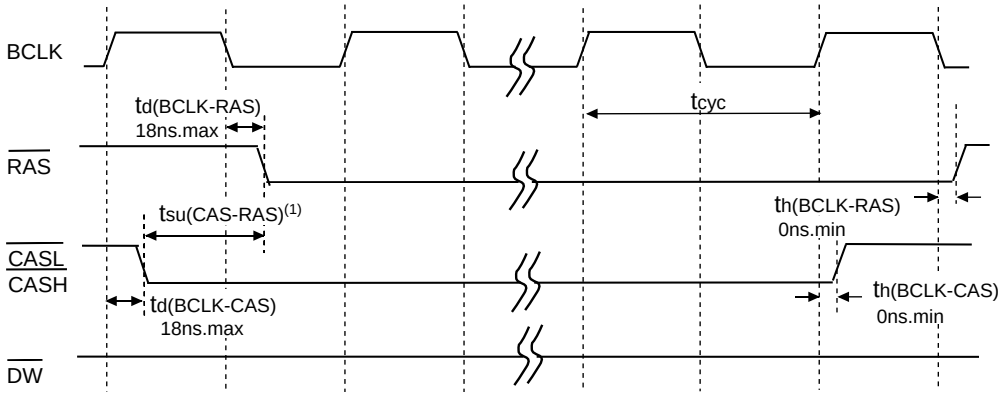
Memory Expansion Mode and Microprocessor Mode

Refresh Timing (CAS-before-RAS refresh)



NOTES:
1. Varies with operation frequency.
$t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Refresh Timing (Self-refresh)



NOTES:
1. Varies with operation frequency.
$t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Measurement Conditions:
- V_{CC}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

Figure 26.15 V_{CC}=3.3V Timing Diagram (6)

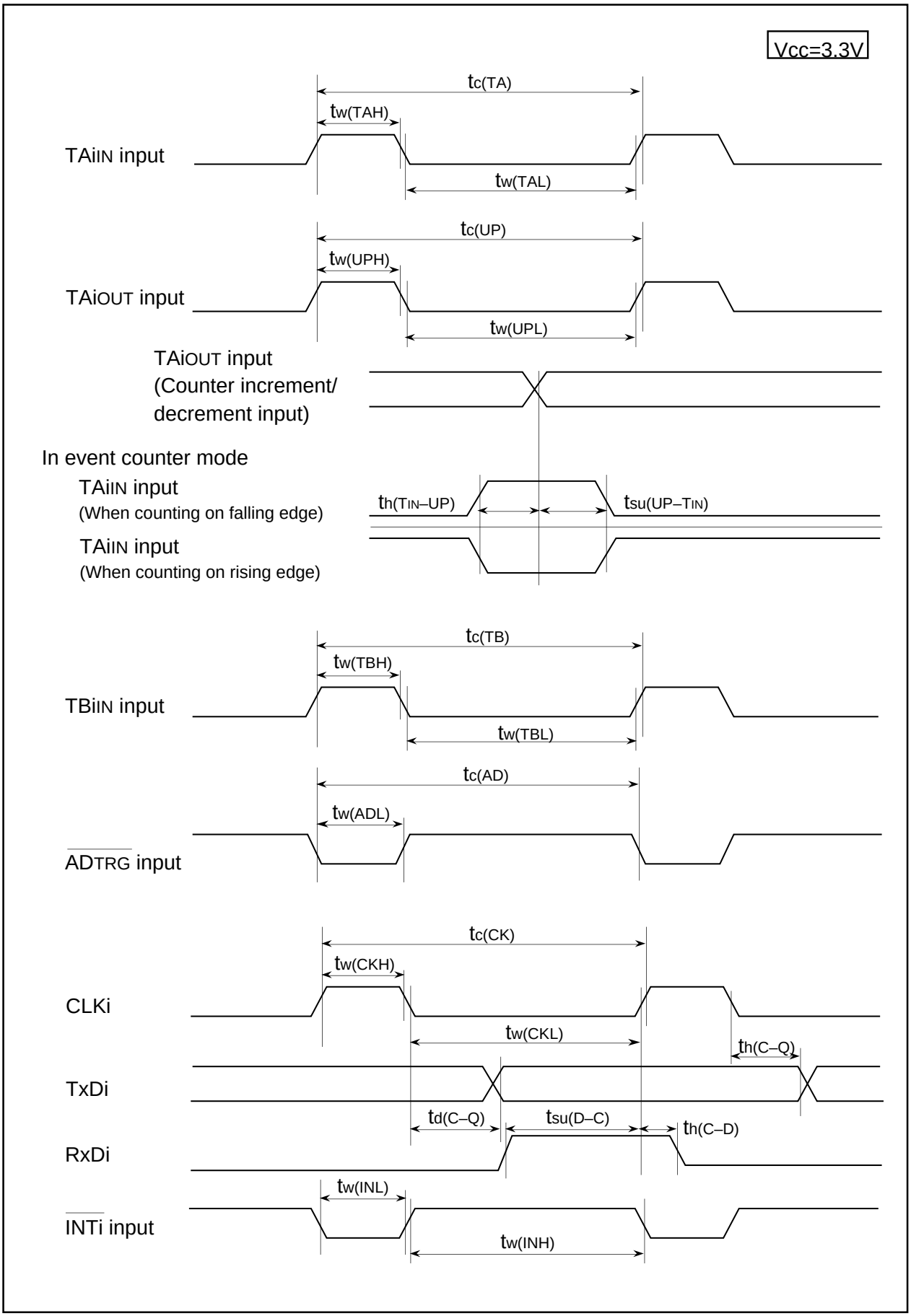
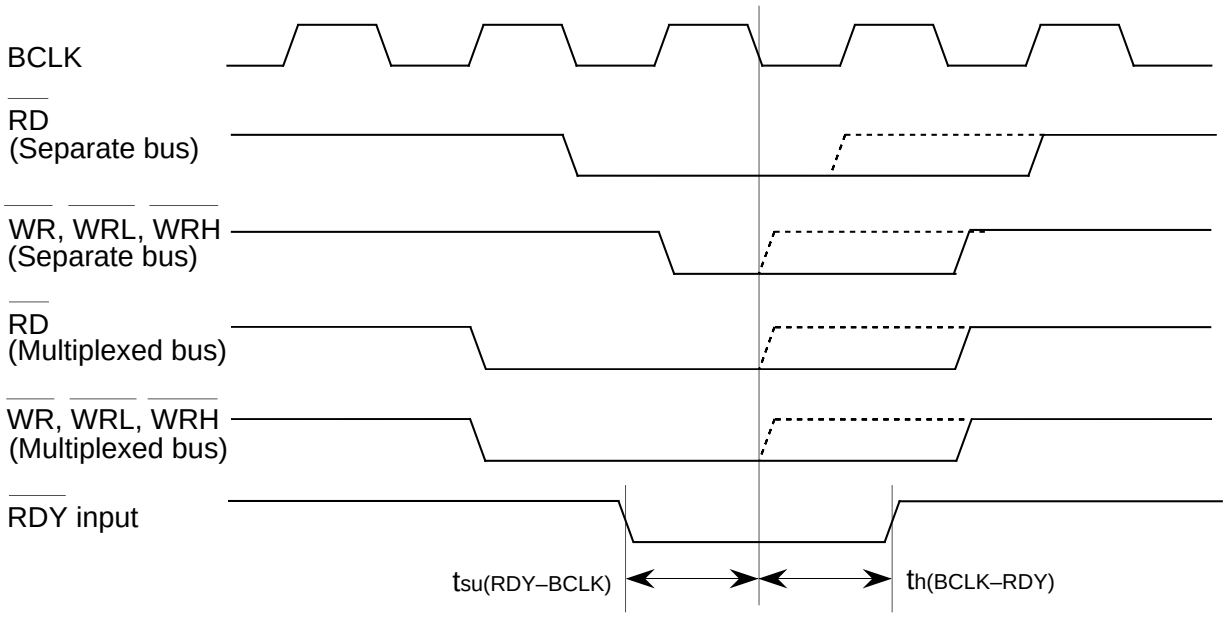


Figure 26.16 Vcc=3.3V Timing Diagram (7)

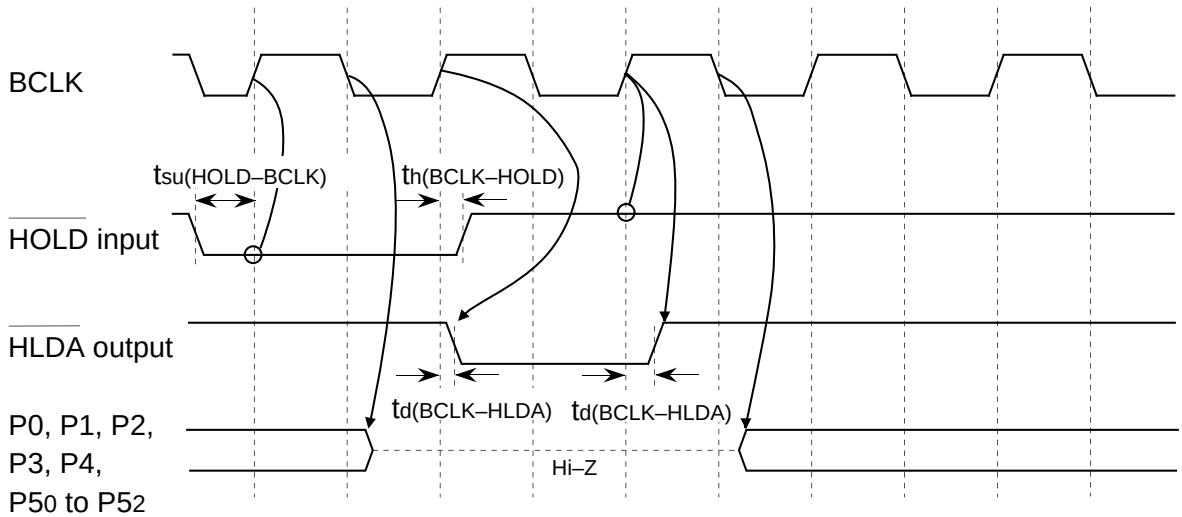
Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode

(Valid only with a wait state)



(Valid with a wait state and no wait state)



Measurement Conditions:
- VCC=3.0 to 3.6V
- Input high and low voltage: VIH=2.4V, VIL=0.6V
- Output high and low voltage: VOH=1.5V, VOL=1.5V

Figure 26.17 Vcc=3.3V Timing Diagram (8)

27. Precautions

27.1 Processor Mode

27.1.1 Microprocessor Mode

SFR, internal RAM and external space can be accessed when in microprocessor mode. The internal ROM cannot be accessed.

The internal ROM cannot be accessed, despite entering memory expansion mode or single-chip mode , if the microcomputer begins operation in microprocessor mode while the CNVSS is held high ("H") after reset.

27.2 Bus

27.2.1 $\overline{\text{HOLD}}$ Signal

When entering microprocessor mode or memory expansion mode from single-chip mode and using $\overline{\text{HOLD}}$ input, set the PM01 to PM00 bits to "11$_2$" (microprocessor mode) or to "10$_2$" (memory expansion mode) after setting the PD4_0 to PD4_7 bits in the PD4 register and the PD5_0 to PD5_2 bits in the PD5 register to "0" (input mode).

P4$_0$ to P4$_7$ (A$_{16}$ to A$_{22}$, $\overline{\text{A}_{23}}$, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, MA8 to MA12) and P5$_0$ to P5$_2$ ($\overline{\text{RD}}$/$\overline{\text{WR}}$/$\overline{\text{BHE}}$, $\overline{\text{RD}}$/$\overline{\text{WRL}}$,$\overline{\text{WRH}}$) do not enter a high-impedance state even when an "L" signal is applied to the $\overline{\text{HOLD}}$ pin, if the PM01 to PM00 bits are set to "11$_2$" (microprocessor mode) or to "10$_2$" (memory expansion mode) after setting the PD4_0 to PD4_7 bits in the PD4 register and the PD5_0 to PD5_2 bits in the PD5 register to "1" (output mode) in single-chip mode.

27.2.2 External Bus

The internal ROM cannot be read when an "H" signal is applied to the CNV$_{SS}$ pin and the hardware reset (hardware reset 1 or hardware reset 2) occurs.

27.3 SFR

27.3.1 100-Pin Package

Set address space for 03CB16, 03CE16, 03CF16, 03D216, 03D316 to "FF16" after reset when using the 100-pin package. 03DC16 must be set to "0016" after reset.

27.3.2 Register Settings

Table 27.1 lists registers containing bits which can only be written to. Set these registers with immediate values. When establishing the next value by altering the present value, write the present value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.

Table 25.1 Registers with Write-only Bits

Register	Address	Register	Address
WDTS register	000E16	U2BRG register	033916
G0RI register	00EC16	U2TB register	033B16, 033A16
G1RI register	012C16	UDF register	034416
G2TB register	016D16, 016C16	TA0 register(1)	034716, 034616
G3TB register	017D16, 017C16	TA1 register(1)	034916, 034816
U4BRG register	02F916	TA2 register(1)	034B16, 034A16
U4TB register	02FB16, 02FA16	TA3 register(1)	034D16, 034C16
TA11 register	030316, 030216	TA4 register(1)	034F16, 034E16
TA21 register	030516, 030416	U0BRG register	036916
TA41 register	030716, 030616	U0TB register	036B16, 036A16
DTT register	030C16	U1BRG register	02E916
ICTB2 register	030D16	U1TB register	02EB16, 02EA16
U3BRG register	032916	AD0CON2 register	039416
U3TB register	032B16, 032A16		

NOTES :

1. In one-shot timer mode and pulse width modulation mode only.

27.4 Clock Generating Circuit

27.4.1 PLL Frequency Synthesizer

Stabilize supply voltage when using the PLL frequency synthesizer. The ripple of supply voltage at 5V must be less than 10kHz in frequency, 0.5V (peak to peak) in voltage fluctuation range, and 1V/ms in voltage fluctuation rate. The ripple of supply voltage at 3.3V must be less than 100Hz in frequency, 0.2V (peak to peak) in voltage fluctuation range, and 0.1V/ms in voltage fluctuation rate.

27.4.2 Power Control

- When resetting the microcomputer to exit stop mode, apply an "L" signal to the $\overline{\text{RESET}}$ pin until the main clock oscillation stabilizes.

- Write at least 4 NOP instructions after the WAIT instruction or instructions to set the CM10 bit in the CM1 register to "1" (all clocks stop). When entering wait mode or stop mode, the instruction queue reads ahead to instructions following the WAIT instruction and instructions to set the CM10 bit to "1", and the program stops. The next instruction may be executed before entering wait mode or stop mode, depending on the combination of instructions and their execution timing.

- The followings are suggestions for reducing power consumption when programming or designing systems:

  Ports: I/O ports maintains the same state despite the microcomputer entering wait mode or stop mode. Current flows through active output ports. Feedthrough current flows through input ports in a high-impedance state. Set unused ports as input ports and stablize electrical potential before entering wait mode or stop mode.

  A/D converter: If the A/D conversion is not performed, set the VCUT bit in the AD0CON1 register to "0"(no V_{REF} connection). Set the VCUT bit to "1" (V_{REF} connection) and wait at least 1µs before starting the A/D conversion.

  D/A converter: Set the DAi bit (i=0 to 1) in the DACON register to "0" (output disabled) and set the DAi register to "00_{16}" when the D/A conversion is not performed.

  Peripheral function stop: Set the CM02 bit in the CM0 register while in wait mode to stop unnecessary peripheral functions. However, this does not reduce power consumption because the peripheral function clock (fc32) generating from the sub clock does not stop. When in low-speed mode and low-power consumption mode, do not enter wait mode when the CM02 bit is set to "1" (peripheral clock stops in wait mode).

  External clock: When using an external clock input for the CPU clock, set the CM05 bit in the CM0 register to "1" (main clock stops). This disables the X_{OUT} pin and reduces power consumption. (When using an external clock input, the clock is applied regardless of the CM05 bit setting.)

27.4.3 Wait Mode

27.4.3.1 Entering Wait Mode

The microcomputer enters wait mode when WAIT instructions are executed.
Follow the procedure below to enter wait mode.

- Initial Setting
  Set each interrupt priority level after setting the minimum interrupt priority level required to exit stop mode and wait mode, controlled by the RLVL2 to RLVL0 bits in the RLVL register, to "7".
- Before Execution of WAIT Instruction
  (1) Set the interrupt priority level of the interrupt being used to exit wait mode
  (2) Set the interrupt priority level of the interrupts not being used to exit wait mode
  (3) Set the IPL in the FLG register. Then, set the minimum interrupt priority level required to exit stop mode and wait mode to the same level as the IPL. (Interrupt priority level of the interrupt used to exit wait mode > minimum interrupt priority level to exit wait mode ≥ interrupt priority level of the interrupts not used to exit wait mode)
  (4) Set the I flag to "1"
  (5) Execute WAIT instruction
- After Exiting Wait Mode
  Set the interrupt priority level required to exit wait mode to "7" immediately after exiting wait mode.

27.4.4 Stop Mode

When the CM10 bit in the CM1 register is set to "1" (all clocks stop), stop mode is entered. The MCD register is simultaneously set to "08_{16}" (divide-by-8 mode).

27.4.4.1 Entering Stop Mode

Follow the procedure below to enter stop mode.

- Initial Setting
  Set each interrupt priority level after setting the minimum interrupt priority level required to exit stop mode and wait mode, controlled by the RLVL2 to RLVL0 bits in the RLVL register, to "7".
- Before Execution of WAIT Instruction
  (1) Set the interrupt priority level of the interrupt being used to exit stop mode
  (2) Set the interrupt priority levels of the interrupts not being used to exit stop mode
  (3) Set the IPL in the FLG register. Then, set the minimum interrupt priority level required to exit stop mode and wait mode to the same level as the IPL. (Interrupt priority level of the interrupt used to exit stop mode > minimum interrupt priority level to exit stop mode ≥ interrupt priority level of the interrupts not used to exit stop mode)
  (4) Set the I flag to "1"
  (5) Set the CM10 bit in the CM1 register to "1" (all clocks stop) after setting the PRC0 bit in the PRCR register to "1" (write enabled)
- After Exiting Stop Mode
  Set the interrupt priority level required to exit stop mode to "7" immediately after exiting stop mode.

27.5 Protection

The PRC2 bit in the PRCR register is changed to "0" (writing disable) when an instruction is written to any address after the PRC2 bit is set to "1" (writing enable). Write instruction immediately after setting the PRC2 bit to "1" to change registers protected by the PRC2 bit. Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the following instruction.

27.6 Interrupts

27.6.1 ISP Setting

After reset, the ISP is set to "000000$_{16}$". The program runs out of control if an interrupt is acknowledged before the ISP is set. Therefore, the ISP must be set before an interrupt request is acknowledged. Set the ISP to an even address, which allows interrupt sequences to be executed at a higher speed.

To use $\overline{\text{NMI}}$ interrupt, set the ISP at the beginning of the program. The $\overline{\text{NMI}}$ interrupt can be acknowledged after the first instruction has been executed after reset.

27.6.2 $\overline{\text{NMI}}$ Interrupt

- $\overline{\text{NMI}}$ interrupt cannot be denied. Connect the $\overline{\text{NMI}}$ pin to V_{CC} via a resistor (pull-up) when not in use.
- The P8_5 bit in the P8 register indicates the $\overline{\text{NMI}}$ pin value. Read the P8_5 bit only to determine the pin level after a $\overline{\text{NMI}}$ interrupt occurs.
- H" and "L" of a signal applied to the $\overline{\text{NMI}}$ pin must be over 2 CPU clock cycles + 300 ns wide.

27.6.3 $\overline{\text{INT}}$ Interrupt

- Edge sense

  "H" and "L" of a signal applied to the $\overline{\text{INT}}$0 to $\overline{\text{INT}}$5 pins must be at least 250 ns wide, regardless of the CPU clock.
- Level sense

  "H" and "L" of a signal applied to the $\overline{\text{INT}}$0 to $\overline{\text{INT}}$5 pins must be at least 1 CPU clock cycle + 200 ns wide. For example, "H" and "L" must be at least 234ns wide if X_{IN}=30MHz with no division.
- IR bit may change to "1" (interrupt requested) when switching the polarity of the $\overline{\text{INT}}$0 to $\overline{\text{INT}}$5 pins. Set the IR bit to "0" (no interrupt requested) after selecting the polarity. Figure 25.1 shows an example of the switching procedure for the $\overline{\text{INT}}$ interrupt.

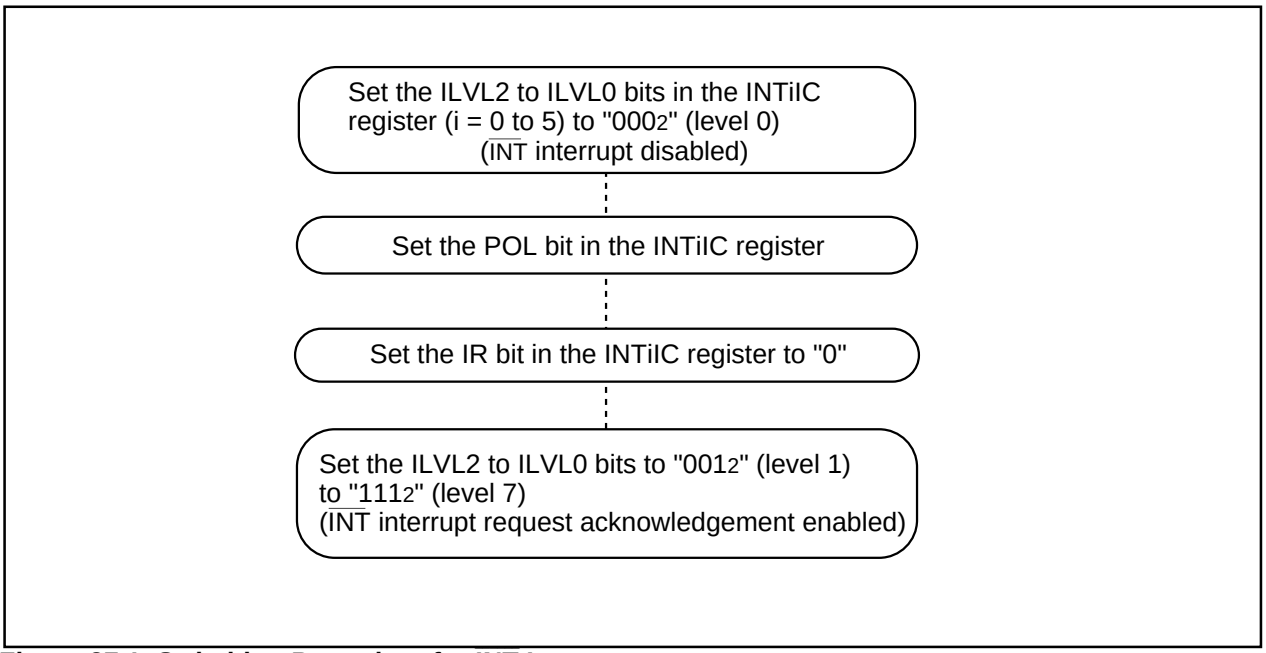


Figure 27.1 Switching Procedure for $\overline{\text{INT}}$ Interrupt

27.6.4 Watchdog Timer Interrupt

Reset the watchdog timer after a watchdog timer interrupt occurs.

27.6.5 Changing Interrupt Control Register

To change the interrupt control register while the interrupt request is disabled, follow the instructions below.

Changing Bits Except IR Bit : When an interrupt request occurs while executing an instruction, the IR bit may not be set to "1" (interrupt requested) and the interrupt may be ignored. If this is a problem, use the following instructions to change the register.
AND, OR, BCLR, BSET

Changing IR bit: The IR bit may not change to "0" (no interrupt requested) depending on the instructions written. If this is a problem, use the following instruction to change the register.
MOV

27.6.6 Changing IIOiIR Register (i = 0 to 11)

Use the following instructions to set bits 1 to 7 in the IIOiIR register to "0" (no interrupt requested).
AND, BCLR

27.6.7 Changing RLVL Register

The DMAII bit is indeterminate after reset. When using the DMAII bit to generate an interrupt, set the interrupt control register after setting the DMACII bit to "0" (interrupt priority level 7 available for interrupts).

27.7 DMAC

- Set DMAC-associated registers while the MDi1 to MDi0 bits (i=0 to 3) in the channel to be used are set to "00$_2$" (DMA disabled). Set the MDi1 to MDi0 bits to "01$_2$" (single transfer) or "11$_2$" (repeat transfer) at the end of the setup procedure to start DMA requests.

- Do not set the DRQ bit in the DMiSL register to "0" (no request).
  When a DMA request is generated but the receiving channel is not ready to receive(1), the DMA transfer is not performed and the DRQ bit is set to "0".

  NOTES:
  1. The MDi1 to MDi0 bits are set to "00$_2$" or the DCTi register is set to "0000$_{16}$" (transferred 0 times).

- To start a DMA transfer by a software trigger, set the DSR bit and DRQ bit in the DMiSL register to "1" simultaneously.
  e.g.,
  OR.B #0A0h,DMiSL Set the DSR and DRQ bits to "1" simultaneously.

- Do not generate a channel i DMA request when setting the MDi1 to MDi0 bits in the DMDj register (j=0,1) corresponding to channel i to "01$_2$" (single transfer) or "11$_2$" (repeat transfer), if the DCTi register of channel i is set to "1"
  Select the peripheral function which causes the DMA request after setting the DMA-associated registers. If none of the conditions above (setting $\overline{\text{INT}}$ interrupt as DMA request source) apply, do not write "1" to the DCTi register.

- Enable DMA(1) after setting the DMiSL register (i=0 to 3) and waiting 6 BCLK cycles or more by program.

NOTES:
1. DMA is enabled when the values set in the MDi1 to MDi0 bits in the DMDj register are changed from "00$_2$" (DMA disabled) to "01$_2$" (single transfer) or "11$_2$" (repeat transfer).

27.8 Timer

27.8.1 Timers A and B

The timers stop after reset. Set the TAiS(i=0 to 4) bit or TBjS(j=0 to 5) bit in the TABSR register or TBSR register to "1" (starts counting) after setting operation mode, count source and counter.

Set the following registers and bits while the TAiS bit or TBjS bit is set to "0" (stops counting).

- TAiMR, TBjMR register
- TAi, TBj register
- UDF register
- TAZIE, TA0TGL, TA0TGH bits in the ONFS register
- TRGSR register

27.8.2 Timer A

27.8.2.1 Timer A (Timer Mode)

(a) The TAiS bit (i=0 to 4) in the TABSR register is set to "0" (stops counting) after reset. Set TAiS bit to "1" (starts counting) after selecting operation mode and setting the TAi register.

(b) The TAi register indicates the counter value during counting at any given time. However, the counter will read "FFFF$_{16}$" when reloading. The setting value can be read after setting the TAi register while the counter is stopped and before the counter starts counting.

(c) TA1$_{OUT}$, TA2$_{OUT}$, TA4$_{OUT}$ pins are placed in a high-impedance state when an "L" signal is applied to the $\overline{NMI}$ pin while INV03 to INV02 bits in the INVC0 register are set to "11$_2$" (forced cutoff of the three-phase output by low-level signal ("L") applied to $\overline{NMI}$ pin)

27.8.2.2 Timer A (Event Counter Mode)

(a) TAiS (i=0 to 4) bit in the TABSR register is set to "0" (stops counting) after reset. Set the TAiS bit to "1" (starts counting) after selecting operation mode and setting the TAi register.

(b) The TAi register indicates the counter values during counting at any given time. However, the counter will read "FFFF$_{16}$" during underflow and "0000$_{16}$" during overflow, when reloading. The setting value can be read after setting the TAi register while the counter is stopped and before the counter starts counting.

(c) The TA1$_{OUT}$, TA2$_{OUT}$, TA4$_{OUT}$ pins are placed in a high-impedance state when an "L" signal is applied to the $\overline{NMI}$ pin while the INV03 to INV02 bit in the INVC0 register are set to "11$_2$" (forced cutoff of the three-phase output by low-level signal ("L") applied to $\overline{NMI}$ pin).

27.8.2.3 Timer A (One-shot Timer Mode)

(a) TAiS (i=0 to 4) bit in the TABSR register is set to "0" (stops counting) after reset. Set TAiS bit to "1" (starts counting) after selecting operation mode and setting the TAi register.

(b) The followings occur when setting the TABSR register to "0" (stops counting) while counting:

- The counter stops counting and the microcomputer reloads contents of the reload register.
- The TAi$_{OUT}$ pin becomes low ("L").
- The IR bit in the TAiIC register is set to "1" (interrupt requested) after 1 CPU clock cycle.

(c) The output of the one-shot timer is synchronized with an internal count source. When set to an external trigger, there is a delay of 1 count source cycle maximum, from trigger input to the TAi$_{IN}$ pin to the one-shot timer output.

(d) The IR bit is set to "1" when the timer operation mode is selected as follows:
- one-shot timer mode is selected after reset.
- timer mode is switched to one-shot timer mode.
- event counter mode is switched to one-shot timer mode.

Therefore, set the IR bit to "0" by program when generating a timer Ai interrupt (IR bit), if the timer operation mode is selected as is described above.

(e) When a trigger is generated while counting, the reload register reloads and continues counting after the counter has downcounted once following a re-trigger. To generate a trigger while counting, wait at least 1 count source cycle after the previous trigger has been generated and generate a re-trigger.

(f) TA1OUT, TA2OUT, TA4OUT pins are placed in a high-impedance state when an "L" signal is applied to the $\overline{\text{NMI}}$ pin while the INV03 to INV02 bits in the INVC0 register is set to "11$_2$" (forced cutoff of the three-phase output by low-level signal ("L") applied to $\overline{\text{NMI}}$ pin).

27.8.2.4 Timer A (Pulse Width Modulation Mode)

(a) TAiS(i=0 to 4) bit in the TABSR register is set to "0" (stops counting) after reset. Set TAiS bit to "1" (starts counting) after selecting an operating mode and setting the TAi register.

(b) The IR bit is set to "1" when the timer operation mode is selected as follows:
- PWM mode is selected after reset.
- timer mode is switched to PWM mode.
- event counter mode is switched to PWM mode.

Therefore, set the IR bit to "0" by program when generating a timer Ai interrupt (IR bit), if the timer operation mode is selected as is described above.

(c) The followings occur when the TAiS bit is set to "0" (stops counting) while PWM pulse is output:
- The counter stops counting.
- The IR bit changes to "1" and the output level changes to low ("L") when TAiOUT pin is held high ("H").
- The IR bit and the output level remain unchanged when TAiOUT pin is held low ("L").

(d) TA1OUT, TA2OUT, TA4OUT pins are placed in a high-impedance state if "L" signals are applied to the $\overline{\text{NMI}}$ pin while the INV03 to INV02 bits in the INVC0 register are set to "1" (three-phase output forced cutoff enabled).

27.8.3 Timer B

27.8.3.1 Timer B (Timer Mode, Event Counter Mode)

(a) TBiS (i=0 to 5) bit is set to "0" (stops counting) after reset. Set TBiS bit to "1" (starts counting) after selecting an operation mode and setting the TBi register.
The TB0S to TB2S bits are the bits 5 to 7 in the TABSR register. The TB3S to TB5S bits are bits 5 to 7 in the TBSR register.

(b) The TBi register indicates the counter value during counting at any given time. However, the counter will read "FFFF16" when reloading . The setting value can be read after setting the TBi register while the counter stops and before the counter starts counting.

27.8.3.2 Timer B (Pulse Period/Pulse Width Measurement Mode)

(a) The IR bit in the TBiIC register is set to "1" (overflow) when the valid edge of a pulse to be measured is input and when timer Bi overflows. The MR3 bit in the TBiMR register determines the interrupt cause within an interrupt service routine.

(b) Count overflow on a different timer if an interrupt cause cannot be determined by the MR3 bit, such as when a pulse to be measured is input at the same time the timer overflows.

(c) To set the MR3 bit in the TBiMR register to "0" (no overflow), set when the TBiS bit is set to "1" (count starts) and at least one count is counted after the MR3 bit is set to "1" (overflow).

(d) The IR bit of the TBiIC register is used to detect overflow only. Use the MR3 bit only to determine interrupt cause within an interrupt service routine.

(e) Indeterminate values are transferred to the reload register during the first valid edge input following the start of the count. Timer B interrupt request is not acknowledged at this time.

(f) The counter value is indeterminate at the start of a count. Therefore, the MR3 bit may change to "1" (overflow) and cause timer B interrupt requests to be generated, until a valid edge is input after the count begins.

(g) The IR bit may be set to "1" (interrupt requested) if the MR1 to MR0 bits in the TBiMR register are set to a different value after a count begins. If the MR1 to MR0 bits are rewritten, but to the same value as before, the IR bit remains unchanged.

(h) Pulse width measurement measures pulse width continuously. Use program to determine whether measurement results are high ("'H") or low ("L").

27.9 Three-Phase Motor Control Timer Functions

27.9.1 Changing TAi and TAi1 (i=1, 2, 4) Registers

Do not write to the TAi and TAi1 registers at the same time timer B2 underflows. Follow the procedure below when rewriting the TAi1 register.

(1) Write value to the TAi1 register

(2) Wait 1 timer Ai count source cycle

(3) Write the same value to the TAi1 register again

27.10 Serial I/O

27.10.1 Clock Synchronous Serial I/O Mode

27.10.1.1 Transmission / Reception

When the $\overline{RTS}$ function is used while an external clock is selected, the output level of the $\overline{RTSi}$ pin is held low ("L") indicating that the microcomputer is ready for reception. The transmitting microcomputer is notified that reception is possible. The output level of the $\overline{RTSi}$ pin becomes high ("H") when reception begins. Therefore, connecting the $\overline{RTSi}$ pin to the $\overline{CTSi}$ pin of the transmitting microcomputer synchronizes transmission and reception. The $\overline{RTS}$ function is disabled if an internal clock is selected.

$\overline{RTS}_2$ pin and CLK_2 pin are placed in a high-impedance state when an "L" signal is applied to the $\overline{NMI}$ pin while the INV02 to INV01 bits in the INVC0 register are set to "11_2" (forced cutoff of the three-phase output by low-level signal ("L") applied to $\overline{NMI}$ pin).

27.10.1.2 Transmission

When an external clock is selected while the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and received on the rising edge) and the external clock is held high ("H") or when the CKPOL bit is set to "1" (data is transmitted on the rising edge of the transfer clock and received on the falling edge) and the external clock is held low ("L"), meet the following conditions:

- Set the TE bit in the UiC1 register to "1" (transmit enabled)
- Set the TI bit in the UiC1 register to "0" (data in the UiBT register)
- Apply "L" signal to the $\overline{CTSi}$ pin if the $\overline{CTS}$ function is selected

27.10.1.3 Reception

Activating the transmitter in clock synchronous serial I/O mode generates the shift clock. Therefore, set for transmission even if the microcomputer is used for reception only. Dummy data is output from the TxDi pin while receiving.

If an internal clock is selected, the shift clock is generated when the TE bit in the UiC1(i=0 to 2) registers is set to "1" (receive enabled) and dummy data is set in the UiTB register. If an external clock is selected, the shift clock is generated when the external clock is input into CLKi pin while the TE bit is set to "1" (receive enabled) and dummy data is set in the UiTB register.

When receiving data consecutively while the RE bit in the UiC1(i=0 to 2) register is set to "1" (data in the UiRB register) and the next data is received by the UARTi reception register, an overrun error occurs and the OER bit in the UiRB register becomes "1" (overrun error). In this case, the UiRB register is indeterminate. When overrun error occurs, program both reception and transmission registers to retransmit earlier data. The IR bit in the SiRIC does not change when an overrun error occurs.

When receiving data consecutively, feed dummy data to the low-order byte in the UiTB register every time a reception is made.

When an external clock is selected while the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and received on the rising edge) and the external clock is held high ("H") or when the CKPOL bit is set to "1" (data is transmitted on the rising edge of the transfer clock and received on the falling edge) and the external clock is held low ("L"), meet the following conditions:

- Set the RE bit in the UiC1 register to "1" (receive enabled)
- Set the TE bit in the UiC1 register to "1" (transmit enabled)
- Set the TI bit in the UiC1 register to "0" (data in the UiTB register)

27.10.2 UART Mode

- Set the UiERE bit in the UiC1 register after setting the UiMR register.
- $\overline{RTS}_2$ and CLK_2 pins will enter a high-impedance state when a "L" signal is applied to the $\overline{NMI}$ pin while the INV03 to INV02 bits in the INVC0 register are set to "11_2" (forced cutoff of the three-phase output by low-level signal ("L") applied to $\overline{NMI}$ pin).

27.10.3 Special Mode 2

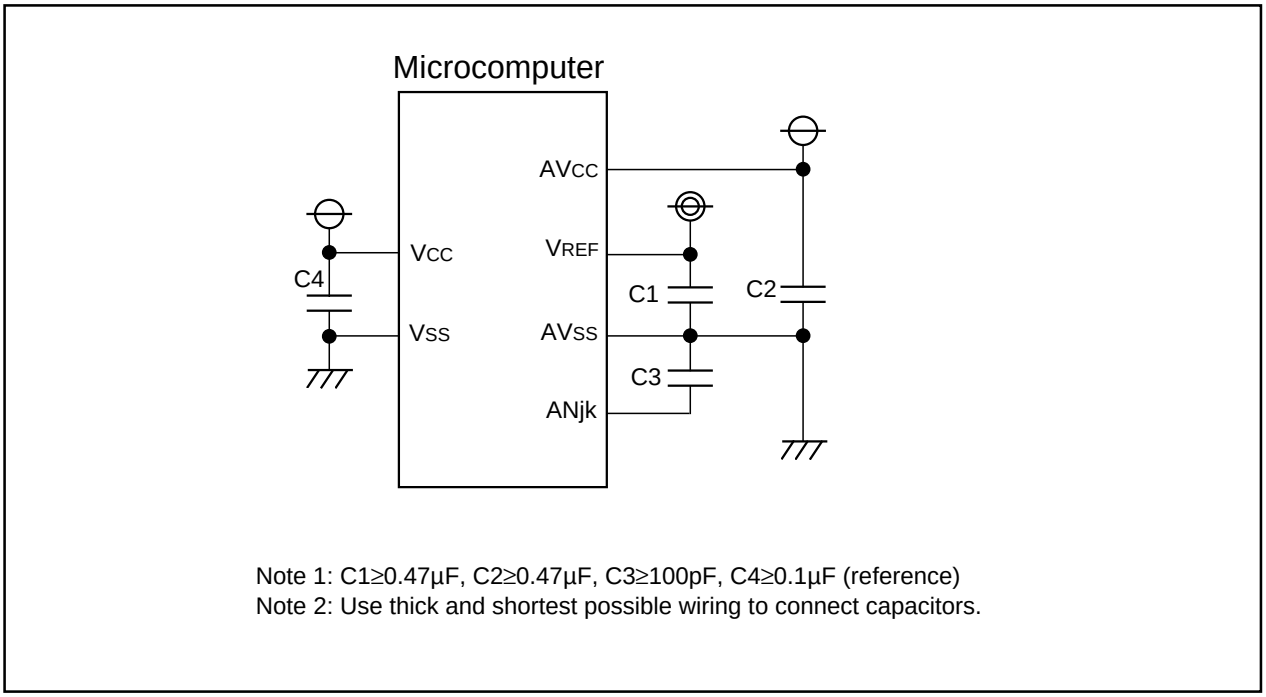
$\overline{RTS}_2$ and CLK_2 pins will enter a high-impedance state when a "L" signal is applied to the $\overline{NMI}$ pin while the INV03 to INV02 bits in the INVC0 register are set to "11_2" (forced cutoff of the three-phase output by low-level signal ("L") applied to $\overline{NMI}$ pin).

27.11 A/D Converter

- Set registers ADiCON0 (i=0,1) (bit 6 excluded), ADiCON1, and ADiCON2 while the A/D conversion is stopped (before trigger is generated).

- Wait a minimum of 1µs before starting the A/D conversion when changing the VCUT bit in the ADiCON1 register from "0" (V_{REF} no connection) to "1" (V_{REF} connection). Change the VCUT bit from "1" to "0" after the A/D conversion is completed.

- Insert capacitors between pins AV_{CC}, V_{REF}, analog input pin ANjk (j=none, 0, 2, 15; k=0 to 7) and AV_{SS} to prevent latch-ups and malfunctions due to noise and to minimize conversion errors. The same applies to pins V_{CC} and V_{SS}. Figure 27.2 shows the procedure.



Note 1: C1≥0.47µF, C2≥0.47µF, C3≥100pF, C4≥0.1µF (reference)
Note 2: Use thick and shortest possible wiring to connect capacitors.

Figure 27.2 Use of Capacitors to Reduce Noise

- Set the bit in the port direction register, which corresponds to the pin being used as the analog input, to "0" (input mode). Set the bit in the port direction register, which corresponds to $\overline{ADTRG}$, to "0" (input mode) if the TRG1 to TRG0 bits of the ADiCON2 register are set to "00_2" ($\overline{ADTRG}$).

- When generating a key input interrupt, do not use pins AN4 to AN7 as analog input pins (key input interrupt request is generated when the A/D input voltage becomes "L").

- When sample and hold function is not activated, $ØAD$ frequency must be 250kHz or more. If sample and hold function is activated, $ØAD$ frequency must be 1MHz or more.

- Set bits CH2 to CH0 in the ADiCON0 register or SCAN1 to SCAN0 in the ADiCON1 register to select analog input pins again when changing A/D conversion mode.

- Wrong values are stored in the ADij register (i=0,1; j=0 to 7) if the CPU reads the ADij register while the ADij register is storing results from a completed A/D conversion. This occurs when the CPU clock is set to a divided main clock or a sub clock.
  In one-shot mode or single sweep mode, read the corresponding ADij register after verifying that the A/D conversion has been completed. The completion of the A/D conversion can be determined by the IR bit in the ADiIC register.
  In repeat mode, repeat sweep mode 0 and repeat sweep mode 1, use an undivided main clock as the CPU clock.

- Conversion results of the A/Di is indeterminate if the ADST bit in the ADiCON0 register (i=0,1) is set to "0" (A/D conversion stopped) and the conversion is forcibly terminated by program. ADij registers (j=0 to 7) not performing an A/D conversion may also be indeterminate.
  If A/Di is forcibly terminated, do not use any values obtained from the ADij registers.
  If either A/D0 or A/D1 is forcibly terminated while the ADS bit in the ADiCON2 register is set to "0" (channel replacement disabled), the other A/D converter, A/Di, will perform normally. The values of ADij registers not performing an A/D conversion remain unchanged.

27.12 Intelligent I/O

27.12.1 Register Setting

Operations controlled by the values written to the GiBT (i=0 to 3), GiBCR1, BTSR, GjTMCR0 to GjTMCR7 (j=0,1), GiTPR6, GiTPR7, GjTM0 to GjTM7, GiPOCR0 to GiPOCR7, GiPO0 to GiPO7, G3MK4 to G3MK7, GjFS, GiFE, G2RTP, and G3RTP registers are affected by the count source (f_{BTi}) set in the BCK1 to BCK0 bits in the GiBCR0 register. Set the BCK1 to BCK0 bits before setting the GiBT, GiBCR1, BTSR, GjTMCR0 to GjTMCR7, GiTPR6, GiTPR7, GjTM0 to GjTM7, GiPOCR0 to GiPOCR7, GiPO0 to GiPO7, G3MK4 to G3MK7, GjFS, GiFE, G2RTP, and G3RTP registers.

Operations controlled by the values written to the GjRI, GjTO, GiCR, GiRB, GiMR, GjEMR, GjETC, GjERC, GjIRF, GiTB, GjCMP0 to GjCMP3, GjMSK0, GjMSK1, GjTCRC, GjRCRC, IECR, IEAR, IETIF, IERIF, and G3FLG registers are affected by the transfer clock. Set transfer clock before setting the GjRI, GjTO, GiCR, GiRB, GiMR, GjEMR, GjETC, GjERC, GjIRF, GiTB, GjCMP0 to GjCMP3, GjMSK0,GjMSK1, GjTCRC, GjRCRC, IECR, IEAR, IETIF, IERIF, and G3FLG registers.

27.12.2 BTSR Register Setting

The BTSR register is a located in the intelligent I/O group 2. When starting the base timer using the BTiS bit in the BTSR register, set the BTiS bit to "1" (base timer starts counting) after selecting the count source for the intelligent I/O group 2. If the BTiS bit is not being used, set the BTiS bit to "0" (base timer reset) after selecting the count source for the intelligent I/O group 2.

Set only either the BTiS bit or the BTS bit in the GiBCR1 register to "1" when starting the base timer. If both BTiS bit and the BTS bit are set to "0", both bits must be set "0" when stopping the base timer.

27.13 Programmable I/O Port

Because ports P7$_2$ to P7$_5$, P8$_0$, and P8$_1$ have the three-phase PWM output forced cutoff function, they are affected by the three-phase motor control timer function and the $\overline{\text{NMI}}$ pin when these ports are set for output functions (port output, timer output, three-phase PWM output, serial I/O output, intelligent I/O output).

Table 27.1 shows the relationship between the INVC0 register setting, the $\overline{\text{NMI}}$ pin input level and the state of output ports.

Table 27.1 INVC0 Register and the $\overline{\text{NMI}}$ Pin

Setting Value of INVC0 Register		Input Level to $\overline{\text{NMI}}$ Pin	States of P7$_2$ to P7$_5$, P8$_0$, and P8$_1$ Pins (when setting an output pin)
INV02 bit	INV03 bit		
0 (not using three-phase motor control function)	-	-	Output functions selected in the PS1, PSL1, PSC, PS2, and PSL2, registers
1 (using three-phase motor control timer function	0 (three-phase PWM output disabled)	-	High-impedance
	1 (three-phase PWM output enabled)(1)	H	Output functions selected in the PS1, PSL1, PSC, PS2, and PSL2, registers
		L (forcibly terminated)	High-impedance

NOTES :

1. The INV03 bit is set to "0" after low signal ("L") is applied to the $\overline{\text{NMI}}$ pin.

- The input threshold voltage differs with programmable I/O ports and peripheral functions. Therefore, if the level of the voltage applied to a pin shared by both programmable I/O ports and peripheral functions is not within the recommended operating condition, V_{IH} and V_{IL} (neither "H" nor "L"), the level determined will differ with programmable I/O ports and peripheral functions.

27.14 Flash Memory Version

27.14.1 Differences Between Flash Memory Version and Masked ROM Version

Due to differences in internal ROM and layout pattern, flash memory version and mask ROM version have varying electrical characteristics such as attributes, performance margins, noise endurance capacity, and noise radiation. When switching to masked ROM version, administer system evaluation tests equal to those held on the flash memory version.

27.15 Noise

Connect a bypass capacitor (approx. 0.1µF) between Vcc and Vss by shortest path, using thick wires.

27.16 Low Voltage Operations

The voltage down converter (VDC) is a circuit used to step down external supply voltage to the internal operation voltage of 3.3V. Disconnect the VDC when applying a 3.3V supply voltage to reduce power consumption.

Figure 27.3 shows the procedure for disconnecting the VDC.

Perform these settings immediately after reset, while the CPU clock is divided by 8. Do not set the VDC0 register ($001B_{16}$) to other values. Furthermore, do not write to the VDC0 register when applying a supply voltage of 3.3V or more.

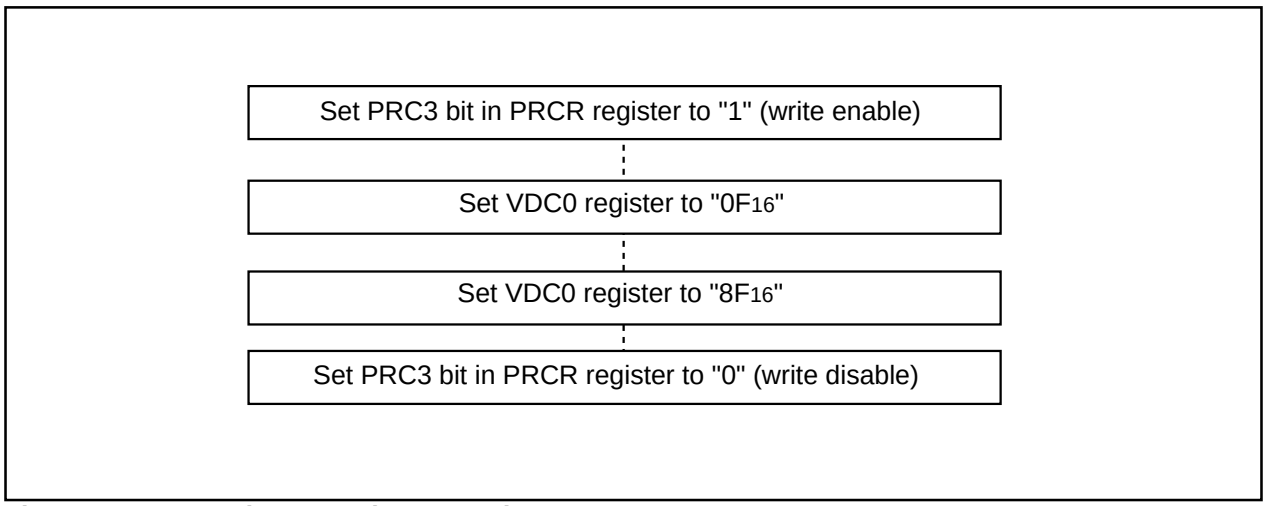


Figure 27.3 VDC Disconnection Procedure

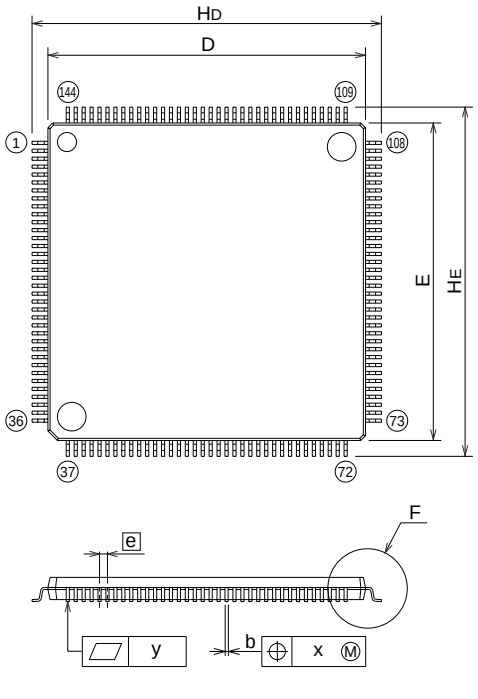
Package Dimensions

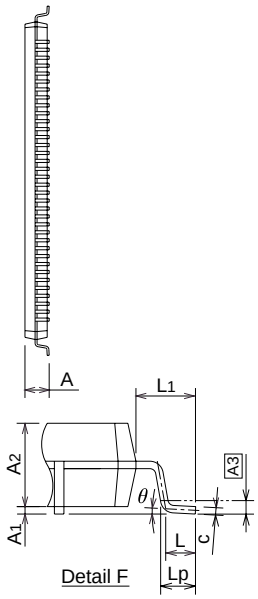
144P6Q-A

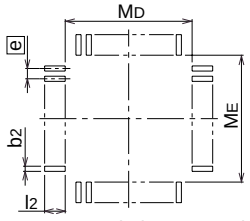
Recommended

Plastic 144pin 20×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	–	1.23	Cu Alloy







Recommended Mount Pad

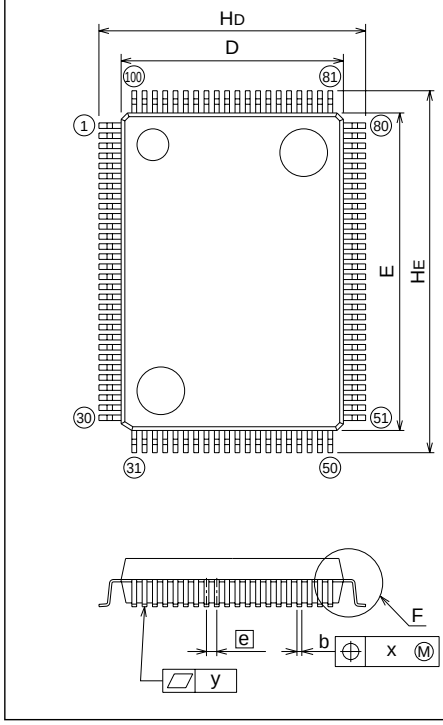
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	–	0.5	–
HD	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	0.95	–	–
MD	–	20.4	–
ME	–	20.4	–

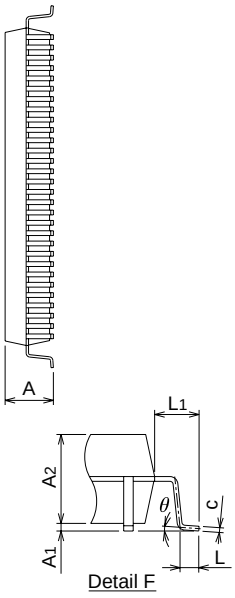
100P6S-A

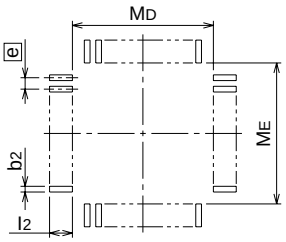
Recommended

Plastic 100pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42







Recommended Mount Pad

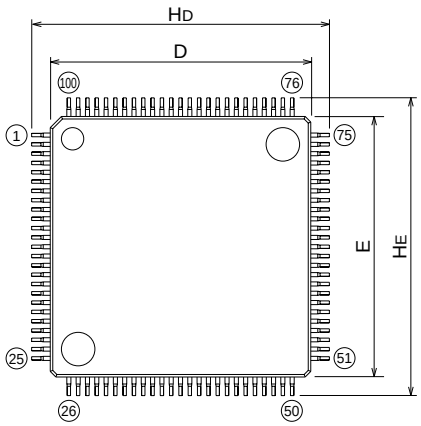
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
l2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

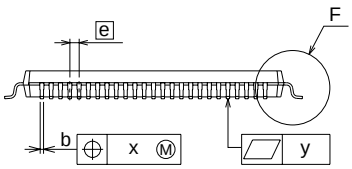
100P6Q-A

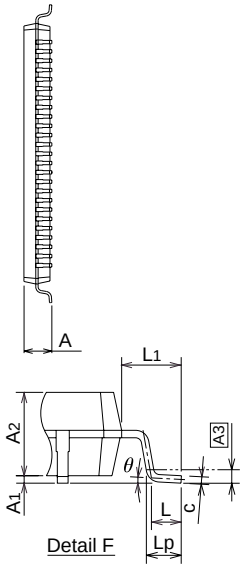
Recommended

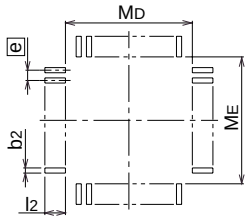
Plastic 100pin 14×14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–	0.63	Cu Alloy









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	14.4	–
ME	–	14.4	–

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Rev.	Date	Description	
		Page	Summary
1.01	**2002-12**	All	**Full-fledged revision** • Modify the notation system of registers and bits
		23	**Reset** • Delete the figure “Device’s internal status after a reset is cleared”.
		65	**System Clock** • Modify the figure “Clock Generation Circuit”. • Add descriptions about the ‘PLL clock’. • Modify the figure “Status Transition”.
		88	**Interrupt** • Modify the figure “Intelligent I/O Interrupt and CAN Interrupt”. • Add tables ‘registers to be used and settings’. • Change symbols of the bits in the interrupt request register. • Change symbols of the bits in the interrupt enable register.
		137	**Timer A** • Modify the figure “Timer A Configuration”. • Add tables ‘registers to be used and settings’.
		154	**Timer B** • Modify the figure “Timer B Configuration”. • Add tables ‘registers to be used and settings’.
		163	**Three-Phase Control Timer Function** • Change the bit name, the ‘INV17bit’ in the INVC1 register to reserved bit.
		174	**Serial I/O** • Modify the figure “UARTi Block Diagram”. • Add the table ‘registers to be used and settings’ in each mode. • Add distributions about the ‘clock-divided synchronous function (GCI mode)’. • Add descriptions about the ‘bus conflict detect function (IE mode)’.
		264	**Intelligent I/O** • Modify the figure “Intelligent I/O Group 0 Block Diagram”. • Modify the figure “Intelligent I/O Group 1 Block Diagram”. • Modify the figure “Intelligent I/O Group 2 Block Diagram”. • Modify the figure “Intelligent I/O Group 3 Block Diagram”. • Add the table ‘registers and settings’ associated with each function and mode. • Add a bit function of ‘the BCK0 to BCK1 bit in the G0BCR0 to G3BCR0 register’. -Group 0 and 1 • Add descriptions about the ‘HDLC data processing mode’. -Group 0 and 1 • Add distributions about the ‘IEBus mode’. -Group2 • Add descriptions about the ‘8-bit and 16-bit clock synchronous serial I/O function’. -Group3

Rev.	Date	Description	
		Page	Summary
		338	**A/D Convertor** • Modify the figure “A/D Convertor Block Diagram”. • Add the table ‘pin settings’.
		355	**D/A Convertor** • Add the table ‘pin settings’.
		394	**Usage Precaution** • Add descriptions about the ‘PLL synthesizer’. • Add descriptions about the ‘Timer A’ and ‘Timer B’. • Add descriptions about the ‘Low-Voltage Operation’.
1.02	**2003-1**		**Overview**
		2-3	• Add -40 to 85°C to ‘Operating ambient temperature’ row in Table 1.1.1 and 1.1.2.
		3	• Delete 8-bit or 16-bit clock synchronous serial I/O:1 channel (group3) on ‘Peripheral function’ row in Table 1.1.2.
			SFR
		33	• Modify 00?0 X000$_2$ to 0000 X000$_2$ on ‘value after RESET’ column on ‘017B$_{16}$’ row.
			System Clock
		78	• Modify 0 to 1 on ‘PLC00’ column and ‘10MHz’ row in Table 1.8.2.
		78	• Modify the PLC02 to PLC0 bits and the PLC05 to PLC04 bits to the PLC0 register in the third step in Figure 1.8.13.
		80	• Modify 1 to 0 on ‘CM00’ column and ‘BCLK output’ row in Table 1.8.5.
			DMAC
		117	• Add the note 3 in Figure 1.11.2.
			Timer
		141	• Modify TA4 and TA1 to TA0 and TA2 on the TA1TGL and TA1TGH in the top figure of Table 1.14.5. • Modify TA4 and TA1 to TA1 and TA3 on the TA2TGL and TA2TGH in the top figure of Table 1.14.5. • Modify TA4 and TA1 to TA2 and TA4 on the TA3TGL and TA3TGH in the top figure of Table 1.14.5. • Modify TA4 and TA1 to TA3 and TA0 on the TA4TGL and TA4TGH in the top figure of Table 1.14.5.
			Serial I/O
		186	• Modify PD7_0=0 to PD7_2=0 on ‘PD7 register’ column and ‘CLK2 input’ row in Table 1.18.4.
		192	• Modify PD7_0=0 to PD7_2=0 on ‘PD7 register’ column and ‘CLK2 input’ row in Table 1.19.4.
		206	• Modify a function description on ‘UiRRM’ row in Table 1.20.9.

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		Page	Summary
		207	• Modify PD7_2=0 to PD7_0=0 on 'PD7 register' column and 'SRxD2 input' row in Table 1.20.11. • Modify PD7_0=0 to PD7_2=0 on 'PD7 register' column and 'CLK2 input' row in Table 1.20.11.
		216	• Modify PS3_4=0 to PS3_5=0 on 'PS3 register' column and 'CLK4 input' row in Table 1.20.23.
			CAN Module
		226	• Modify PSL2_2=0 to PSL2_1=0 on 'PSL1 and PSL2 registers' column and 'P8$_2$' row in Table 1.21.2.
			Intelligent I/O
		296	• Modify Setting value of the GiPO0 register to Setting value of the GiPOk register as n and m on the second figure in Figure 1.22.26.
		304	• Modify RxD to ISRxD on 'IPOL' row and TxD to ISTxD on 'OPOL' row in Figure 1.22.33.
		315	• Modify IPS=1 to IPS1=1 on IPS registers column and 'P11$_2$' row in Table 1.22.26.
		317	• Modify TCRCRC to TCRCE on 'CRC' row in Table 1.22.28. • Delete SIOiTR and SIOiRR and add SRTiR in note 3 in Table 1.22.28.
		320	• Modify IER to OER in note 1 in the second figure of Figure 1.22.42.
		324	• Modify SIOiTR to SIO2TR and SIO5RR to SIO2RR in Table 1.22.30 and 1.22.36.
		334	• Modify GiCR to G3CR in Table 1.22.41.
			DRAMC
		364	• Modify SRDF to SREF in note 3 in Figure 1.27.1.
		385	• Modify IOUTC1$_0$ to OUTC1$_0$ on 'PSC_3' row in Figure 1.28.14.
		388	• Modify P0 to P5 to P1 in note 1 in Table 1.28.17.
			Programable I/O Port
		390	• Modify INPC$_1$ to INPC1$_1$ on 'PS1 register' column and 'Bit 4' row in Table 1.28.4.
		391	• Modify INPC$_0$ to INPC0$_2$ on 'PS2 register' column and 'Bit 0' row in table 1.28.5.
		393	• Modify ISCLK input to ISCLK0 input on 'Bit 1' row in table 1.28.12.
			Usage Precaution
		394	• Modify PM0 to PM00 in "$\overline{\text{HOLD}}$ Signal" • Modify all SP to ISP in (1) SP Setting of "Interrupts".
		398	• Modify all TAi to TBi in 1. Timer Mode and Event Counter Mode of "Timer B".
		400	• Modify the CAN module to the microcomputer in "Resetting CNVSS Pin with H". • Delete a discription of 'Difference between Flash Memory version and Masked ROM'
			Electric Charactistics
		429	• Modify IOH=5mA to IOL=5mA on 'VOL' row and 'Mesurement Condition' column in Table 1.31.3.

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		Page	Summary
1.10	**2004-3**	All Pages	Chapter numbers, section numbers, etc., added; Table and Figure numbers modified; Chapter sequence modified; Word Phrasing in Revision History changed
			Overview
		2, 3	• **Tables 1.1 and 1.2 M32C/83 Group Performance** Shortest Instruction Execution Time modified: 31.3ns(f(BCLK)=30MHz changed to 31.3ns(f(BCLK)=32MHz, 50ns(f(BCLK)=20MHz added; Performance details of Multifunction Timer, Intelligent I/O, Clock Generating Circuit, and Electrical Characteristics revised; Oscillator Stop Detect Function added; 32MHz added to Supply Voltage and Power Consumption Note 3 added
		4	• **Figure 1.1 M32C/83 Block Diagram** modified
		5	• **Table 1.3 M32C/83 Group** Product deleted
		9, 13	• **Tables 1.4 and 1.5 Pin Characteristics** VREF pin changed from “analog pin” to “control pin”
		15 to 18	• **Table 1.6 Pin Description** SDA0 to SDA4 changed from “output” to “input”; Descriptions of A/D-related pin functions revised
			Centeral Processing Unit
		20	• **Figure 2.1 CPU Register** modified
			Memory
		23	• **Figure 3.1 Memory Map** Product deleted; Diagram modified
			SFR
		24 to 45	Value after reset and lisiting sequence modified • “? : Indetermination” changed to “X : Indeterminate” • Notation “Users cannot use any symbols with *” deleted • Register names, symbols, and Values after RESET of addresses $001F_{16}$ to 0025_{16}, 0030_{16} to 0035_{16}, 0055_{16} to 0056_{16}, $01AC_{16}$, and $01AE_{16}$ to $01BF_{16}$ deleted • Notations added to PM0 and TCSPR registers • Value after reset in the RLVL register modified
			Reset
		46	• **Figure 5.1 Reset Circuit** modified
		47	• **Figure 5.2 Reset Sequence** Diagram modified; Note 1 added
		48	• **5.3 Watchdog Timer Reset** added
		49	• **Figure 5.3 CPU Register after Reset** modified
			Processor Mode
		50	• **6.2.2 Applying Vcc to CNVss Pin** Contents added

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		Page	Summary
			Bus
		55	• **7.1.3.2 Multiplexed Bus** revised
		60	• **7.2.4 Bus Timing** revised
		64	• **7.6 $\overline{\text{RDY}}$ Signal** revised
		65	• **Figure 7.7 $\overline{\text{RD}}$ Signal Output Extended by $\overline{\text{RDY}}$ Signal** modified
			Clock Generating Circuit
			Chapter name changed from “System Clock “ to “Clock Generating Circuit”
		67	• **Table 8.1 Clock Generation Circuit Specifications** Main clock clock frequency modified; “Ceramic oscillator” changed to “Ceramic resonator”; Reference point added to PLL Frequency Synthesizer
		68	• **Figure 8.1 Clock Generation Circuit** revised
		69	• **Figure 8.2 CM0 Register** Bit 3 function changed from “Nothing is assigned” to “Reserved Bit”
		72	• **Figure 8.5 CM2 Register** CM21 bit function modified; Note 5 revised
		75	• **Figure 8.8 PLC1 Register** Note 3 revised; Note 4 added
		77	• **8.1.2 Sub Clock** revised
		79	• **Figure 8.11 Switching Procedure form On-chip Oscillator Clock to Main Clock** modified
			• **8.1.4 PLL Clock** revised
			• **Table 8.2 Bit Settings to Use PLL Clock as CPU Clock Source** Setting added for when f(X_{IN}) is 8MHz
		80	• **Figure 8.13 Procedure to Use PLL Clock as CPU Clock Source** modified
		81	• **8.2 CPU Clock and BCLK** revised
		84	• **8.5.2.2 Before Entering Wait Mode** revised
		85	• **8.5.2.5 Entering Wait Mode** added
		86	• **8.5.3 Stop Mode** revised
			• **8.5.3.1 Before Entering Stop Mode** revised
			• **8.5.3.3 Exiting Stop Mode** revised
		87	• **8.5.3.4 Entering Stop Mode** added
		88	• **Figure 8.15 Status Transition** modified
			Interrupts
		93	• **Table 10.1 Fixed Vector Table** Point of reference changed
		95	• **Table 10.2 Relocatable Vector Tables** Reserved Space added
		99	• **Figure 10.5 RLVL Register** Value after reset changed; Note 3 revised; Note 4 added
			• **10.6.2.3 RLVL2 to RLVL0 Bits** revised
		103	• **Figure 10.8 Interrupt Priority** “Oscillation Stop Detect” added
		104	• **Figure 10.9 Interrupt Priority Level Select Circuit** modified
		106	• **10.8 NMI Interrupt** revised

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		Page	Summary
		108	• "**10.11 Intelligent I/O and CAN Interrupt**" changed to "**10.11 Intelligent I/O Interrupt and CAN Interrupt**" • Precautions pertaining to Interrupts are compiled into one chapter, "**27. Precaution**"
			Watchdog Timer
		111	Contents revised
			DMAC
		115	• **12. DMAC** revised
		114	• **Table 12.1 DMAC Specifications** CAN interrupt added to DNA Request Factors; Note 1 revised • Precautions pertaining to DMAC are compiled into one chapter, "**27. Precaution**"
			DMAC II
		125	• **Table 13.1 DMAC II Specifications** Note 2 added
		126	• **Figure 13.1 RLVL Register** Values after reset modified; Note 3 revised; Note 4 added
		129	• **13.3 Transfer Data** Contents added
		130	• **13.4.2 Burst Transfer** revised • **13.4.4 Chain Transfer** revised
		132	• **13.5 Execution Time** revised
			Timer
		135	• **14.1 Timer A** Contents added
		140	• **Table 14.1 Pin Settings for Output from TAiOUT Pin (i= 0 to 4)** modified
		149	• **14.1.4 Pulse Width Modulation Mode** Settings changed for 16-bit PWM and 8-bit PWM
		152	• **14.2 Timer B** Contents added
		159	• **Figure 14.22 TB0MR to TB5MR Registers (Pulse Period/ Pulse Width Measurement Mode)** Values after reset modified
			Three-Phase Motor Control Timer Function
		161	• **Table 15.1 Three-Phase Motor Control Timer Functions Specification** modified
		162	• **Figure 15.1 Three-Phase Motor Control Function Block Diagram** modified
		163	• **Figure 15.2 INVC0 Register** modified
		164	• **Figure 15.3 INVC1 Register** modified
		166	• **Figure 15.5 ICTB2 Register, TA1, TA2, TA4, TA11, TA21 and TA41 Registers and TB2SC Register** Notes 2 and 3 added to ICTB2 register; Note 7 added to TAi and TAi1 registers
		168	• **Figure 15.7 TAiMR Register (i=1, 2, 4)** MR1 bit function modified

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		Page	Summary
		169	• **Figure 15.8 Triangular Wave Modulation Operation** modified
		170	• **Figure 15.9 Sawtooth Wave Modulation Operation** modified
			Serial I/O
		173	• **Figure 16.2 U0TB to U4TB Registers and U0RB to U4RB Registers** Note 3 added to U0RB to U4RB registers
		175	• **Figure 16.4 UiC0 Register** Note 3 added to UFORM bit
		176	• **Figure 16.5 UiC1 Register** Note 2 added to UiLCH bit; Note 1 added to SCLKSTPB (UiERE) bit
		181	• **Table 16.1 Clock Synchrnous Serial I/O Mode Specifications** Explanation of CLK Polarity in Selectable Functions revised
		182 to 219	• **Tables 16.2, 16.7, 16.12, 16.19, 16.24, and 16.34 Registers to be Used and Settings** Points of reference deleted
		183	• **Table 16.3 Pin Settings in Clock Synchronous Serial I/O Mode (1)** revised
		184	• **Figure 16.10 Transmit and Receive Operation** modified
		188	• **Table 16.7 Registers to be Used and Settings in UART Mode** Function of the UiERE bit in the UiC1 register modified
		189	• **Table 16.8 Pin Settings in UART (1)** revised
		190	• **Figure 16.14 Transmit Operation** modified
		192	• **Figure 16.17 Serial Data Logic Inverse** modified
		195	• **Table 16.12 Registers to be Used and Settings (I^2C Mode)** Setting values for master and slave indicated separately
		196	• **Table 16.13 I^2C Mode Functions** "$P6_1$, $P6_5$, $P7_2$, $P9_0$, $P7_5$ Pin Functions" changed to "$P6_1$, $P6_5$, $P7_2$, $P9_0$, $P9_5$ Pin Functions"
		197, 198	• **Tables 16.14 to 16.16 Pin Settings in I^2C Mode** modified
		200	• **16.3.4 Transfer Clock** revised
		203	• **Table 16.19 Registers to be Used and Settings in Special Mode 2** Functions of the UFORM bit in the UiC0 register and the UiRRM bit in the UiC1 register modified
		204	• **Table 16.20 Pin Settings in Special Mode 2 (1)** revised
			• **Table 16.21 Pin Settings in Special Mode 2 (2)** revised
			• **Table 16.22 Pin Settings in Special Mode 2 (3)** revised
		208	• **Table 16.23 GCI Mode Specifications** Explanations of Transmit/Receive Start Conditions revised
		210	• **Table 16.25 Pin Settings in GCI Mode (1)** revised
			• **Table 16.26 Pin Settings in GCI Mode (2)** revised
			• **Table 16.27 Pin Settings in GCI Mode (3)** revised
		213	• **Table 16.31 Pin Settings in IE Mode (2)** revised
			• **Table 16.32 Pin Settings in IE Mode (3)** revised
		219	• **Figure 16.29 SIM Interface Operation** modified

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		221	• **Figure 16.32 SIM Interface Format** modified
			A/D Converter
			Sequence of content modified
		223	• **Table 17.1 A/D Converter Specifications** Explanaition of A/D Conversion Start Conditions revised; ϕ A/D frequency modified
		226, 227	• **Figure 17.2 AD0CON0 Register, Figure 17.3 AD0CON1 Register** ϕ A/D frequency modified
		229, 230	• **Figure 17.5 AD1CON0 Register, Figure 17.6 AD1CON1 Register** ϕ A/D frequency modified
		232	• **Table 17.4 One-shot Mode Specifications** Explanation of Start Condition revised
		235	• **Table 17.9 Trigger Select Function Settings** Table modified; Note 2 added
		237	• **Figure 17.9 Analog Input Pin and External Sensor Equivalent Circuit** Capacitance of the capacitor modified
		238 to 247	Sequence of the following Chapters have been changed: **D/A Converter, CRC Calculation, XY Conversion**
			Intelligent I/O
		248	• **Figure 21.2 Intelligent I/O Group 1 Block Diagram** modified
		251	• **Figure 21.5 G0BT to G3BT Registers and G0BCR0 to G3BCR0 Registers** Note 2 added to G0BT to G3BT registers, Note 3 deleted from G0BCR0 to G3BCR0 registers
		252	• **Table 21.2 Base Timer Specifications** Explanation of Counter increment/ decrement mode in Selectable Function modified
		263	• **Tables 21.3, 21.6, 21.8, 21.17, 21.23, 21.29, 21.31, 21.37, and 21,42 Associated Register Settings** Point of reference deleted
		266	• **Figure 21.18 Counter Increment Mode (Group 0 and 1)** modified
		265	• **Figure 21.19 Counter Increment/Decrement Mode (Group 0 and 1)** modified
		266	• **Figure 21.20 Base Timer Operation in Two-Phase Pulse Signal Processing Mode** Note 1 revised
		267	• **21.2 Time Measurement Function (Group 0 and 1)** Contents added
		270	• **Figure 21.22 Time Measurement Function (2)** modified
		271	• **Figure 21.23 Prescaler Function and Gate Function** Diagram modified; Note 2 of Gate Function deleted
		272	• **Table 21.7 Pin Settings for Waveform Generation Function** modified
		273	• **Table 21.8 Waveform Generation Function Associated Register Settings** Note 1 added
		274	• **21.3.1 Single-Phase Waveform Output Mode (Group 0 to 3)** revised
			• **Table 21.9 Single-Phase Waveform Output Mode Specifications** revised
		275	• **Figure 21.24 Single-Phase Waveform Output Mode** modified

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		276	• **Table 21.10 Phase-Delayed Waveform Output Mode Specifications** revised
		277	• **Figure 21.25 Phase-Delayed Waveform Output Mode** modified
		278	• **21.3.3 Set/Reset Waveform Output (SR Waveform Output) Mode** revised
			• **Table 21.11 SR Waveform Output Mode Specifications** revised
		280	• **Figure 21.26 SR Waveform Output Mode** modified
		281	• **21.3.4 Bit-Modulation PWM Output Mode** revised
			• **Table 21.12 Bit Modulation PWM Output Mode** revised
			• **Figure 21.27 Bit Modulation PWM Mode** Pulse numbering added
		283	• **21.3.5 Real-Time Port (RTP) Output Mode (Group 2 and 3)** revised
			• **Table 21.14 RTP Output Mode Specifications** Note 1 added
		284	• **Figure 21.29 Real-Time Port Output Mode** modified
		285	• **21.3.6 Parallel Real-Time Port Output Mode (Group 2 and 3)** revised
			• **Table 21.15 Parallel RTP Output Mode** Note 1 added
		286	• **Figure 21.31 Parallel RTP Output Mode** modified
		290	• **Figure 21.35 G0EMR to G1EMR Registers and G0ETC to G1ETC Registers** Note 1 added
		291	• **Figure 21.36 G0ERC to G1ERC Registers** Note 1 added
		292	• **Figure 21.37 G0IRF to G1IRF Registers and G0TB to G1TB Registers** Notes 1 and 2 in G0IRF to G1IRF registers revised; Note 1 added to G0TB to G1TB registers
		293	• **Figure 21. 38 G0CMP0 to G0CMP3 Registers, G1CMP0 to G1CMP3 Registers, G0MSK0 to G0MSK1 Registers, G1MSK0 to G1MSK1 Registers, G0TCRC to G1TCRC Registers, and G0RCRC to G1RCRC Registers** Note 1 revised and Note 2 added to G0TCRC to G1TCRC registers; Note 3 in G0RCRC to G1RCRC registers revised
		294	• **Table 21.16 Clock Synchronous Serial I/O Mode Specifications (Group 0 and 1)** Explanation of transfer clock revised
		297	• **Table 21.22 UART Mode Specifications (Group 0 and 1)** Explanation of transfer clock and Note 2 revised
		301	• **Table 21.28 HDLC Processing Mode Specifications (Group 0 and 1)** Explanation of transfer clock revised
		308	• **Table 21.30 Variable Clock Synchronous Serial I/O Mode Specifications (Group 2)** Explanation of transfer clock revised
		312	• **Table 21.36 IE Bus Mode Specification** Explanation of transfer clock revised
		318	• **Table 21.41 Clock Synchronous Serial I/O Mode (Group 3)** Explanation of transfer clock revised
			CAN
		322	Bit symbols of each register are now capitalized (e.g. Reset0 is changed to RESET0)

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		Page	Summary
		325	• **22.1.1.3 BASICCAN Bit** revised
		344	• **22.1.16 CANi Message Slotj Control Register (CiMCTLj Register) (i=0, 1; j=0 to 15)** Funtion of the INVALDATA/TRMACTIVE bit when set to "1" changed to "Transmits"; Note 4 in REMACTIVE deleted; RW modified to RO • **Table 22.4 C0MCTLi Register (i=0 to 15) Setting and Transmit/Receive Mode** Hyphens (-) changed to "0"
		345	• **22.1.16.4 REMACTIVE Bit** revised
		346	• **22.1.16.5 RSPLOCK Bit** revised
			Programmable I/O Port
		364	• **24.4 Function Select Register Bk (PSLk Register) (k=0 to 3)** revised
		365	• **24.5 Function Select Register C (PSC Register)** revised • **24.7 Port Control Register (PCR Register)** revised
		367	• **Figure 24.2 Programmable I/O Ports (2)** modified
		369	• **Figure 24.5 PD0 to PD15 Registers** Note 4 added
		371	• **Figure 24.7 PS0 Register and PS1 Register** PS0 register revised
		372	• **Figure 24.8 PS2 Register and PS3 Register** PS3 register revised
		376	• **Figure 24.12 PSL0 Register and PSL1 Register** Note 1 added to PSL1 register
		377	• **Figure 24.13 PSL2 Register and PSL3 Register** PSL3 register revised
		378	• **Figure 24.14 PSC Register** revised
		379	• **Figure 24.15 PUR0 Register, PUR1 Register and PUR2 Register** Note 1 revised
		383	• **Table 24.3 Port P6 Peripheral Function Output Control** Bits 3 and 7 modified • **Table 24.4 Port P7 Peripheral Function Output Control** Note 1 added to PSC register; Bit 0 modified
		384	• **Table 24.6 Port P9 Peripheral Function Output Control** Bit 2 and 6 modified
			Flash Memory Version
		387	• **Table 25.1 Flash Memory Version Specifications** Supply voltage modified
		389	• **25.2.1 ROM Code Protect Function** revised • **25.2.2 ID Code Check Function** revised
		393	• **25.3.1.3 FMR02 Bit** revised
		395	• **25.3.3 Data Protect Function** revised
		397	• **25.3.5.3 Clear status Register** revised
		405	• **25.3.7.8 Rewriting the User ROM Area**
		406	• **25.4.2 ID Code Check Function** revised
		412	• **25.5.2 ROM Code Protect Function** revised

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		Page	Summary
			Electrical Characteristics
		413	• **Table 26.1 Absolute Maximum Ratings** VREF, XIN P70 and P71 deleted and XOUT added to Output Voltage
		414	• **Table 26.2 Recommended Operation Conditions (Vcc= 3.0V to 5.5V at Topr= -20 to 85°C)** Maximum value of 50MHz added to f(XCIN) Sub Clock Oscillation Frequency
		416	• **Table 26.4 A/D Conversion Characteristics** ϕAD frequency modified
		416, 434	• **Tables 26.6 Flash Memory Version Electrical Characteristics** added
			Precautions
		450 to 472	• Overall structure modified
1.20	**2004-6**	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
			Interrupts
		111	• **Figure 10.15 IIO0IE to IIO11IE Registers** Note 2 added
			Watchdog Timer
		112	• **Figure 11.1 Watchdog Timer Block Diagram** modified

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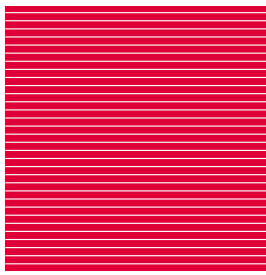

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