ColdFire MCF5282

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ColdFire MCF5282 - Contents

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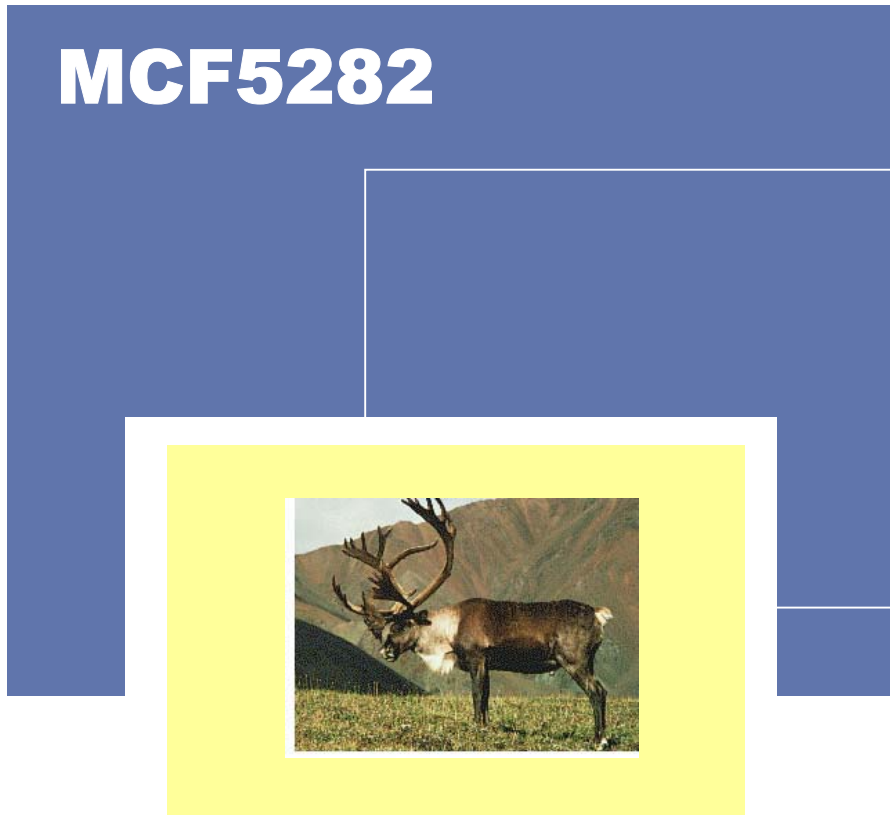


Target Markets and Applications

Market Trends Driving *ColdFire* Development

- Designers indicate that “Component Availability” with the right level of integration is one of the most critical design challenges causing changes in processor selection.
- Networking of applications that have been “stand alone” up to now
- Emerging markets are driving the growth of low-cost, high volume embedded control
- Customers demand clear documentation Quality and Quantity in terms of development tool support
- Increased number of applications being networked together
- Growing markets:
  - -Biometrics/security
  - -Distributed control applications used in industrial environments
  - -Health care equipment
  - -Network printing and wireless connectivity

Growing Demand for Embedded Ethernet

- Customers ranked Ethernet as the #1 feature to be integrated on future 32-bit Flash MCUs.
- Field experts ranked Ethernet as the #1 feature to be integrated on future 32-bit Flash MCUs from Motorola (next highest: LCD controller, 17%).
- According to Dataquest, the projected volumes for Ethernet-enabled ICs in the home networking market alone will top $740 million in 2003.
- Industrial controls integrating Ethernet are now appearing ~ the migration from CAN to Ethernet has begun.

MCF5282 Target Markets

- "Traditional" MCU applications that need to be networked
- Industrial Networked Control
  - ✓ CAN (DeviceNet) networked applications
  - ✓ CAN (DeviceNet) to Ethernet network migration
  - ✓ Ethernet networked applications
  - ✓ Ethernet to CAN (DeviceNet) gateways

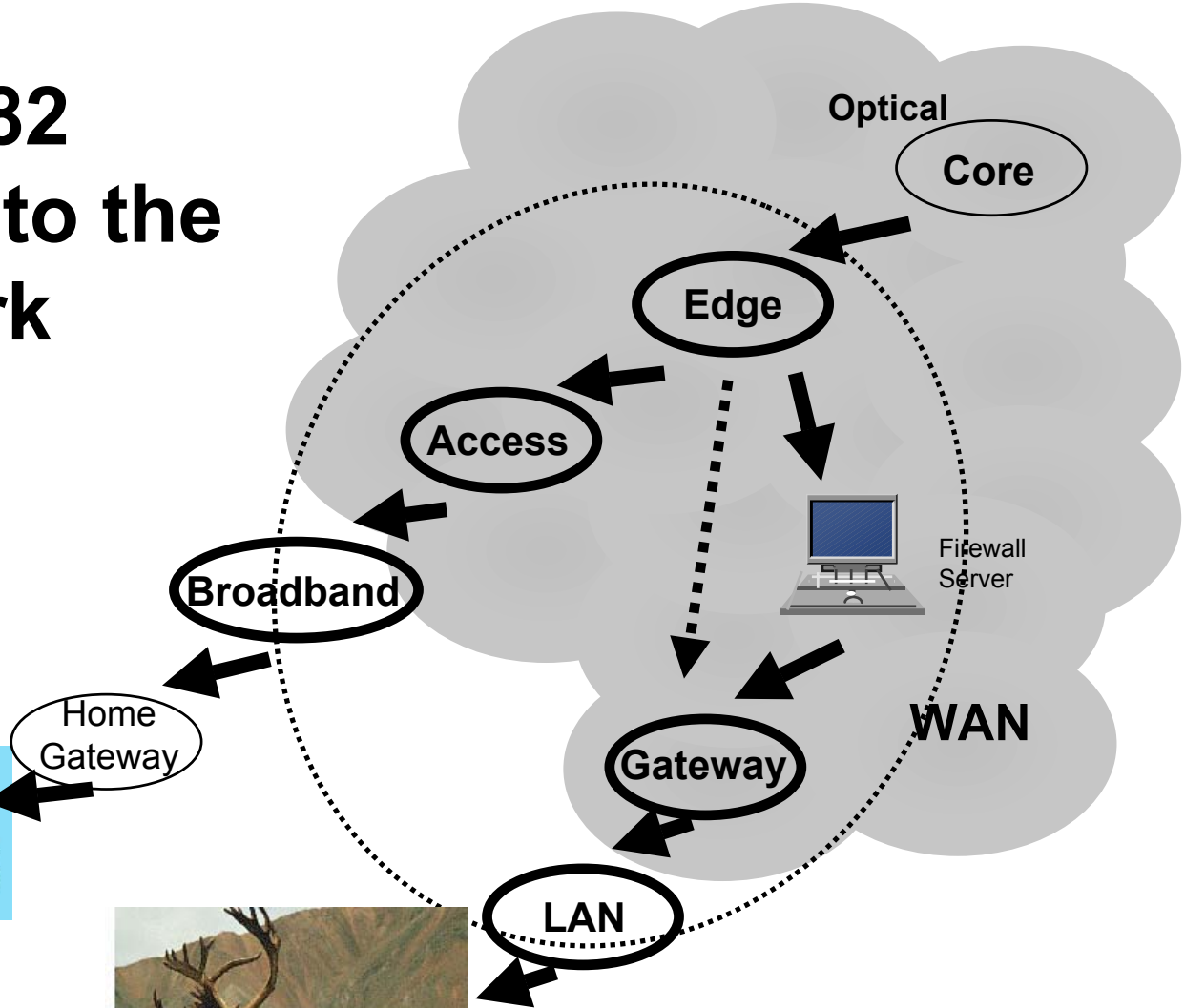
- "Emerging" low to medium complexity connected control applications
- Medium complexity un-connected control applications

MCF5282 Target Applications

- Medical Instrumentation
  - *S/5 Network*
- Food Service Equipment
  - *NAFEM On-line Kitchen Protocol*
- Home Automation
  - *Web Interface for X-10 Devices*
- Industrial Control Networking
  - *Ethernet to DeviceNet Gateway*
- Security
  - *Remote access, Camera control*
- Lighting control
- And many, many more!!!

MCF5282 Connected to the Network

Home
Small Commercial
SOHO/SOBO



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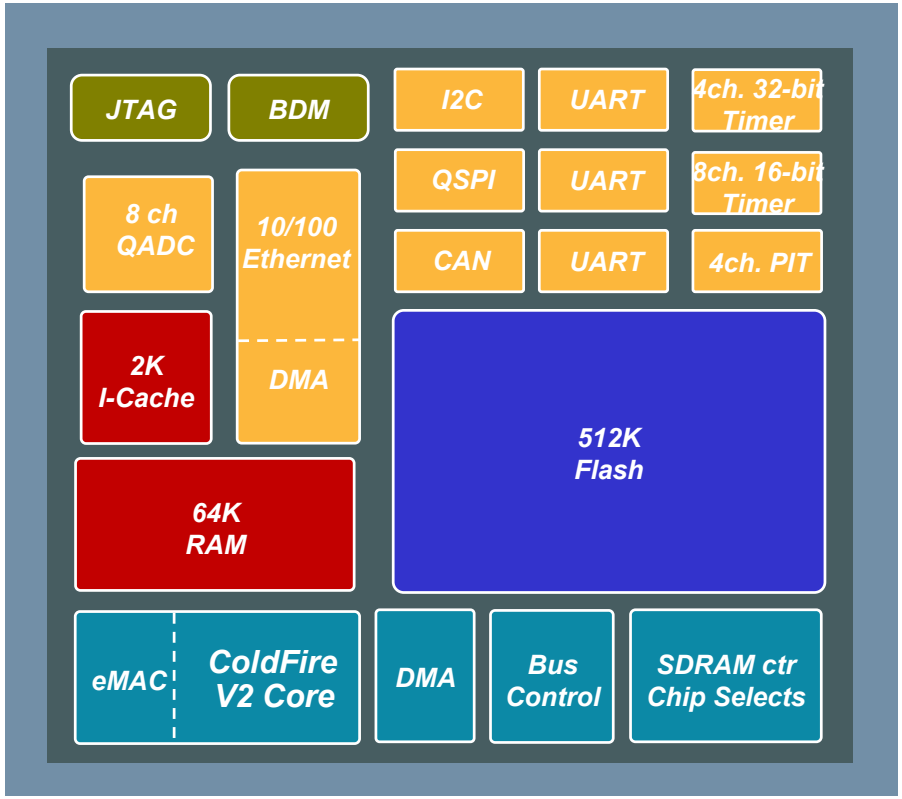
MCF5282 System Overview

ColdFire : MCF5282

Features

- ColdFire V2 core
  - 59 Dhrystone 2.1 MIPS at 66 MHz
  - Enhanced MAC Module
  - HW Divide
- Integrated Memory
  - 2K I-cache (* for off chip accesses only)
  - 64K RAM
  - 512K Flash (10K W/E cycles, 10 years data retention)
  - 0K Flash on MCF5280
- Integrated Peripherals
  - 10/100 Ethernet MAC (external PHY)
  - Enhanced CAN 2.0B Controller (FlexCAN)
  - 3 UARTs (2 with flow control)
  - Queued Serial Peripheral Interface (QSPI)
  - I2C bus interface
  - 8 ch. 16-Bit Capture/Compare/PWM timers
  - 4 ch. 32-bit timers with DMA
  - 8 ch. Queued 10-bit A-to-D converter
  - 4 ch. DMA controller
  - SDRAM Controller
  - 32-bit non-multiplexed data bus w/7 Chip Selects
  - Up to 152 General-Purpose I/O
  - System Integration (PLL, SW Watchdog)
  - Reset controller with “Brown-out” detection



Speed and Temperature

- 66MHz at -40°C to +85°C
- Planning a higher speed version at 0°C to +70°C

Package

- 256 Ball Plastic MAPBGA Package

RTXC™ Quadros™ for MCF5282

Summary

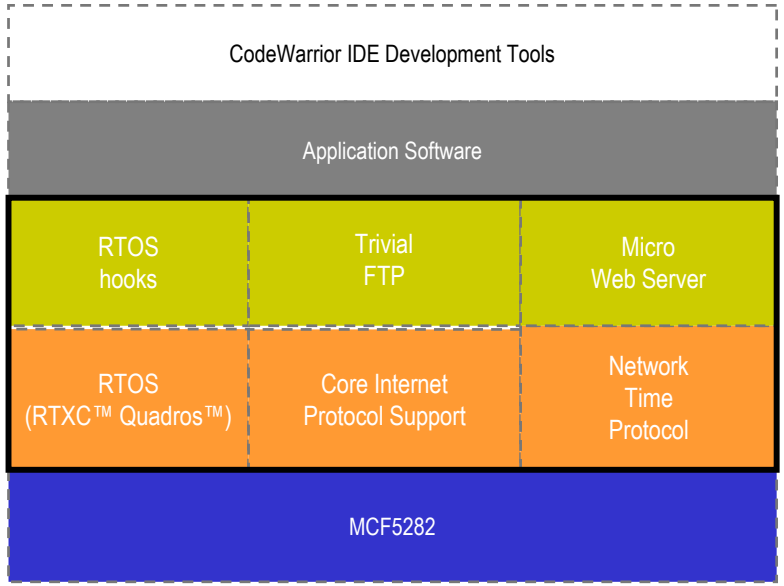
- Software suite supporting embedded networking, designed for ease of use and fast development for all users (from first time to experienced network users)

Features

- RTX™C Quadros™ Real Time Operating System
  - Scalable thread based Kernel
  - Scalable task based Kernel
  - Execute in place (Flash)
  - Small memory footprint (less than 50% of MCF5282 including networking)
  - High performance with low system latency
- Networking support
  - Ethernet driver
  - Core Internet protocols (IP, UDP, TCP, ICMP, ARP, DHCP)
  - Application-level protocol servers
    - HTTP (small web server)
    - TFTP (trivial FTP server for remote firmware updates)
  - Application-level protocol clients
    - SMTP (ability to send e-mail but not act as a relay server)
    - SNTP (retrieve time from a network NTP server)

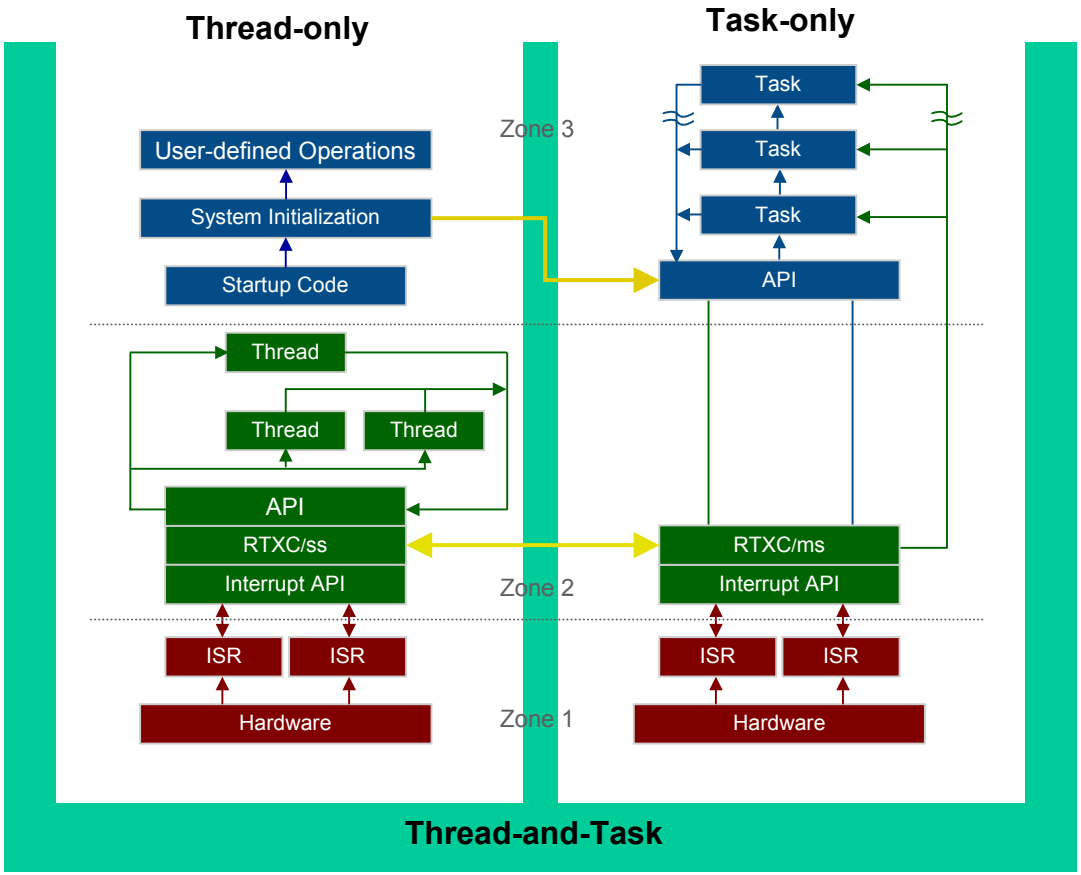
3 versions offering a range of pricing and functionality

- RTXC™ Quadros™ for MCF5282 **Special Edition**
  - Fixed binary image - Supporting a limited number of tasks and network connections. Suitable for basic Networking
    - FREE! (no NRE, no License, no Royalties)



- RTXC™ Quadros™ for MCF5282 **Standard Edition**
  - Configurable binary - Providing flexibility in number of tasks, network connections and memory requirements. Suitable for advanced embedded control and networking
    - <$20K License per Project
- RTXC™ Quadros™ for MCF5282 **Professional Edition**
  - Fully configurable/scalable Source Code - Supports a very wide range of configuration options for optimal performance and memory requirements
    - ~$50K License per Project

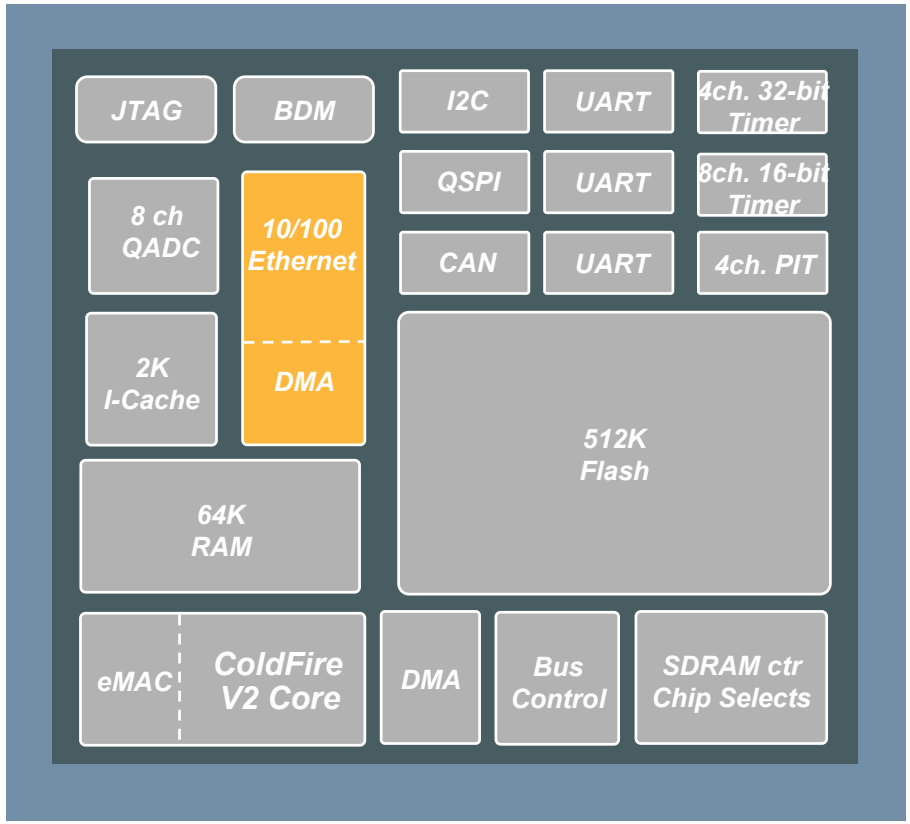
RTXC™ Quadros™ Architecture



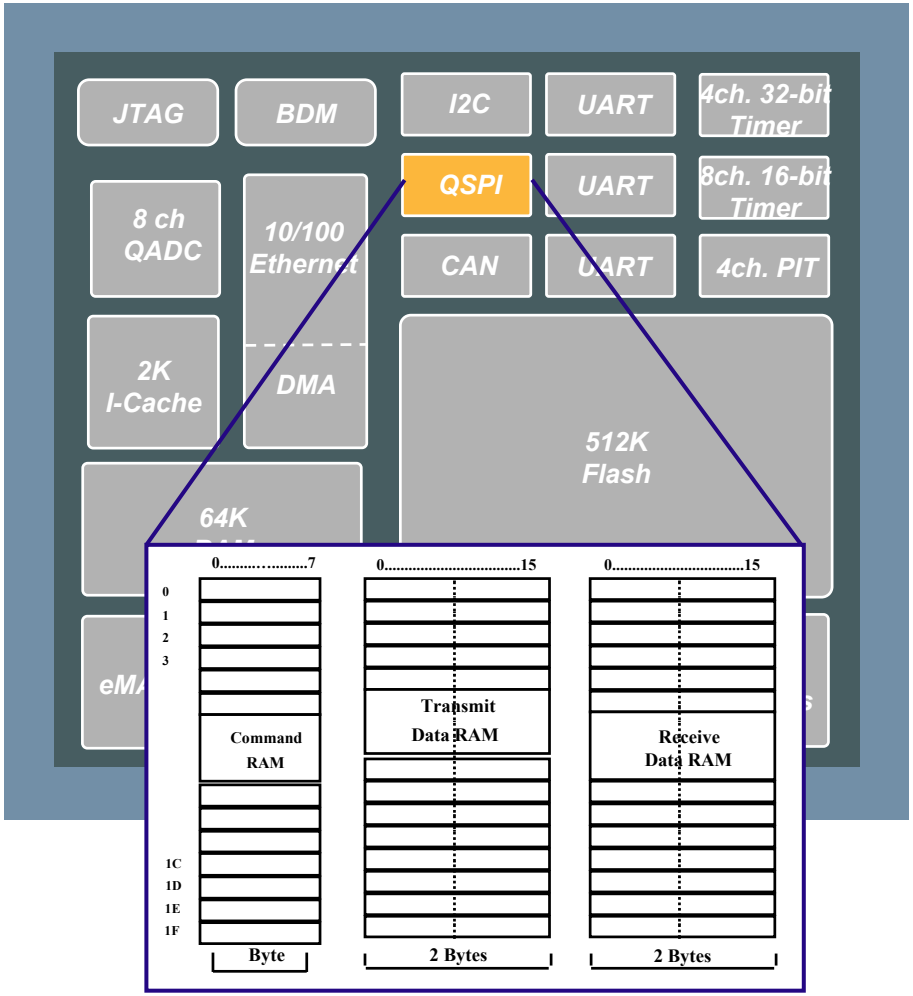
Communication Systems

10/100Mbit Fast Ethernet Controller (MAC)

- Fully IEEE 802.3 standard compliant
- Supported interfaces :
  - 10 Mbps 7-wire
  - 10/100 Mbps 18-wire MII
- Supported data rates :
  - 10 Mbps full duplex and half duplex operation
  - 100 Mbps half duplex operation
  - 100 Mbps full duplex operation when packet rate very low
- Dedicated DMA
- FIFOs :
  - 448 bytes on-chip transmit and receive FIFO to support a variety of bus latencies
  - Retransmission from FIFO following collision with no intervention
  - Automatic receive FIFO flushing for runts and collisions with no intervention
- Off-chip descriptor rings/buffers permit wide user capabilities and flexibility

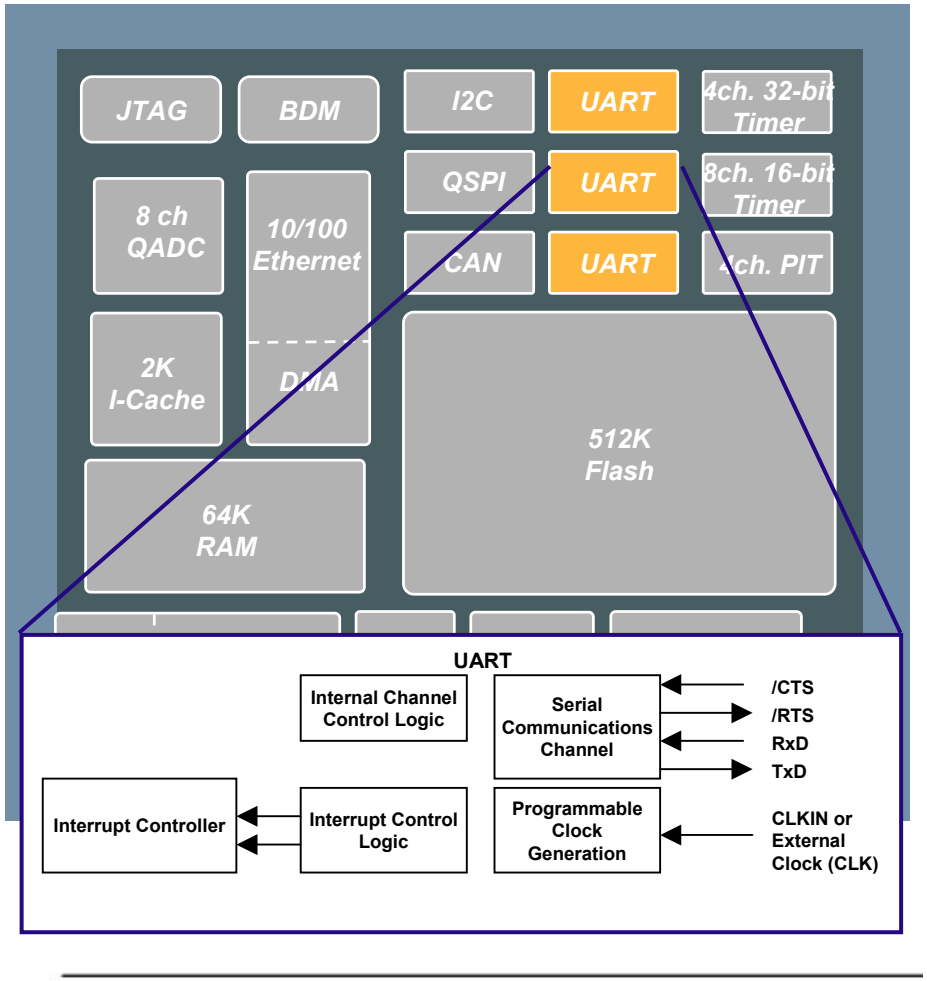


QSPI Module



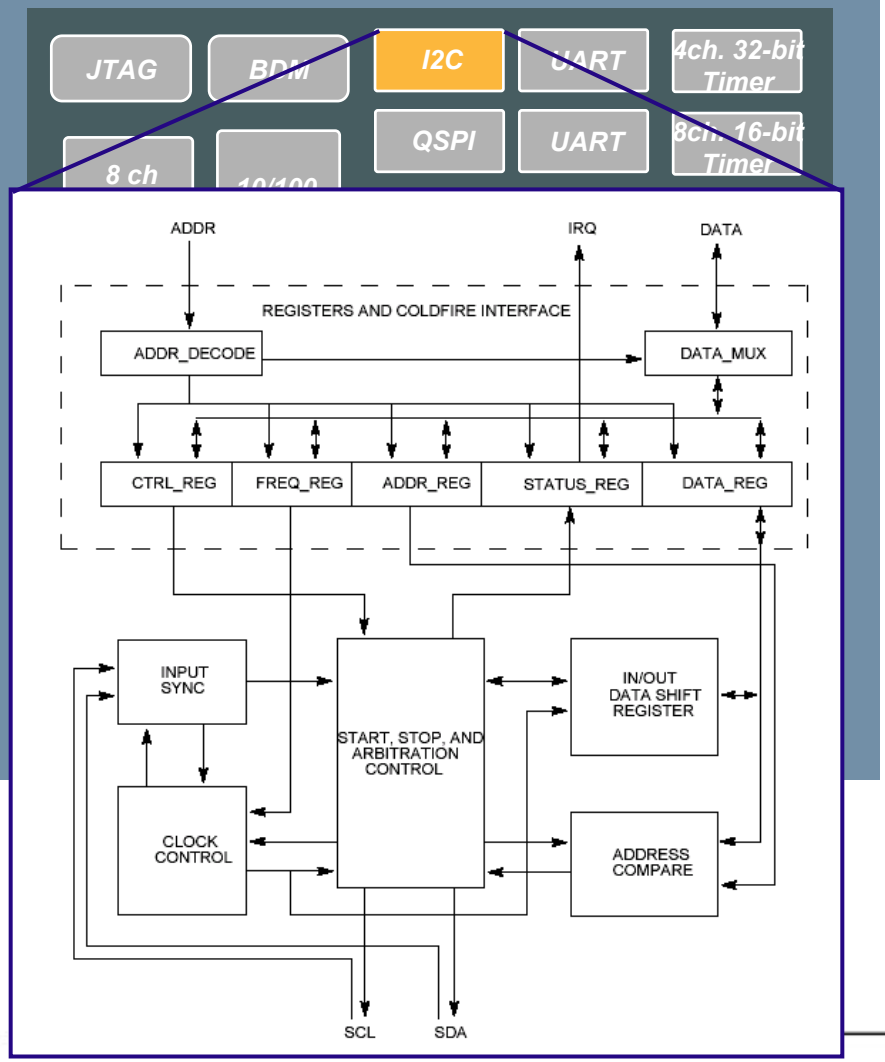
- Serial interface to control external peripherals or transfer data
- Programmable bit rates, clock polarity and phase
- End-of-transmission interrupt flag, master-master mode fault flag
- Programmable queue : Up to 16 pre-programmed transfers
- Wraparound transfer mode with no CPU overhead
- Programmable transfer length, transfer delay, queue pointer
- Four programmable peripheral chip-selects
  - One dedicated chip select output
  - Three chip selects multiplexed with other pin functions
  - general purpose I/O port pins can be used as chip selects

Three UART Modules



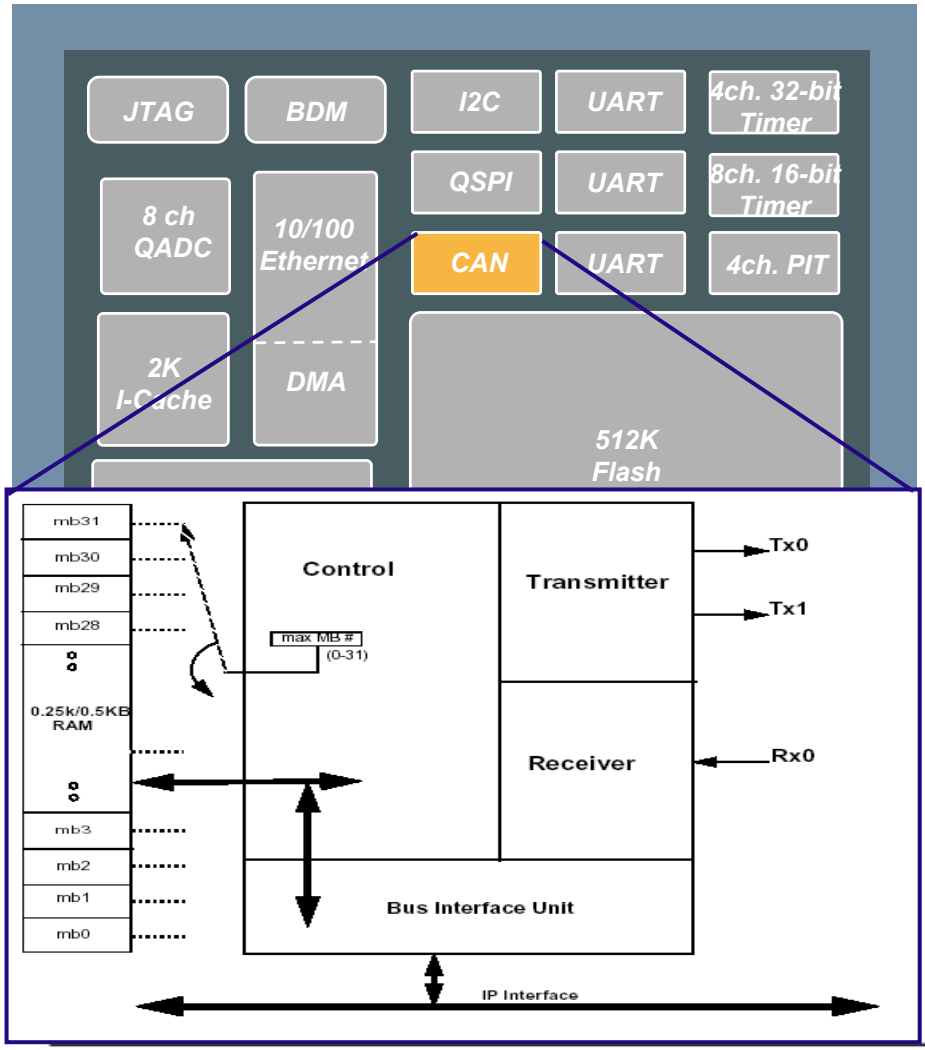
- **Three modules, two with flow control**
- **All can initiate DMA transfers**
- **Receiver Features**
  - 4-stage FIFO receive buffer
  - Frame, parity, and overrun error detections
  - Detection of a break originating in the middle of a character
  - Line-break detection
  - Receiver operation may be polled or interrupt driven
  - Automatic wakeup for multidrop applications
  - Start/end break interrupt status
  - False start bit detection
- **Transmitter Features**
  - Double-buffered operation
  - Programmable character length from 5 to 8 bits
  - Parity generation: odd, even, no parity, or force parity
  - Break generation
  - Stop bit generation from .563 to 2 bits
  - Automatic negation of request-to-send upon completion of message transmission

I²C Module



- Compatibility with I²C bus standard
- Two-wire bi-directional serial bus for on board communication
- Multiple master operation with arbitration and collision detection
- Software programmable for one of 64 different serial clock frequencies
- Interrupt driven, byte-by-byte transfer
- Automatic switching from master to slave on arbitration loss
- Start and stop signal generation and detection
- Repeated START signal generation
- Interchip bus interface for EEPROMs, LCD controllers, A/D converters, keypads

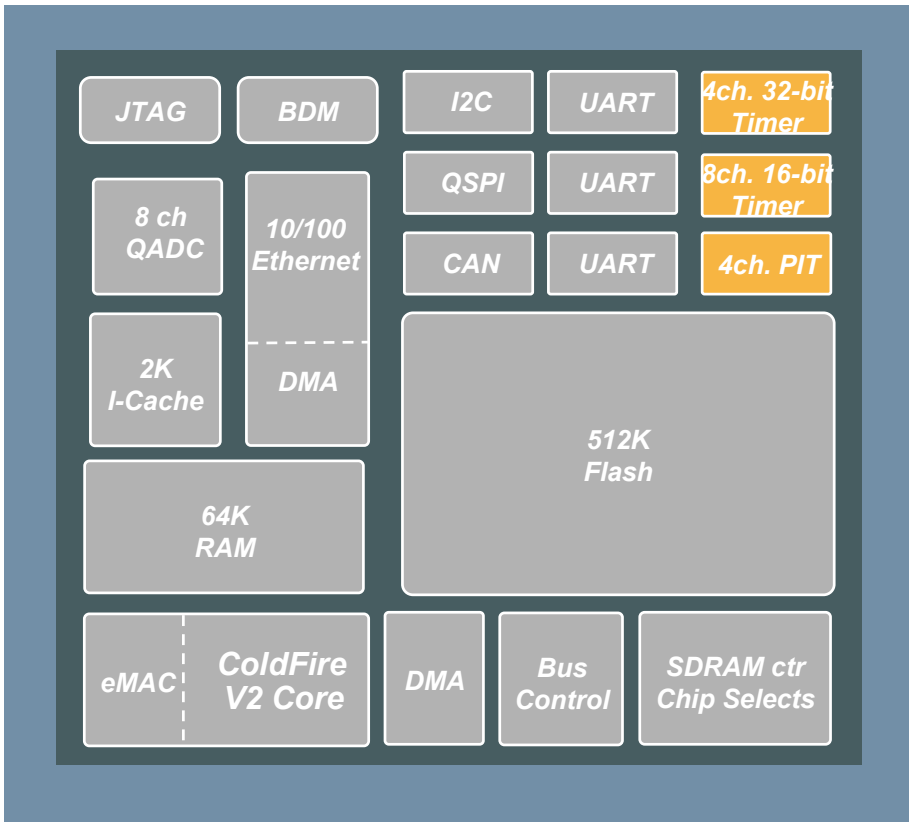
CAN Module



- Full implementation of the CAN protocol specification - Version 2.0B
  - Standard data and remote frames (up to 109 bits long)
  - Extended data and remote frames (up to 127 bits long)
  - 0-8 bytes data length
- 16 message buffers
  - Each configurable as RX or TX
  - All support standard and extended messages
  - Interrupt flag for each message buffer
  - Global mask registers for message buffers 0-13
  - Dedicated mask registers for message buffers 14 & 15
- Programmable Bit Rate up to 1Mbit/sec
- Programmable transmit-first scheme: Lowest ID or lowest buffer number
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Listen only mode (no receive acknowledge) for diagnostic use
- Programmable I/O Modes
- Maskable interrupts
- Open network architecture
- Multimaster architecture
- High immunity to EMI
- Short latency time for high-priority messages
- Low power sleep mode, with programmable wake up on bus activity

MCF5282 Timer Systems

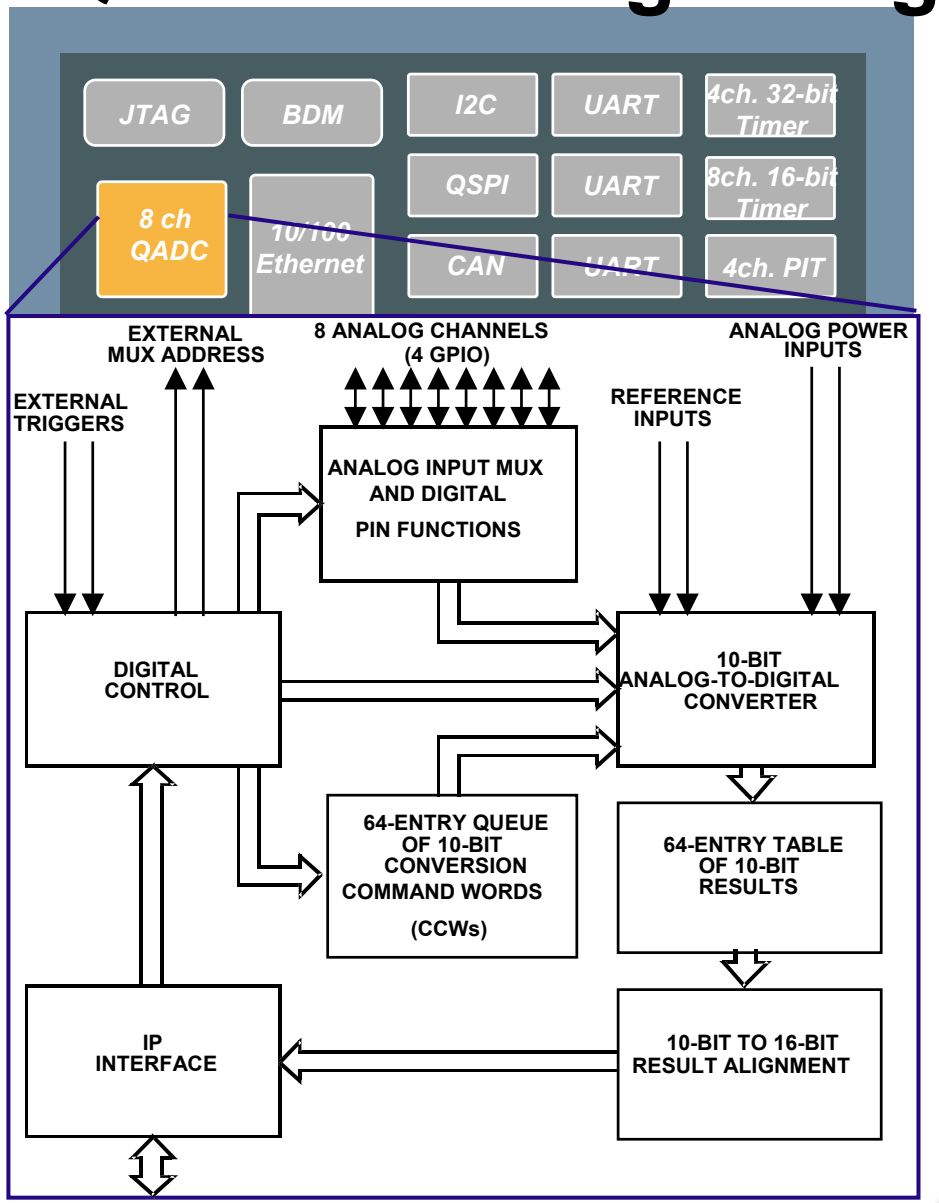
MCF5282 Timer Systems



- Four 32-bit DMA Timers
  - Four independent timers with 32-bit free-running counters
  - 1 Input Capture unit and 1 Output Compare unit per timer
  - Selectable active-low pulse or pin toggle on counter compare
  - Optional free-running counter reset on compare
  - Interrupt or DMA transfer on capture or compare event
- 8 Channels of General Purpose 16-bit Timer
  - Two independent modules with 4 channels each
  - Each channel is programmable as either Input Capture or Output Compare
  - PWM capability using 2 channels
  - Programmable prescaler per module
  - Pulse width is variable from microseconds to seconds
  - External timer clock input option
  - 16-bit pulse accumulator per module
- 4 Channel Periodic Interrupt Timer
  - Provides Interrupts at Regular Intervals
  - Based on a 16-bit Free-running Down Counter
  - Sets a Timeout Flag Upon Underflow
  - Can Selectively Generate an Interrupt or Set Flag
  - Timeout Period is User Specified via a 16-bit Modulus Register
  - Timeout Period = $2^{PRE[3:0]}$ X (PM[15:0] + 1) System Clock Cycles
  - Current Counter State Readable Anytime
  - Can Continue to Operate in Low-power Modes
  - Always Stopped in Stop Mode

Analog to Digital Converter

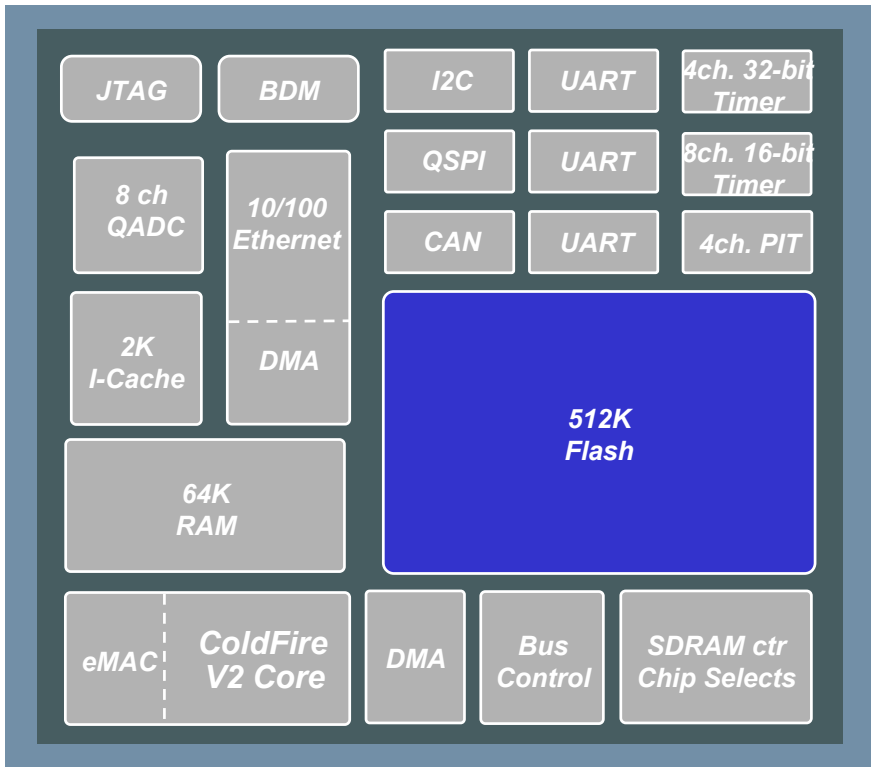
Queued Analog to Digital Converter (QADC)



- 10-bit Successive Approximation A/D
- Up to 8 A/D Channels Without External Multiplexing
- Up to 18 A/D Channels With External Multiplexing
  - Signal Support for Up to Four 1-of-4 External Multiplexers
- Internal Sample and Hold with Programmable Sample Time
- Dual Command Queues (64 Entries) with Sub-queue Support
- Multiple Modes for Queue Initiating and Cycling
  - Timer triggered
  - External pin triggered
  - Software triggered
    - Continuous scan mode
    - Single scan mode
      - Sub queues (Pause bit)
- Interrupt Capability for Queue Complete and Pause
- Selectable Result Formats

Memory System

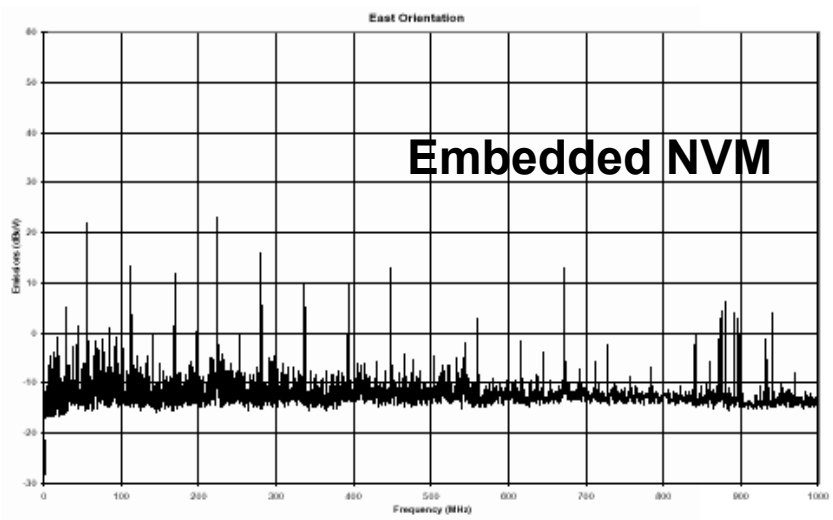
MCF5282 Flash Memory

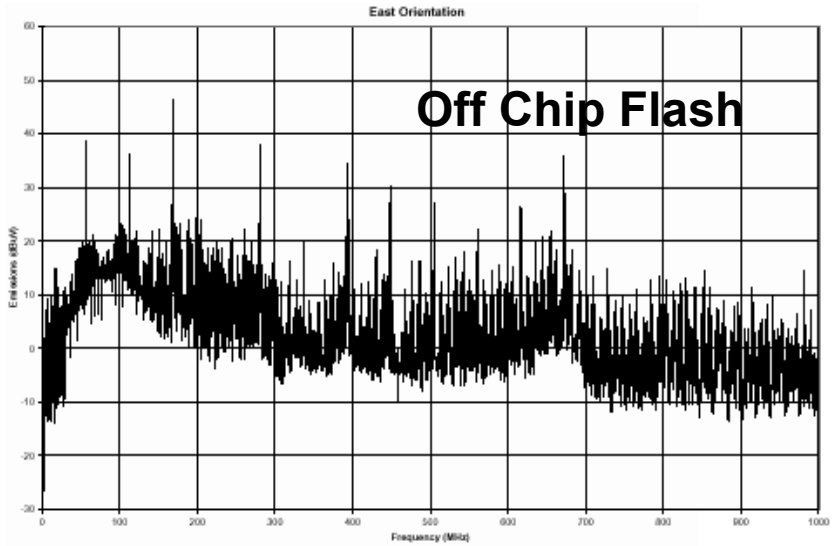


- 512 Kbytes of Flash memory
- 10,000 W/E cycles and 10 years data retention
- Supports 66Mhz Flash array read operations with as few as 1 clock access
  - 2 clocks for first access followed by 1 clock access until change of flow
  - CPU pipelining helps to achieve performance close to that of 1 clock accesses
- Security for data/program protection
- Concurrent program, erase or blank verify of all Flash array blocks (16K byte blocks)
- Automated program and erase operation
- Single power supply (MCF5282 Vdd, 3.3V) used for all module operations
- Read-while-write capability
- Optional interrupt on command completion
- Protection scheme to prevent accidental program or erase
- Access restriction control for supervisor/user and data/program space operations
- Security for single-chip operations
- Auto sense amplifier timeout for low-power, low frequency operation read operations

Embedded Flash Advantages

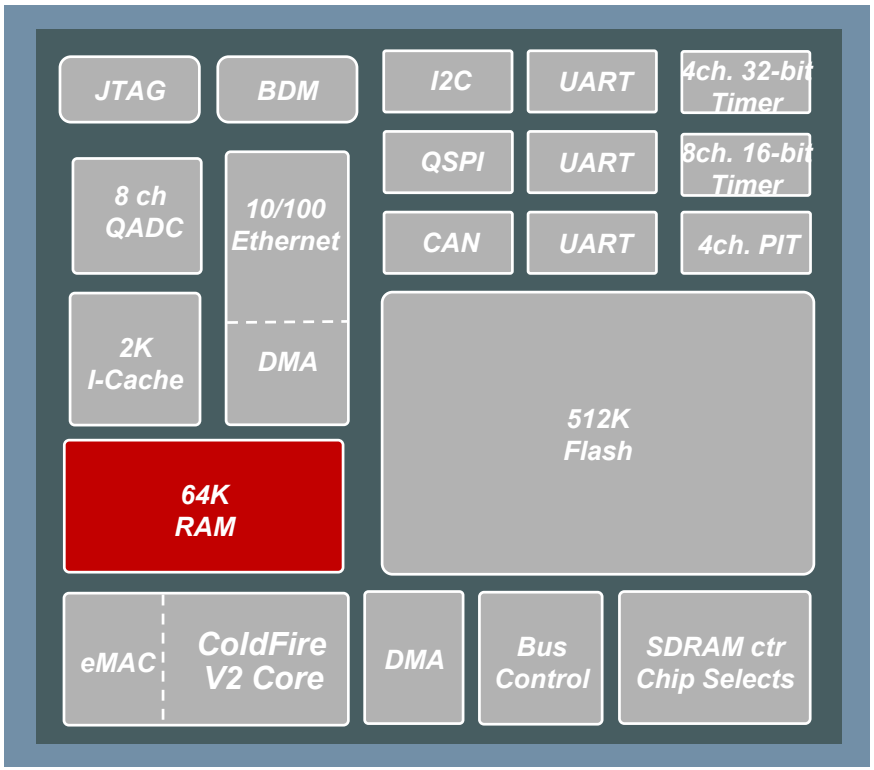
Radiated/Conducted Emissions





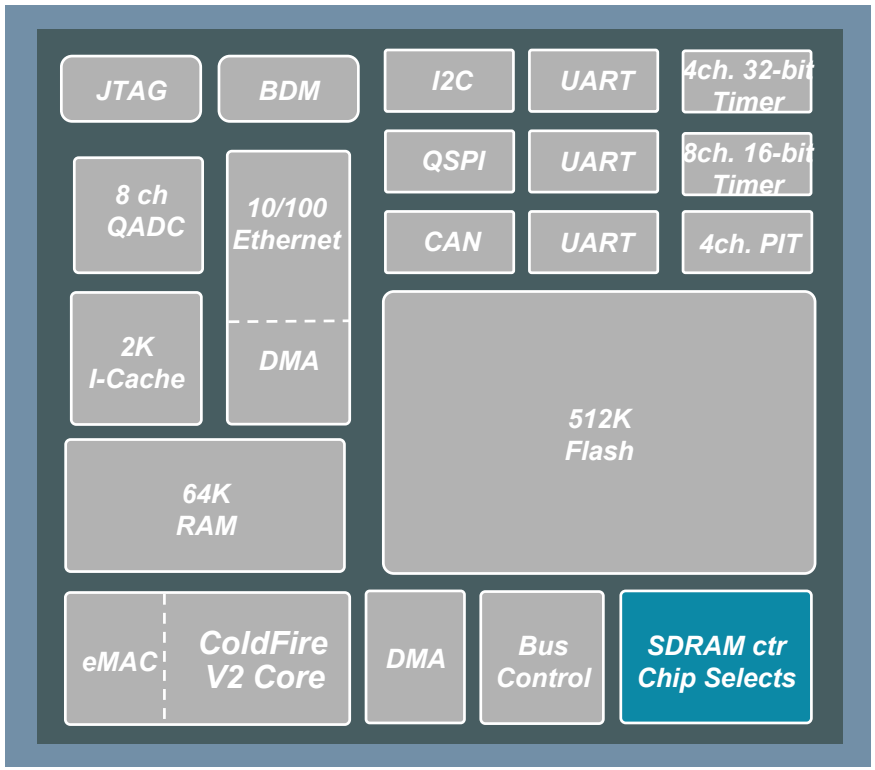
Higher performance due to faster on chip accesses

MCF5282 RAM Module



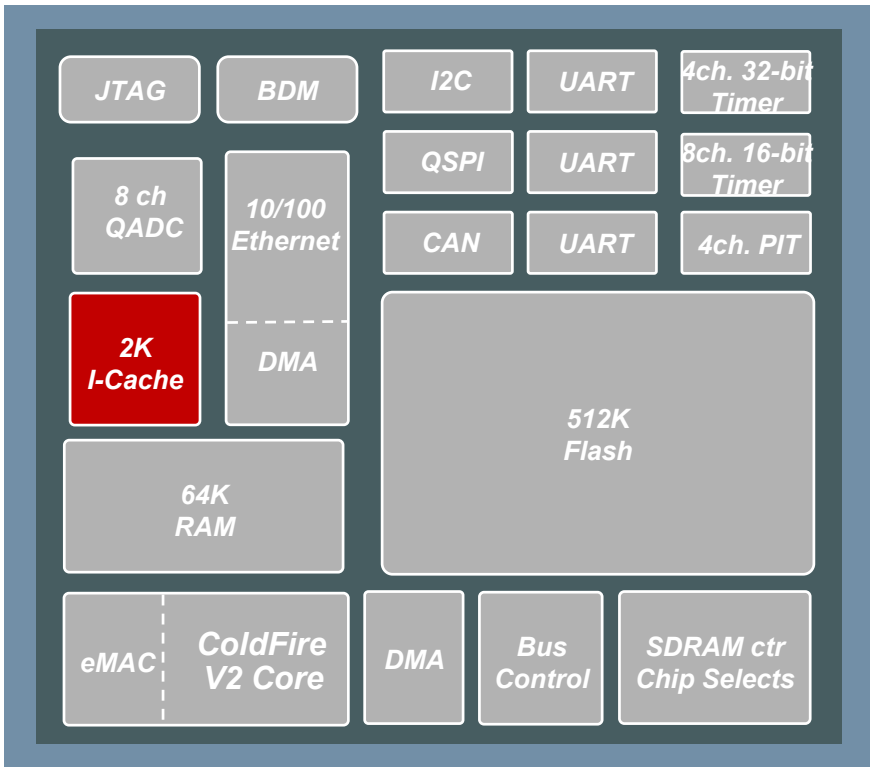
- 64K bytes of RAM memory
- Dual port access supporting K-bus and S-bus
- Standby data retention
- Typical standby current target 20µA
- 1 clock access

(S)DRAM Controller



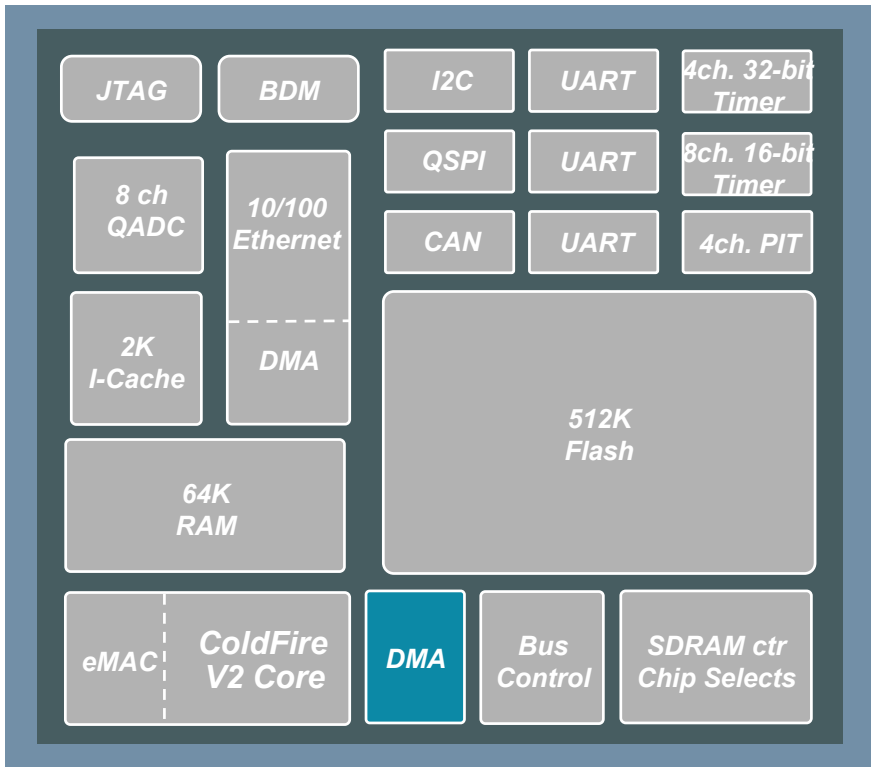
- Supports up to 2 banks of DRAM
- Supports external masters
- Programmable wait states and refresh timer
- Supports 8-, 16-, & 32-bit wide DRAM banks
- Supports Synchronous (S)DRAM

MCF5282 Cache



- Supports off-chip accesses only
- 2 blocks of 1K bytes
  - 1K byte block is Instruction cache (I-Cache) only
  - 1K byte block is selectable for either Instruction cache (I-Cache) or Data cache (D-Cache)

DMA Controller



- Four Fully Independent DMA Channels
- Dual Address Transfer Operation
- 16-Byte Holding Buffer Size
- Data Transfer of 8, 16, 32 or 128-bit block with bursting capability
- Auto-Alignment capable on source or destination transfers
- DMA transfer operation can be initiated by a UART or DMA timers (32-bit)
- Channel arbitration on transfer boundaries
- Two Address Pointers, source and destination
- 16-bit Byte Count Register allowing block transfers up to 64KBytes
- Support data transfers from and to:
  - Memory to memory
  - Peripheral to memory
  - Memory to peripheral
- Independent transfer widths for source and destination
- Source and destination pointer may be programmed to increment after transfer or not
- Maximum sustained data transfer rate of ???

System Integration

Interrupt Features

- 7 Levels of Interrupt with 9 Priorities at each level
  - **Levels 1-6 Maskable**
  - **Level 7 Non-Maskable**
    - **Each level has 8 programmable priorities**
    - **Each level has 1 fixed priority associated with an IRQ input pin**
- Interrupt sources are mapped to available interrupt priorities within levels as required and available
- 3-Bit Mask in CCR Determines Lowest Interrupt Priority Level that will be recognized.
  - **Interrupt mask set by interrupts or by instructions**
- 128 Unique User Defined Interrupting Sources Allowed
- 7 Auto-Vectors - one per interrupt level

Reset Controller Module (RCM)

- Determines the cause of reset
- Asserts the appropriate reset signals to the system
- Keeps a history of the cause of the reset
- Seven Sources of Reset
    - External (reset pin)
    - Power on Reset (POR)
    - Watchdog Timer
    - PLL loss of clock
    - PLL loss of lock
    - Software
    - Low Voltage Detect (LVD)

Chip Configuration Module (CCM)

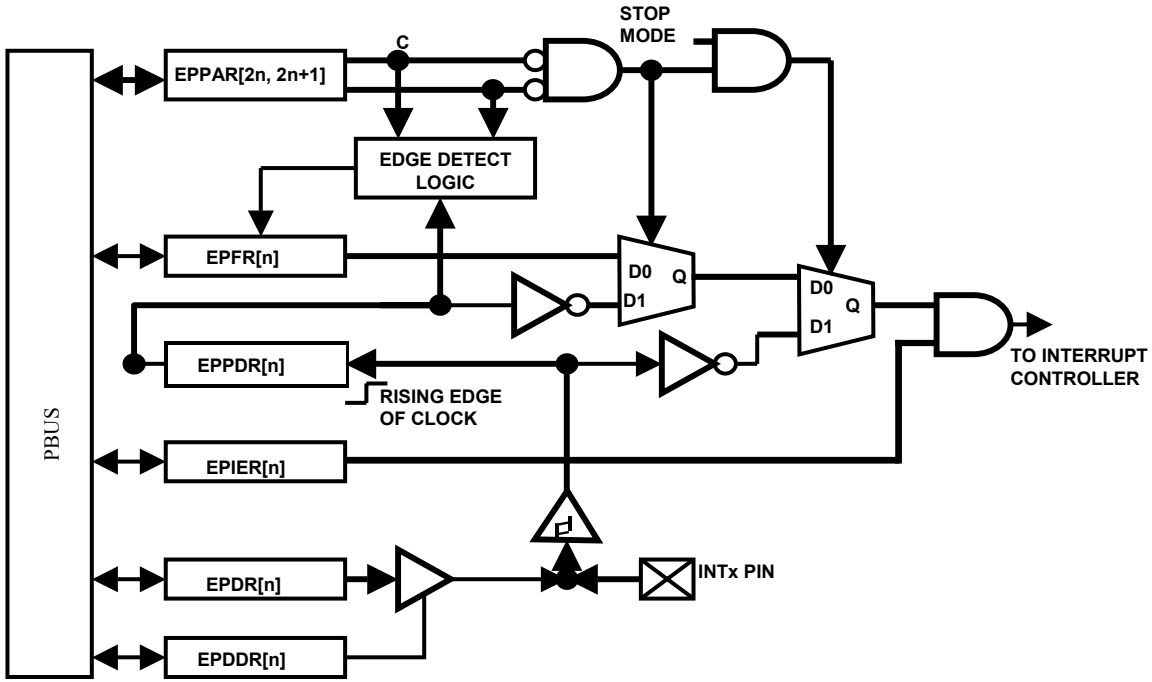
- Selects Operating Mode
  - Master Mode
  - Single Chip Mode
  - Factory Test
- Selects Clock Operation
  - Normal PLL with crystal reference
  - Normal PLL with external clock reference
  - 1 to 1 PLL mode
  - External clock mode
- Selects Boot Device and Data width
  - 8, 16, 32 bit wide data bus for external accesses
- Selects Output Pad Drive Strength
- Selects Chip Select Configuration
  - Chip selects 6-4 can be individually configures as upper address lines

Power Management Module (PMM)

- Controls the low power operation
- Four modes of operation: Run, Wait, Doze, Stop
  - Stop mode wake interrupt level is programmable
- Most peripherals can be shutdown Independently
- External clock output pin has disable option

EPORT

- Allows Up to Seven Sources of External Interrupts
- Sensitivity Can be Low-level or either/Both Edge Detection
- Each Pin Can be Used as Interrupt or General-purpose I/O
- Schmitt Triggered Inputs Reduce Chance of False Interrupts
- Operational in All Three Low-power Modes.



MCF5282 System Protection

- **Software watchdog**
- **Low voltage detection (brownout protection)**
- **Bus monitor**
- **PLL loss of clock**
- **PLL loss of lock**
- **Flash security**
- **Flash protection (by block, 16K bytes)**
  - Program and Erase
  - Data or Instruction/Data access
  - Supervisor only or Unrestricted

MCF5282 System Clock Generation

- Generates clocks for processors, slave modules, and communication modules
- PLL is used to generate system clock from reference oscillator
- Crystal frequency 2 to 10 MHz
- PLL lock time maximum 500µseconds
- External clock mode

MCF5282 Power Supply Considerations

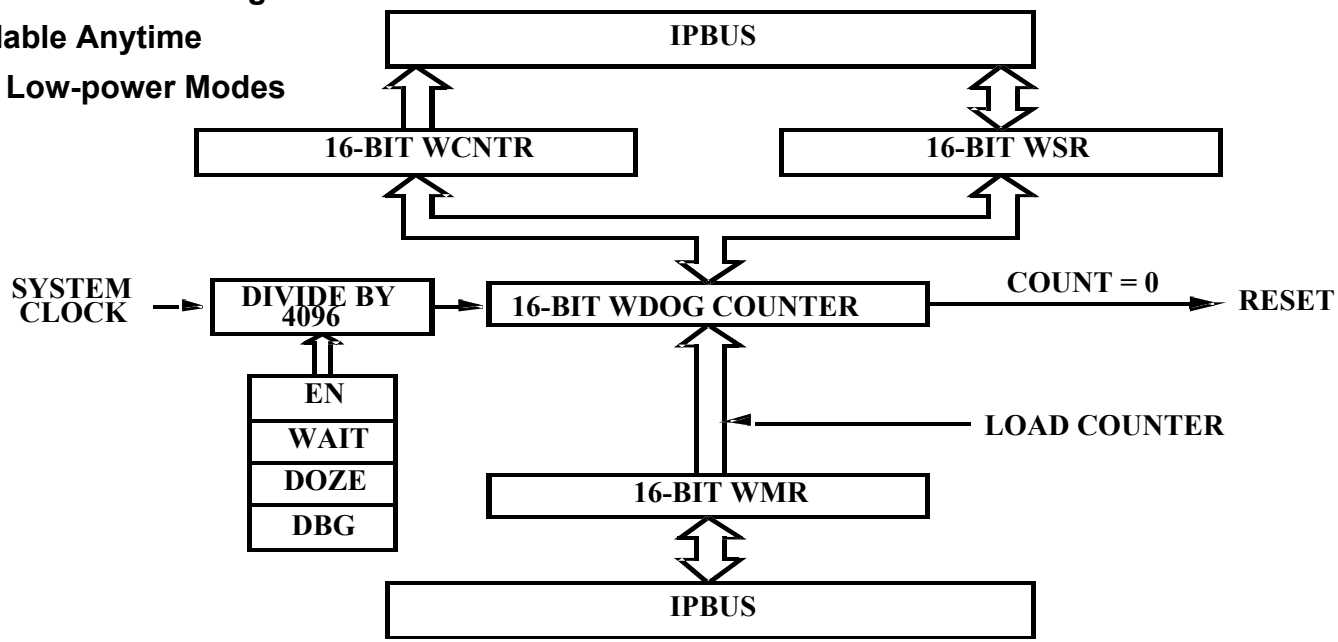
- **Supply voltage = 3.3V +/- 10%**
- **Power Consumption**
  - **Run master mode = 175mA (max)**
  - **Run single chip = 150mA (max)**
  - **Stop mode = 100µA (max**
  - **RAM standby = 20µA**
- **I/O pins are 5V tolerant**

Low Voltage Detect Features

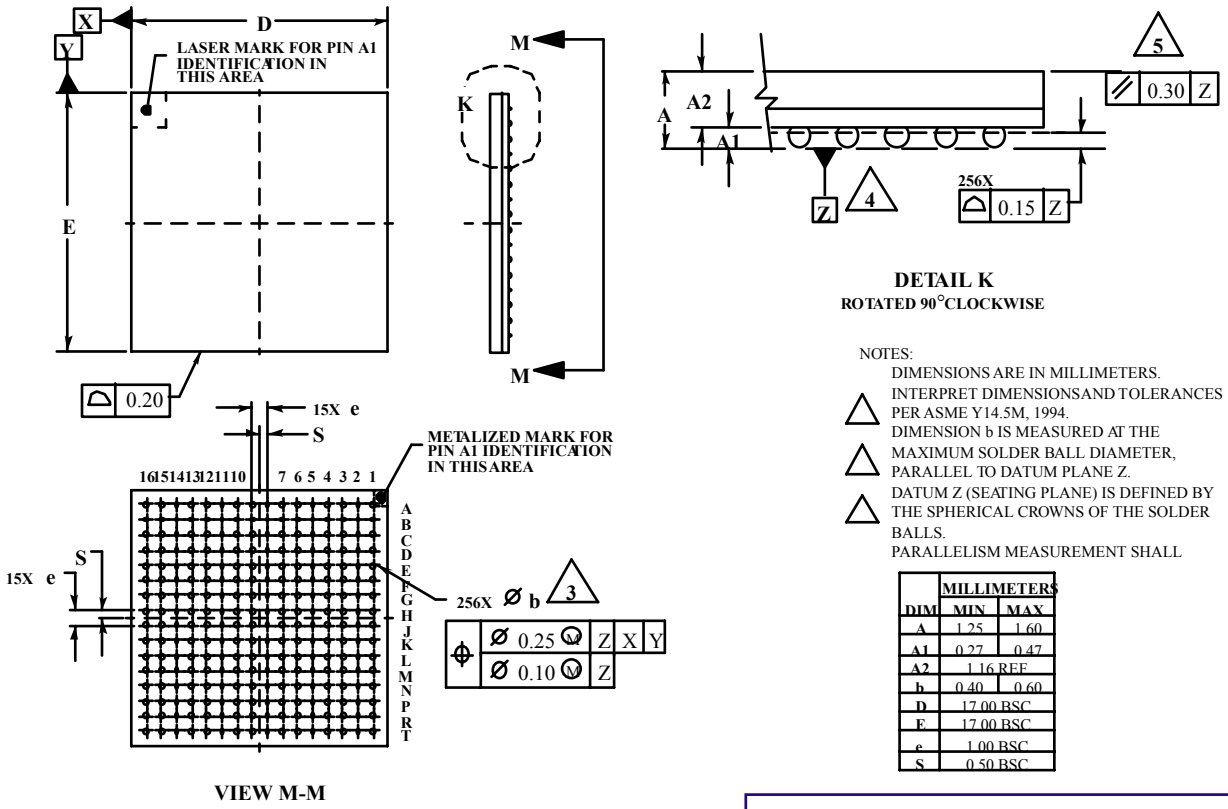
- LVD Enabled/Disabled in Software
- Selectable Reset or Interrupt Action upon Low-voltage Detection
- Selectable Enable/Disable in Stop Mode
- Reset Caused by LVD Indicated in Reset Status Register after Reset
- LVD Interrupt Maskable and Configurable
- LVD Interrupt Vector Shared with EPORT's INT0

Watchdog Timer

- **The watchdog timer is a 16-bit timer used to help software recover from runaway code. The watchdog timer has a free-running down-counter (watchdog counter) that generate a reset on underflow. To prevent a reset, software must periodically restart the countdown by servicing the watchdog.**
- **Used to Recover from Runaway Code**
- **Automatically Generates a Reset if Not Serviced**
- **Based on a 16-bit Free-running Down Counter**
- **Timeout Period is User Specified via a 16-bit Modulus Register**
- **Serviced by Writing Twice to the Service Register**
- **Current Counter State Readable Anytime**
- **Can Continue to Operate in Low-power Modes**



MCF5282 Package



VIEW M-M

DETAIL K
ROTATED 90°CLOCKWISE

NOTES:
DIMENSIONS ARE IN MILLIMETERS.
INTERPRET DIMENSIONSAND TOLERANCES PER ASME Y14.5M, 1994.
DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
PARALLELISM MEASUREMENT SHALL

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

CASE 1216B-01
ISSUE O

17 mm x 17 mm x 1.6 mm 256-ball (1 mm pitch) mold array process ball grid array (MAPBGA) package

MCF5282 Pinout

Legend

- = 45 west signals
- = 48 south signals
- = 45 east signals
- = 43 north signals
- = VDD balls
- = VSS balls
- = no-connect balls

181 signals, 21 VSS, 20 VDD

222 total pads

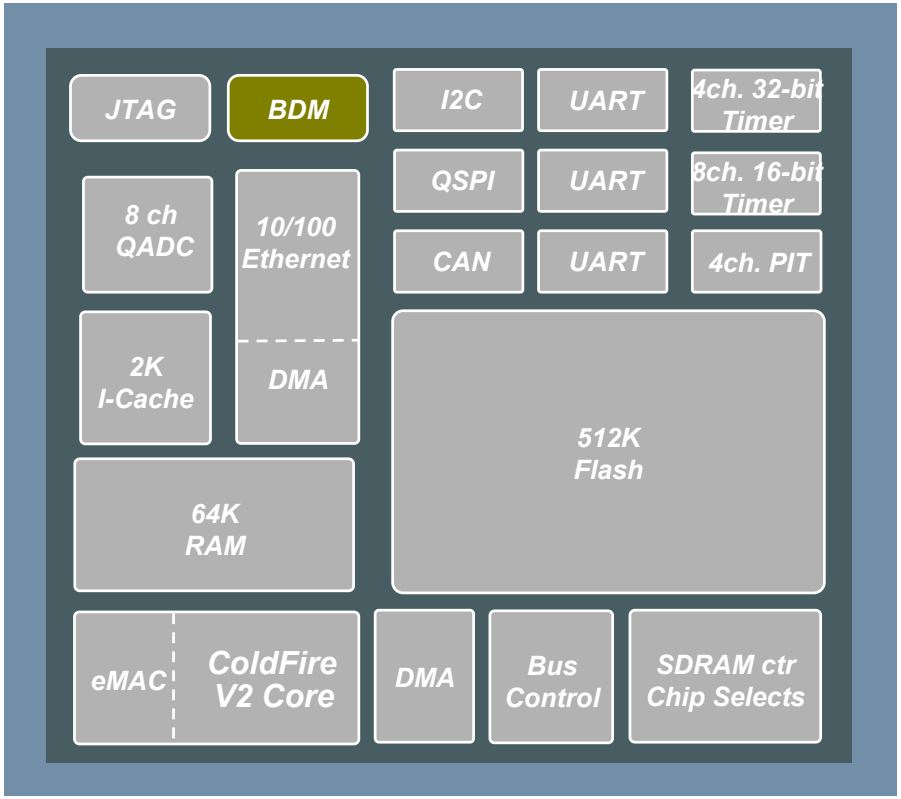
17x17mm 256 1mm pitch MAPBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	A15	A16	A18	A21	VPP	ETXD[3]	ETXCLK	ERXD[3]	ERXCLK	ECRS	VDDF	DDATA1	PST2	PST0	VSS
B	A14	A13	A17	A19	VSSF	A22	ETXD[2]	ERXER	ERXD[2]	EMDC	ECOL	VSSF	DDATA0	PST1	IRQ[7]_B	IRQ[6]_B
C	A12	A11	A10	A20	VDDF	A23	ETXD[1]	ERXDV	ERXD[1]	EMDIO	VPP	DDATA3	PST3	IRQ[5]_B	IRQ[4]_B	IRQ[3]_B
D	A9	A8	A7	A6	VDDF	ETXEN	ETXD[0]		ERXD[0]	ETXER	VDDF	DDATA2		IRQ[2]_B	IRQ[1]_B	CANRX
E	A5	A4	A3	A2	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VSS	CANTX	SDA	SCL	QSDI
F	A1	A0	D31		VDD	VSS	VDD	VDD	VDD	VDD	VSS	VDD	QSDO	SCKE	PCS[0]	PCS[1]
G	D30	D29	D28	D27	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	PCS[2]	PCS[3]	SDWE_B	RAS[0]_B
H	D26	D25	D24	D23	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	RAS[1]_B	SCKE	SRAS_B	SCAS_B
J	D22	D21	D20	D19	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	T0OUT	T0IN	T1OUT	T1IN
K	D18	D17	D16		VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	T2OUT	T2IN	T3OUT	T3IN
L	D15	D14	D13	D12	VDD	VSS	VDD	VDD	VDD	VDD	VSS	VDD	CS[0]_B	CS[1]_B	CS[2]_B	CS[3]_B
M	D11	D10	D9	D8	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VSS		TIP_B	TS_B	TSIZ[0]_B
N	D7	D6	D5		D3	U0RXD	CLKOUT	VDDPLL		TEST	VSTBY	ICOCB[0]	ICOCA[0]	TSIZ[1]_B	R/W_B	OW_B
P	D4	VDDH	PQA3	VRH	VSSA	D0	U1TXD	VSSPLL	TRST_B	TMS	RSTOUT_B	ICOCB[1]	ICOCA[1]	BS[3]_B	TEA_B	TA_B
R	PQB3	PQB1	PQA4	PQA0	VDDA	D1	U1RXD	XTAL	JTAG_EN	TDI	RESET_B	ICOCB[2]	ICOCA[2]	CLKMOD[0]	BS[1]_B	BS[0]_B
T	VSS	PQB2	PQB0	PQA1	VRL	D2	U0TXD	EXTAL	TCLK	TDO	RCON_B	ICOCB[3]	ICOCA[3]	CLKMOD[1]	BS[2]_B	VSS

Debug & Test

ColdFire Background Debug Mode

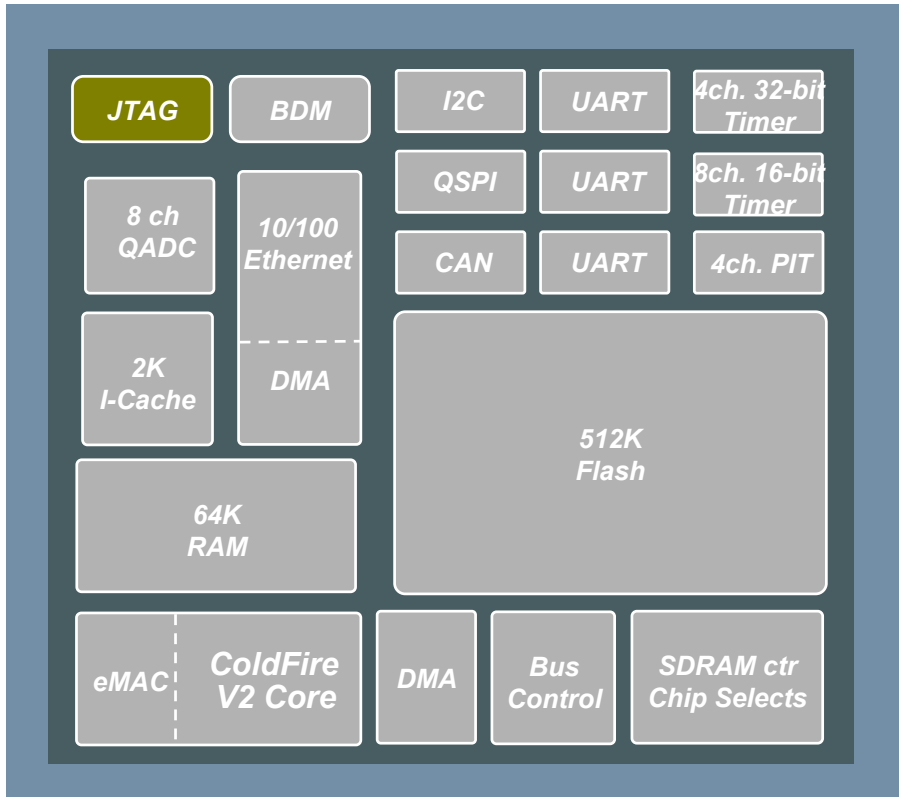
- Real-time trace support
- Background Debug Mode
- Real-time Debug support
- Direct/High speed connection to processor
- Tool vendor support
  - Metrowerks
  - WindRiver
  - Green Hills



Test Access Port (JTAG)

JTAG pins:

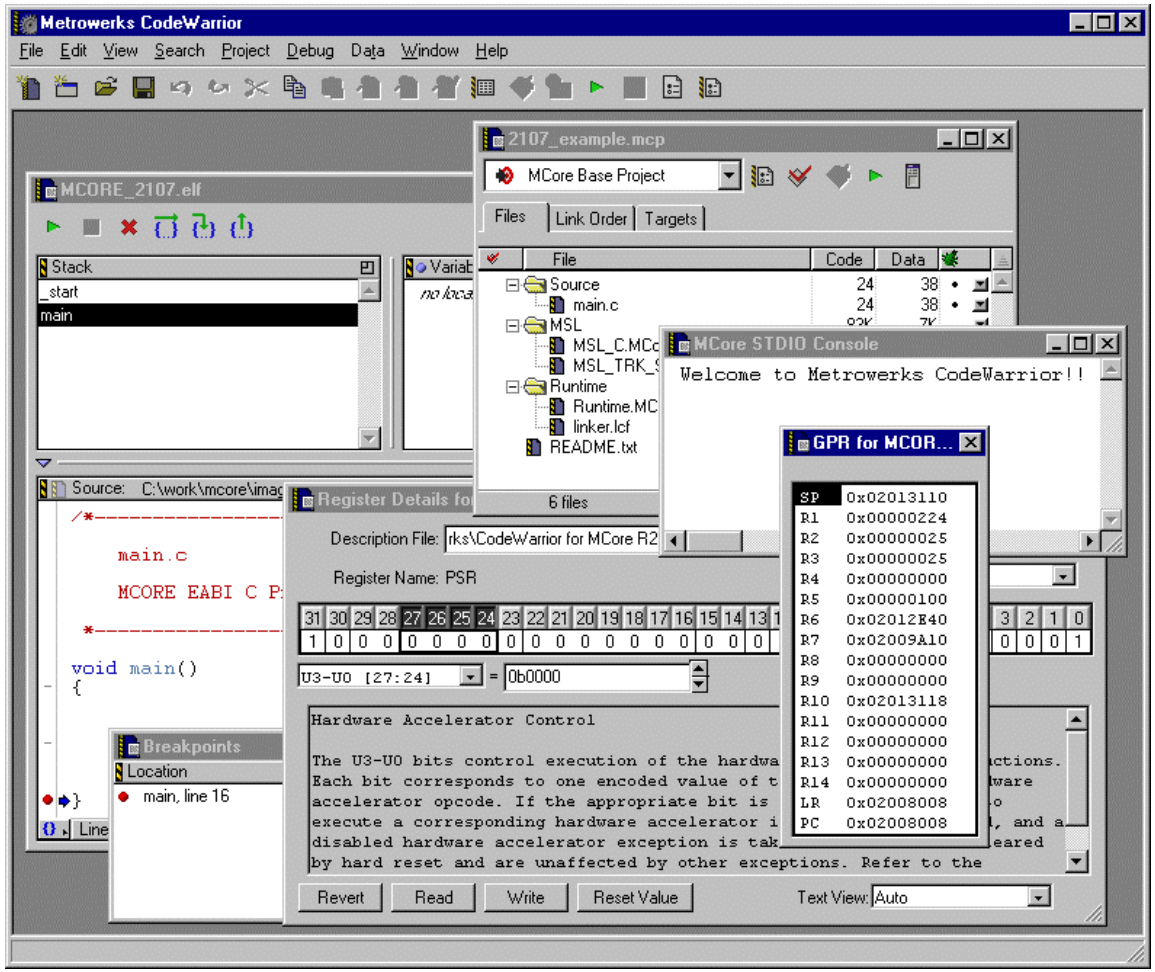
- **TDI: test data input**
- **TDO: test data output**
- **TCK: test clock**
- **TMS: test mode select**
- **TRST: test reset**



Tools

Introducing CodeWarrior
The Industry Leading IDE

- ✓ **CodeWarrior IDE streamlines system design**
- ✓ **Optimized C/C++ compiler ensures smallest code size and fastest execution time**
- ✓ **Industrial-strength project manager eliminates complicated build scripts**
- ✓ **Graphical source level debugging solves complex problems quickly and easily**
- ✓ **Persistent debugger views shorten build-debug cycle**



MOTOROLA intelligence everywhere
digital dna

CodeWarrior IDE Tools Overview

Project Manager - Manipulate items associated with a project

- Handles top-level file management for the software developer
- Organizes project items by major group, such as files and targets
- Tracks state information (such as file-modification dates)
- Determines build order and inclusion of specific files in each build
- Coordinates with plug-ins to provide version-control services

Editor - Create and modify source code

- Uses color to differentiate programming-language keywords
- Allows definition of custom keywords for additional color schemes
- Automatically verifies parenthesis, brace, and bracket balance
- Allows use of list pop-ups for navigation to any function or into the header files used by the program

Search Engine - Locate and replace text

Source Browser - Manage and view program symbols

Build System - Convert source code into an executable file

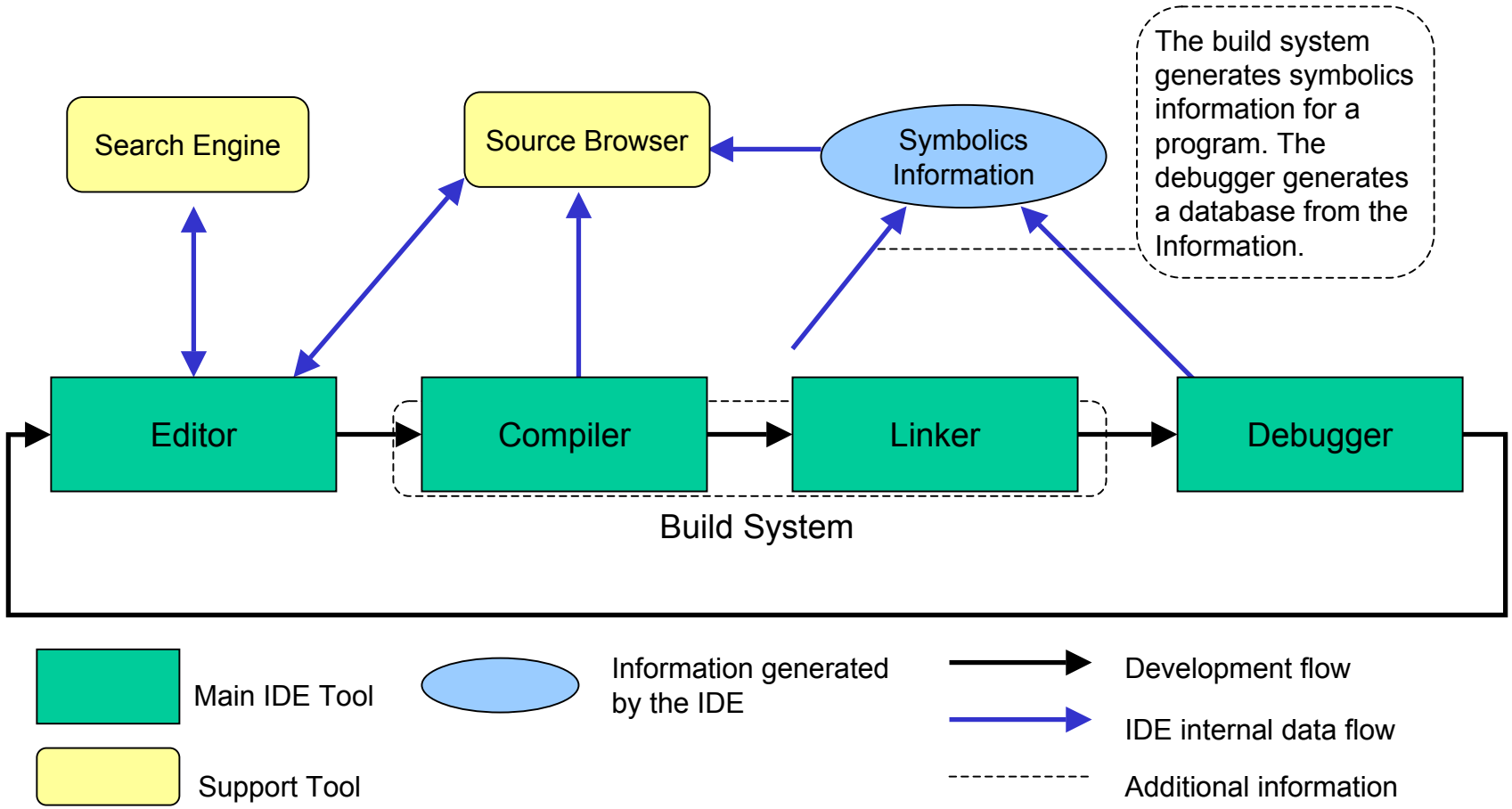
- Uses the compiler to generate object code from source code
- Uses the linker to generate a final executable file from object code

Debugger - Resolve errors

- Uses the symbolics database to provide source-level debugging
- Supports symbol formats such as CodeView, DWARF (Debug With Arbitrary Records Format), and SYM (SYMbolic information format)

RAD tools Support

CodeWarrior Project Manager



CodeWarrior Development System Embedded Network Edition - *ColdFire* Edition

CodeWarrior Development System for Embedded Networks Evaluation Edition for ColdFire MCF5272

Part Number: CWDS5272RTE SRP $660.00

-Evaluation copy of CodeWarrior development tools for ColdFire Embedded Systems v3.0

-Evaluation copy of RTXC™ Quadros™

-M5272C3 Evaluation Board.

CodeWarrior Development System for Embedded Networks Edition for ColdFire MCF5272

Part Number: CWDS5272RTX SRP $42,500.00

-CodeWarrior development tools for ColdFire Embedded Systems v3.0

-Fully licensed RTXC™ Quadros™ with SDK, source code, protocol stacks and sample apps

-Source Code for Ethernet Driver, RTXCtcpip, RTXC DM, RTXChttp.

-Ethernet Driver, UART Driver & Serial Driver included!

-M5272C3 Evaluation Board.

metrowerks
Software Starts Here

Edition for ColdFire MCF5282 will be available in 1Q2003

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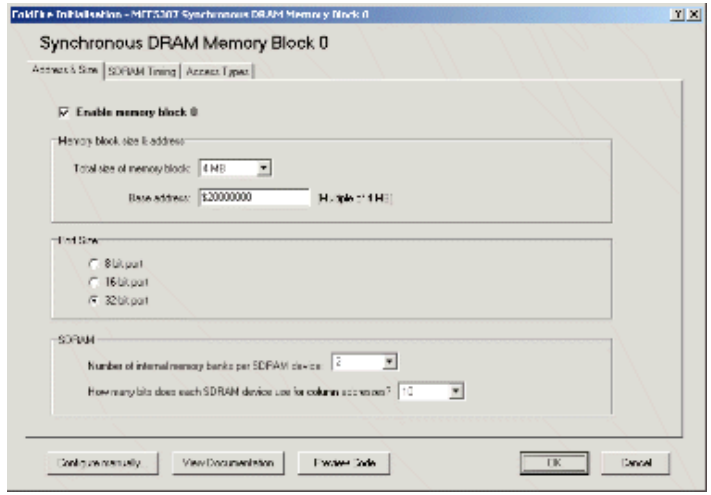
ColdFire_Init
Graphical Configuration Tool



- **Supports device initialization through a graphical user interface**
- **Usable with most software tool sets**
- **Supplied by MicroAPL**
- **Will be available with silicon in 1Q2003**
  - **A series of dialogs allow you to specify exactly how you want the processor to be configured.**
  - **Configurations can be saved to disk for later re-use.**
  - **CFInit checks to determine whether the configuration you have specified includes problems which would show up when you try to run the code. (For example you might**
  - **have mistakenly included the memory-mapped peripherals in the range of addresses which are cached).**
  - **At any stage you can view the code which will be generated for a particular module, or generate the final code for the whole processor.**
  - **Generated code is in ColdFire assembly language and includes detailed comments.**
  - **Supports most major ColdFire toolsets, including Diab Data, Microtec/Mentor Graphics, CodeWarrior, Green Hills and Gnu assemblers.**
  - **Closely tied to Motorola's own documentation on each ColdFire processor. With one mouse click you can view the documentation for an individual ColdFire module or register. (Requires Adobe Acrobat Reader)**
  - **CFInit also includes informative popup help which explains your options in detail and tells you exactly how the processor's registers will be initialized.**
  - **Supports manual configuration of individual registers at the bit level for the rare cases where the standard configuration options are insufficient.**
  - **Runs under Windows 95/98/Me/NT/2000/XP**
  - **Includes comprehensive support for ColdFire modules**

M5282EVB - Evaluation Board

- **Memory**
  - 8M byte SDRAM, 2M byte external Flash EPROM
- **Development Ports**
  - BDM Debug Development connector
- **General**
  - 10/100 Ethernet PHY and RJ45 connector
  - CAN transceiver (SN65HCD230D) and DB-9 connector
  - 2 serial ports DB-9 connectors
  - All internal module signals connectors available on 2x20 headers
  - Expansion connectors for Daughter board connection, provides access to all MCF5282 signals
  - Chip configuration capability
  - Multiple clocking options
  - Debug monitor
  - Power_Port with Power supply access
  - 6 to 14VDC Input
  - Typical Operating Power: 400mA @ 66MHz (expected)
- **Part number & Price**
  - M5282EVB
  - Recommended Resale $850

ColdFire Development Tools Vendors

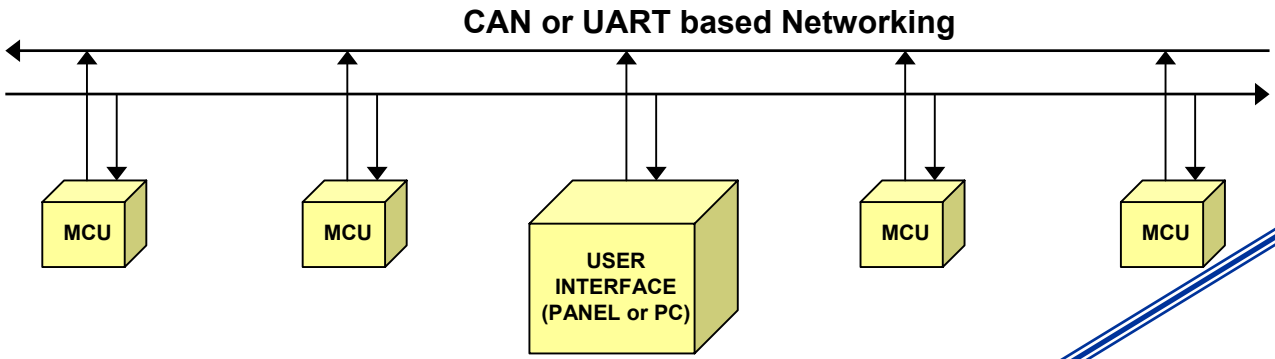
ColdFire Device	Metrowerks	WindRiver						Green Hills						SnapGear (Lineo)		ATI	Netburner	Mentor				Gnu			Noral		Crossware			MicroAPL		P&E MICRO	Precise
	IDE - Codewarrior	H/W Debugger - VisionProbe	S/W Debugger - Singlestep	S/W Debugger - VisionClick/VisionXD	Wiggler - VisionProbe II	RTOS - VxWorks	Compiler - Diab, C/C++	IDE - Multi	Compiler - C/C++/EC++	MULTI Source Level Debugger	RTOS - ThreadX	Host Support (Sun/HP/Windows)	Embedded IP (i.e. TCP/IP Stack)	OS - µCLinux*	Embedded IP (i.e. TCP/IP Stack)	RTOS - Nucleus +	Network Development Kit	Simulator	Compiler - C/C++	Debugger - X-Ray	RTOS - VRTX	Gnu Debugger	Compiler - C*	RTOS - uCLinux	FLEX - BDM	Emulator - Flex	Compiler - C	Simulator	Debugger	Emulation Library*	Code Translator - PortASM 68K/CF*	P&E ColdFire Wiggler Cable	RTOS
MCF5206e	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻		✻	✻	✻
MCF5249	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻						✻	✻	✻			✻	✻	✻	✻	✻	✻	
MCF5272	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻					✻	✻	✻			✻	✻	✻	✻	✻	✻	
MCF5307	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻			✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻
MCF5407	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻	✻						✻	✻	✻			✻	✻	✻	✻	✻	✻	✻

✻	Available
✻	Projected to be available

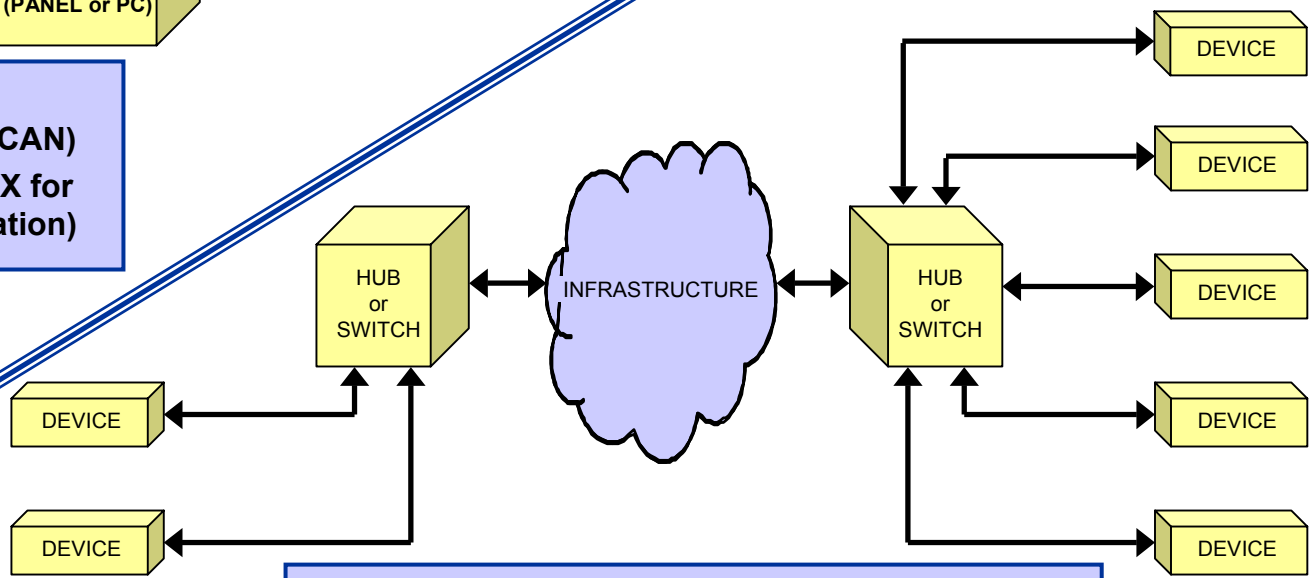
ColdFire MCF5282 information will become available with samples in 2003

Application Examples

Traditional Networking

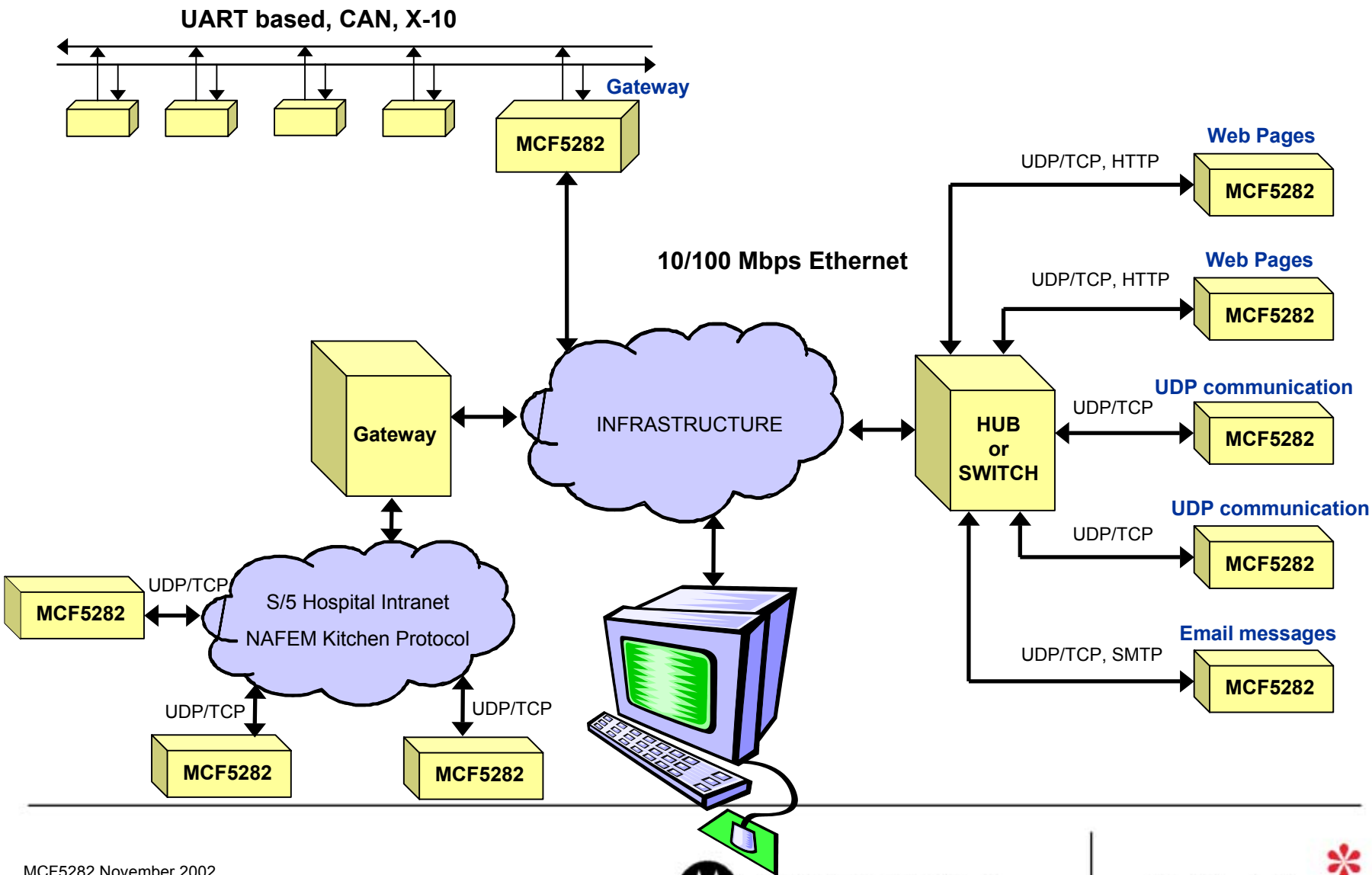


- Inexpensive Cabling
- Standard MCU modules (SCI, CAN)
- Some standard protocols (DMX for lighting, DeviceNet for automation)



- Standard protocols
- Slow and fast devices on same network
- Access to World Wide Web
- Ability to handle proprietary protocol layers

Evolution of Networking with MCF5282



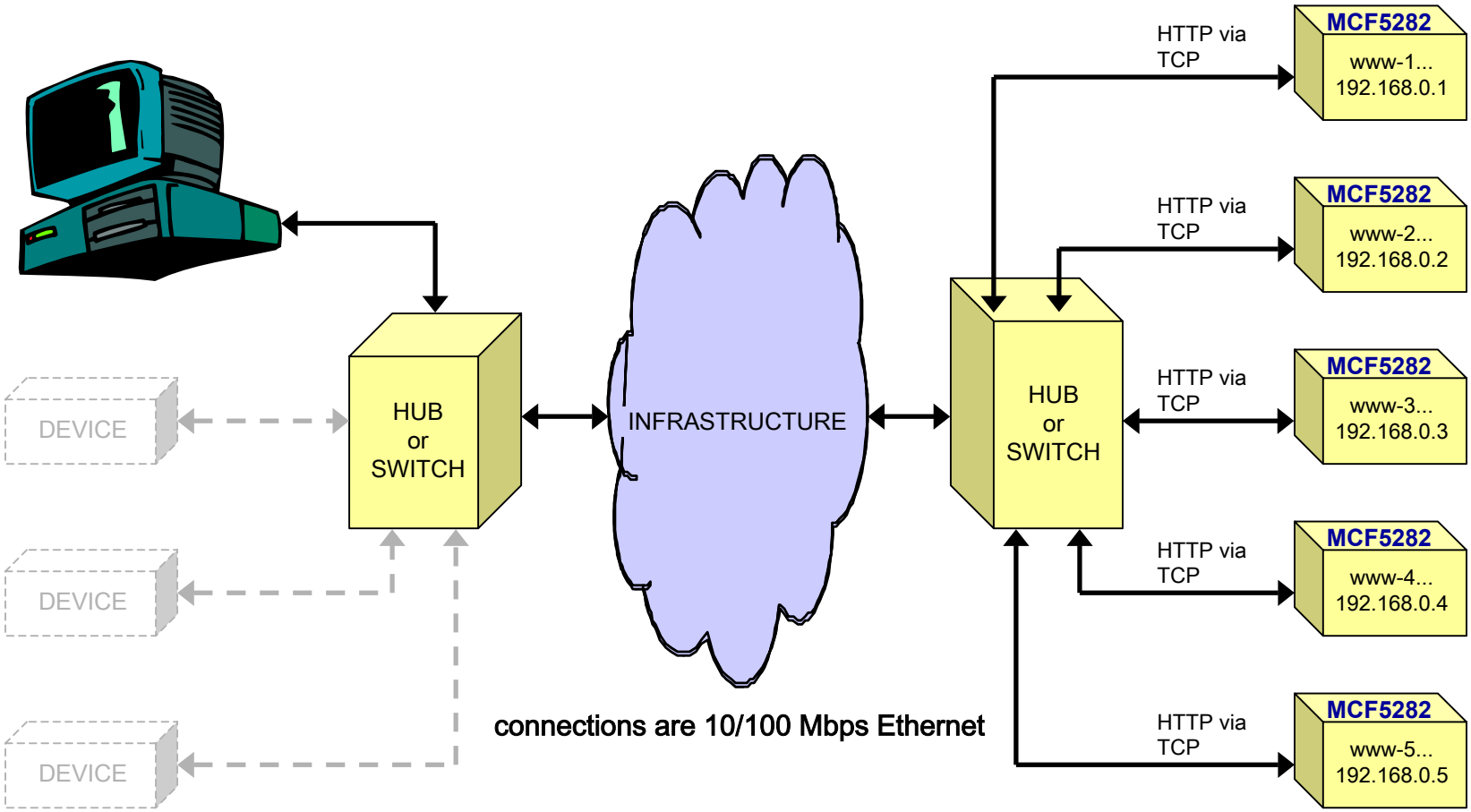
Ethernet Protocol Primer

- ARP - Address Resolution Protocol is used to find what network interface (Ethernet MAC) owns a given IP address
- DHCP - Dynamic Host Configuration Protocol is used to automatically allocate IP addresses on an as-needed basis
- IP - Internet Protocol is the basic delivery mechanism for packets of data sent between all systems on the Internet
- ICMP - Internet Control Message Protocol is used to convey diagnostic and management messages
- TCP - Transmission Control Protocol provides disassembly, sequencing, error checking, and assembly services for packets moved by IP. TCP makes IP reliable
- UDP - User Datagram Protocol is a simple protocol with no error checking or sequencing that uses IP to move packets between endpoints on the Internet. UDP is faster than TCP

Why is Ethernet / IP Required?

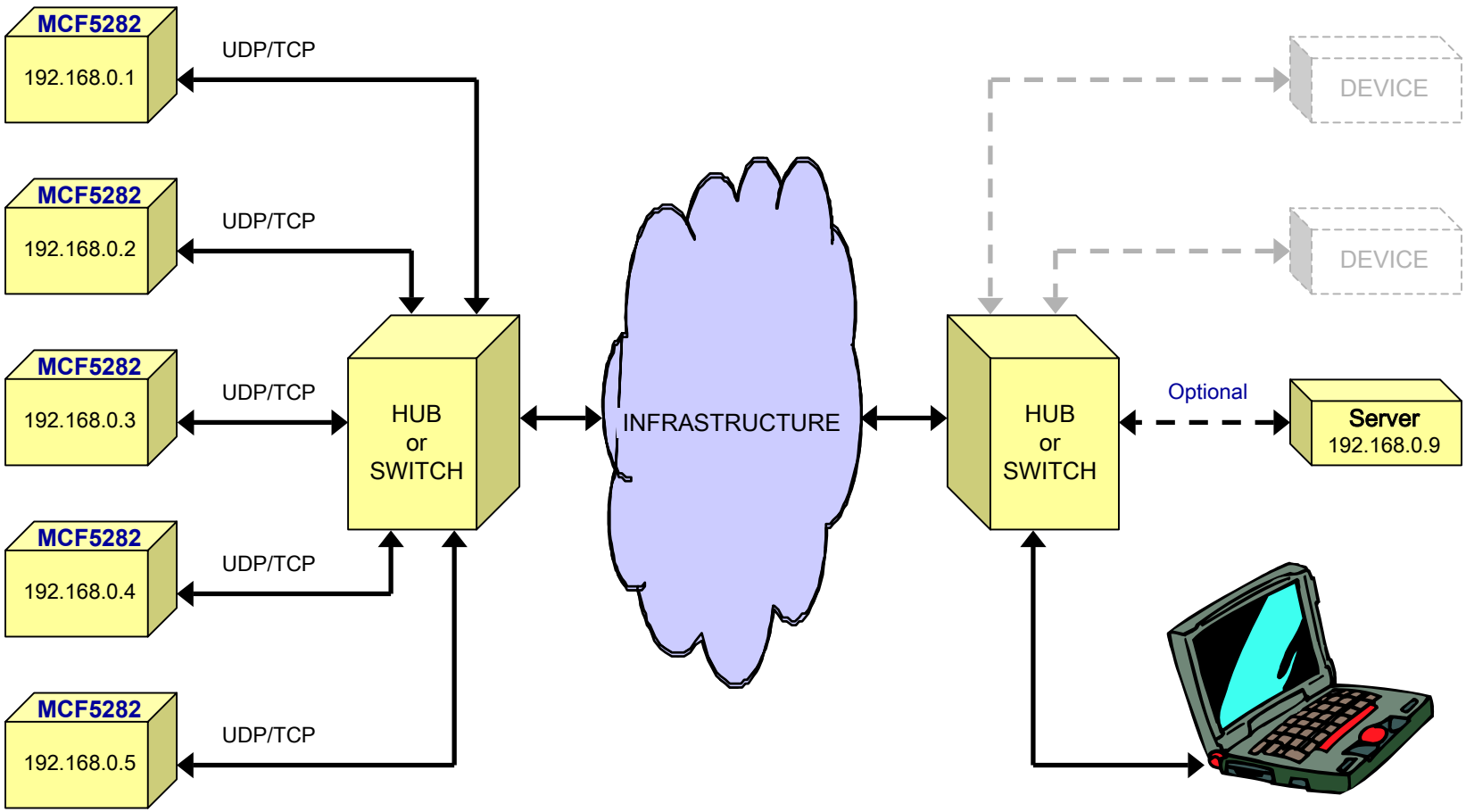
- Common language
- Modern infrastructure supports automatic negotiation between slow (10 Mbps) and fast (100 Mbps) devices
- Can have slow and fast devices on same network when a switch is used
- Distances up to 100 meters between devices using commodity CAT5 cable
- Unlimited distances over the World Wide Web
  - ✓ **Size and extent of network really only limited by infrastructure**
- Protocols for Ethernet networks are long established standards
- Easy to package many proprietary network protocols for routing on Ethernet
- Brings MCU networks a step closer to web-enabled user interfaces

MCF5282 as a Web Server



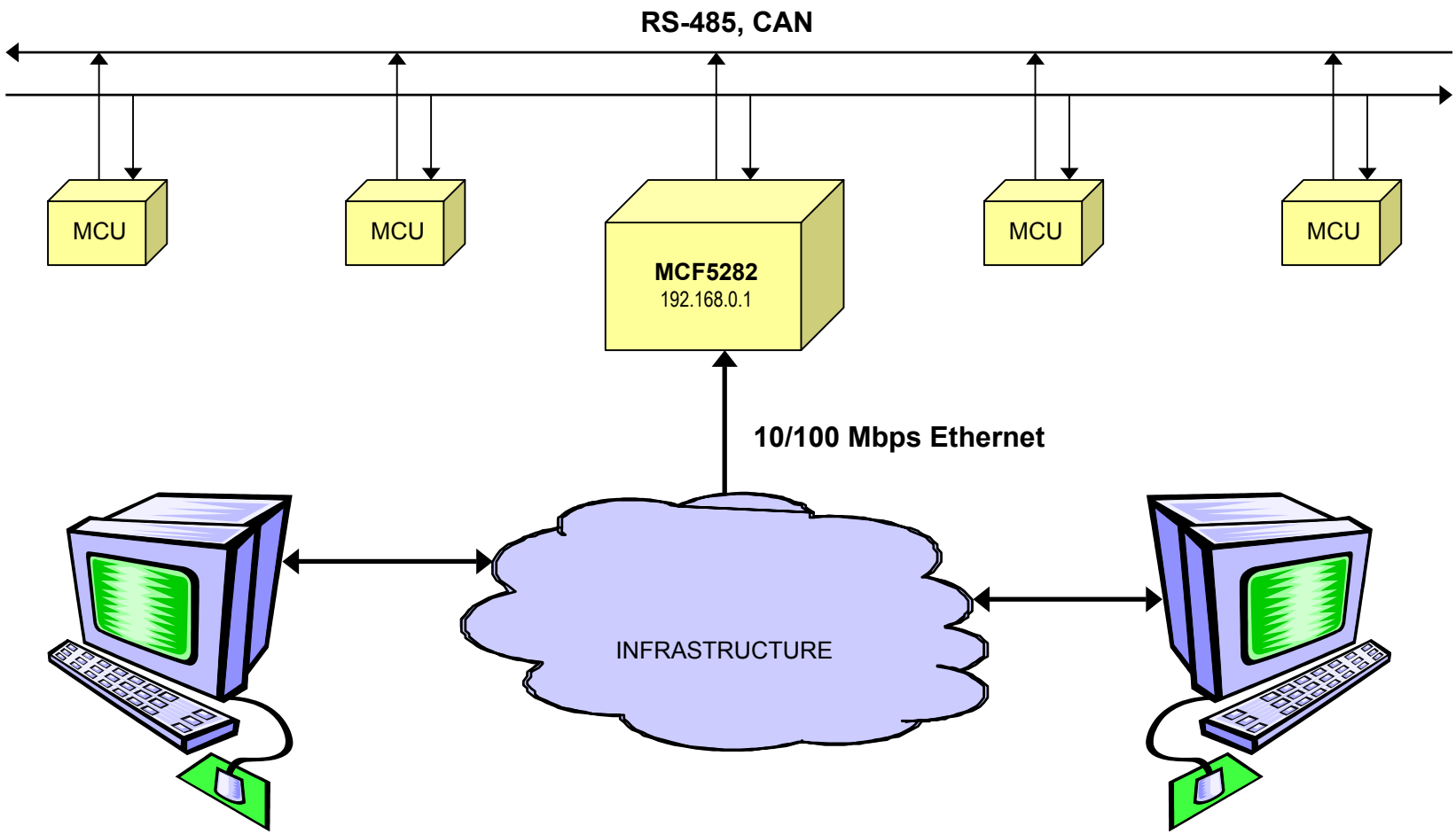
The MCF5282 node is accessible over the network like any other node (web page).

MCF5282 as a UDP/TCP Server



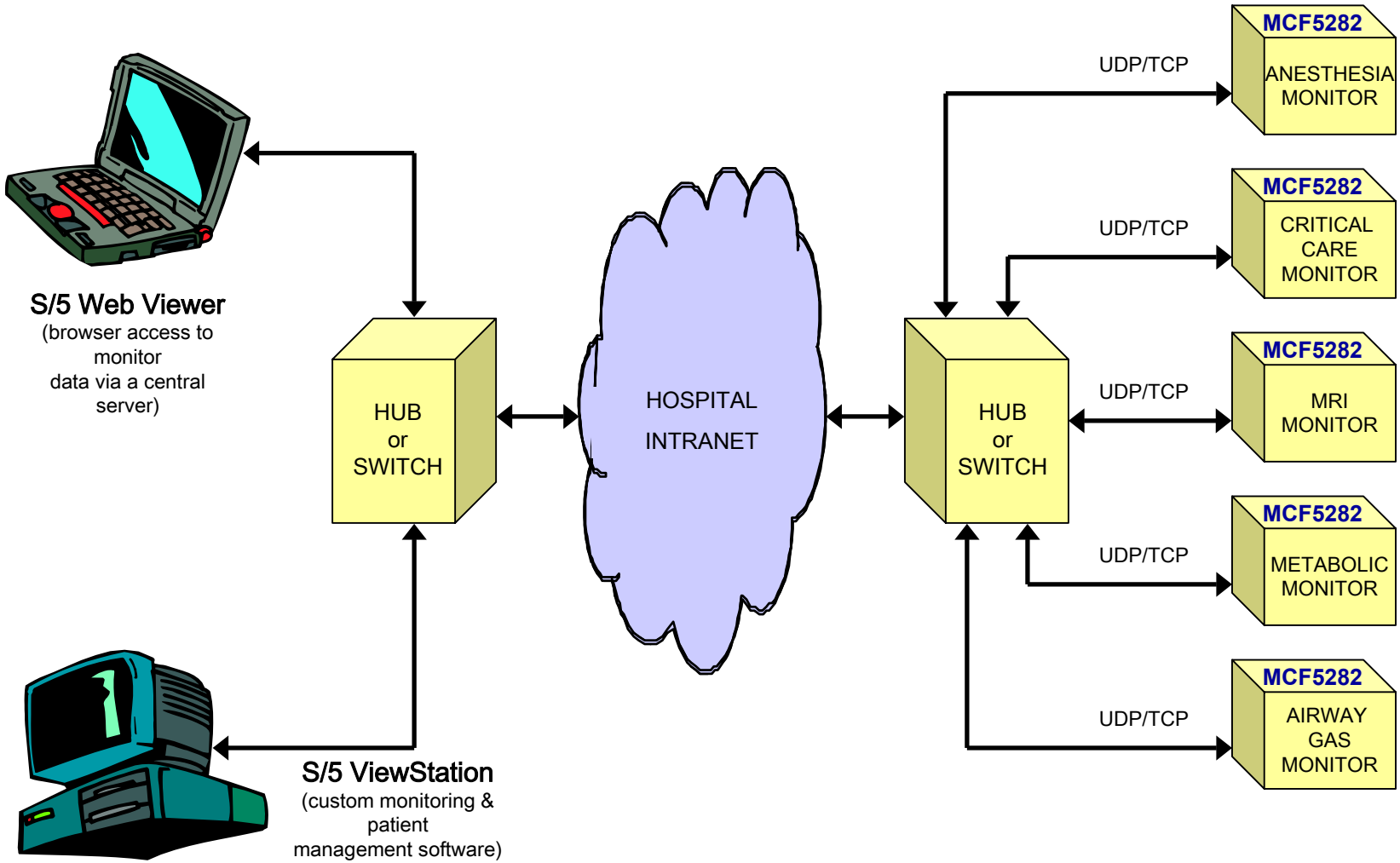
- **The MCF5282 node as accessible over the network using a customized protocol on top of UDP.**
- **The optional server is accessible over the network like any other node (web page) and may access the combined data from all MCF5282 nodes.**

MCF5282 as a CAN Gateway/Router

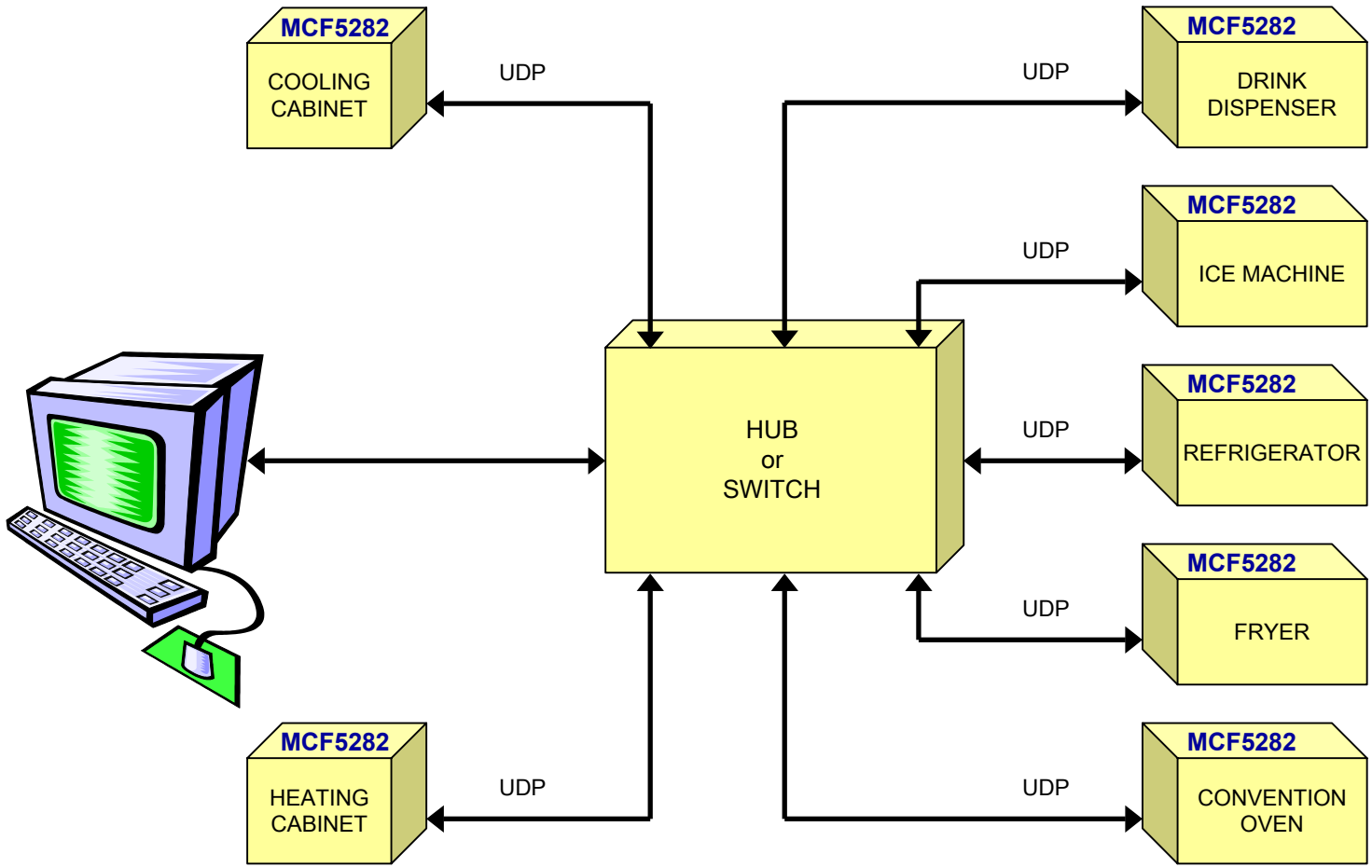


The MCF5282 Gateway is accessible over the Ethernet network as either a Web server or a UDP/TCP server.

MCF5282 in an S/5 Network



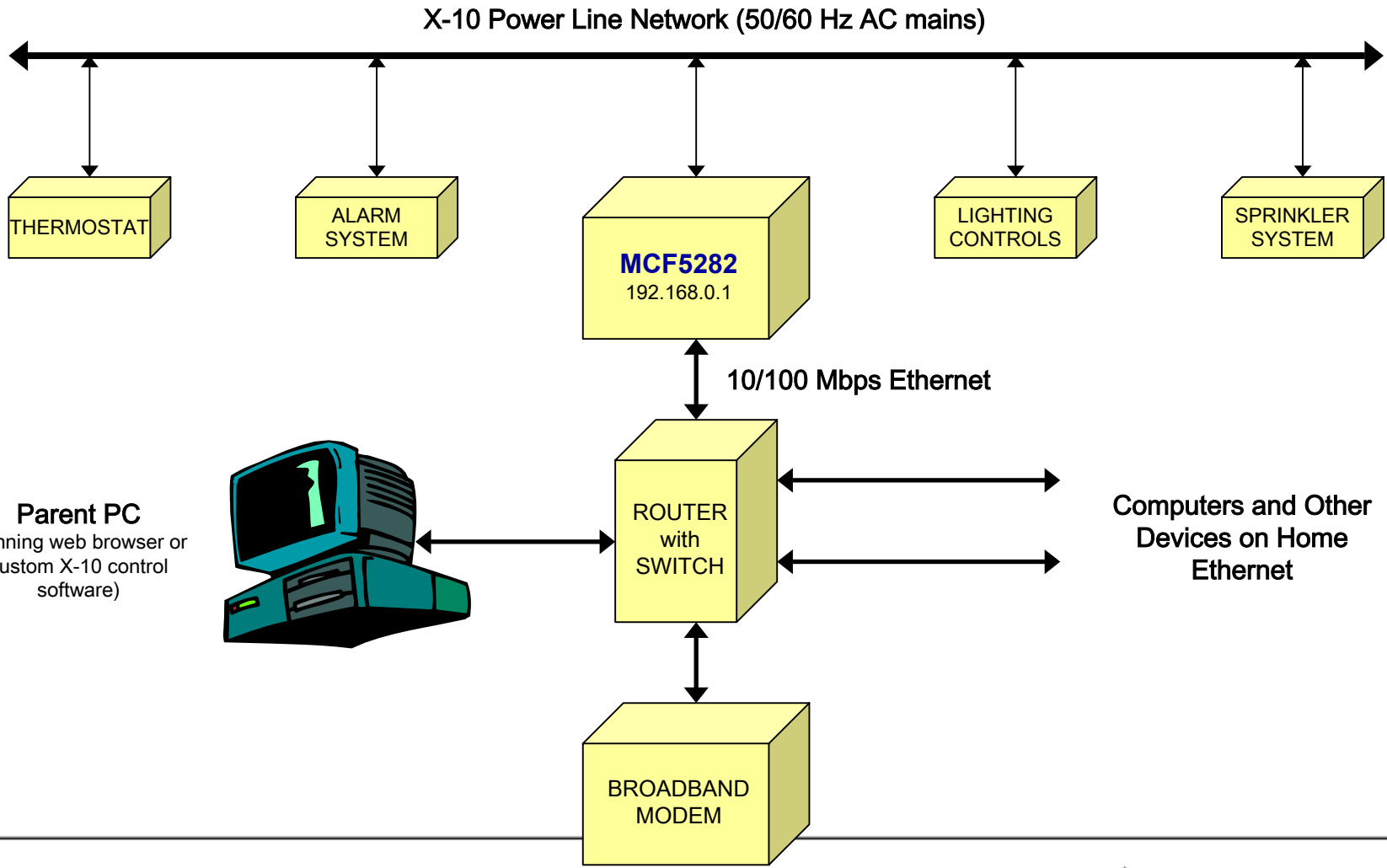
MCF5282 In NAFEM On-line Kitchen Protocol



Back of House PC
(custom front-end software for NAFEM Data Protocol)

NAFEM = North American Association of Food Equipment Manufacturers

MCF5282 ~ Web Interface for X-10 Devices



Roadmaps & Summary

ColdFire Family Roadmap

Features

V5 Core Family
610 MIPS @ 333MHz
Superscalar EMAC
MMU

MCF5407
V4 ColdFire Core
316 Dhrystone 2.1 MIPS @ 220MHz
1 UART, 1 USART, 1 I²C,
16K I-Cache, 8K D-Cache

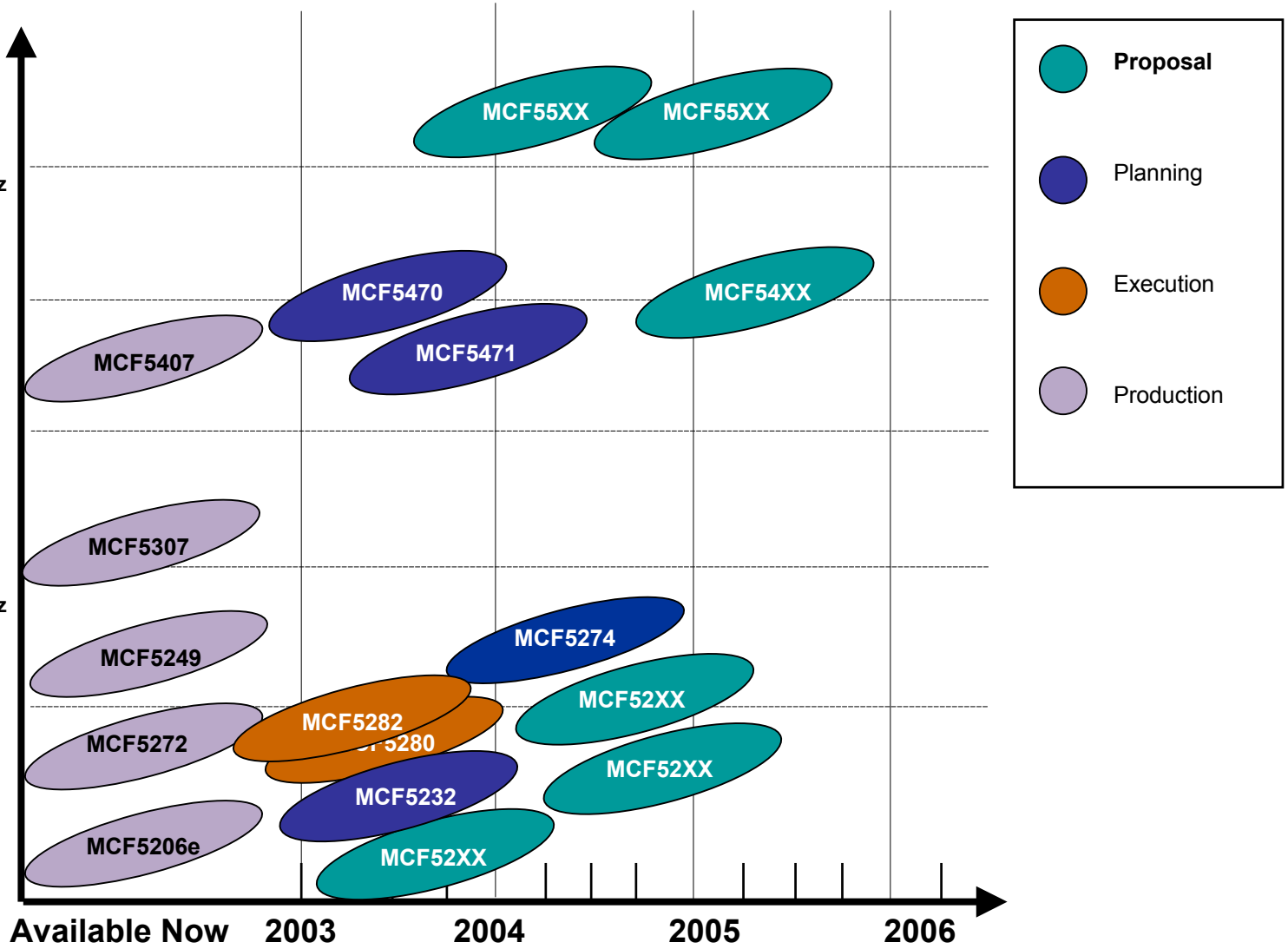
MCF5307
V3 ColdFire Core
75 Dhrystone 2.1 MIPS @ 90MHz
4KB SRAM, 1 I²C, 2xUART
8KB Unified Cache, 4-ch DMA

MCF5282/MCF5280
V2 ColdFire Core
59 Dhrystone 2.1 MIPS @ 66MHz
eMAC, 10/100 Ethernet Controller,
CAN, 512KB/ 0KB Flash

MCF5249
V2 ColdFire Core
125 Dhrystone 2.1 MIPS @ 140MHz
96KB SRAM, eMAC, 2 UART,
2 I²C, 1 QSPI

MCF5272
V2 ColdFire Core
63 Dhrystone 2.1 MIPS @ 66MHz
10/100 Ethernet Controller
2 UART, 1 USB 1.1, 1 FEC, 1 QSPI

MCF5206e
V2 ColdFire Core
50 Dhrystone 2.1 MIPS @ 54MHz
MAC, 2-ch DMA, 2 UART, 1 I²C



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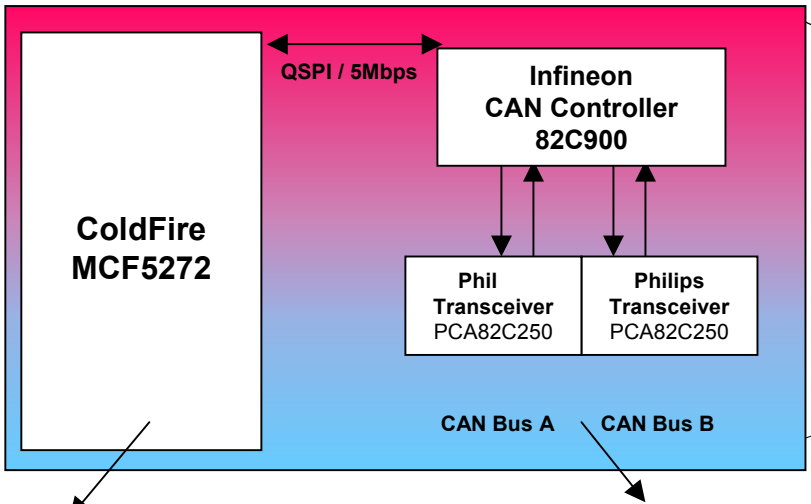
MCF5272 + CAN Reference Design

- Available NOW! -

•Design Aids
Schematics
Driver Software
Applications note detailing hardware design and software development
QSPI Interface Engineering Bulletin

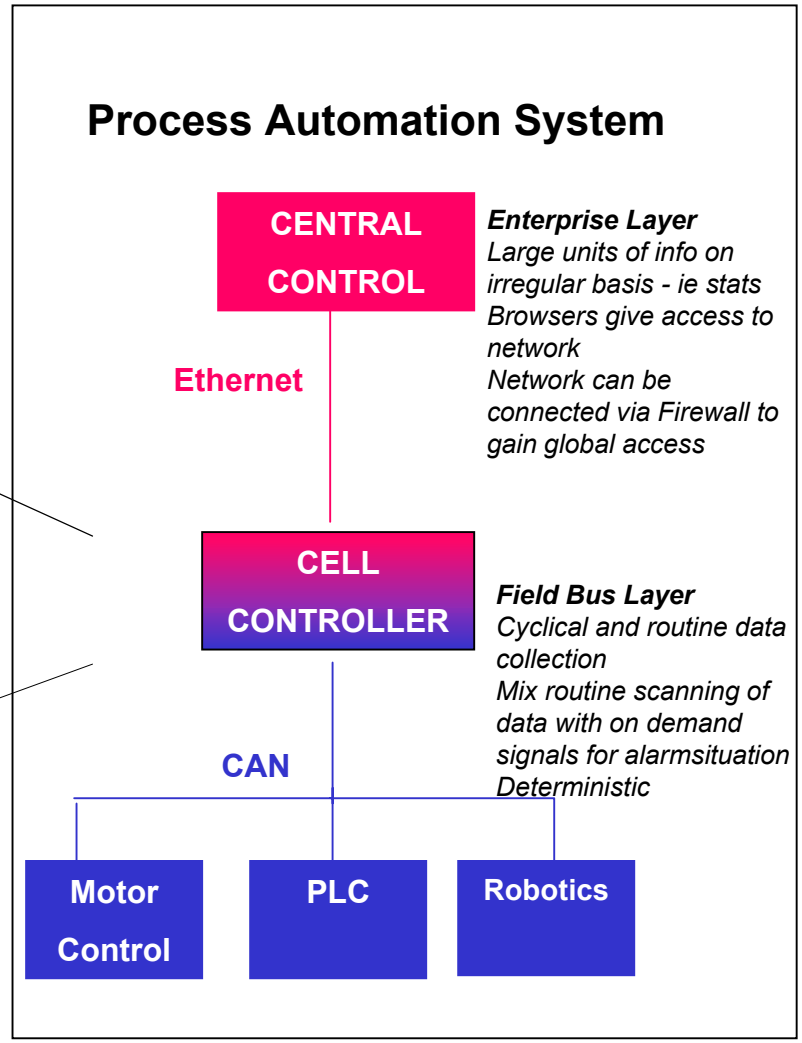
•Design Test and Evaluation
CAN peripheral daughter card for M5272C3 board available on loaner basis



CAN Ethernet Gateway Example

10/100 base T Ethernet
USB
QSPI
MAC/HW Divide
PLIC
Timers

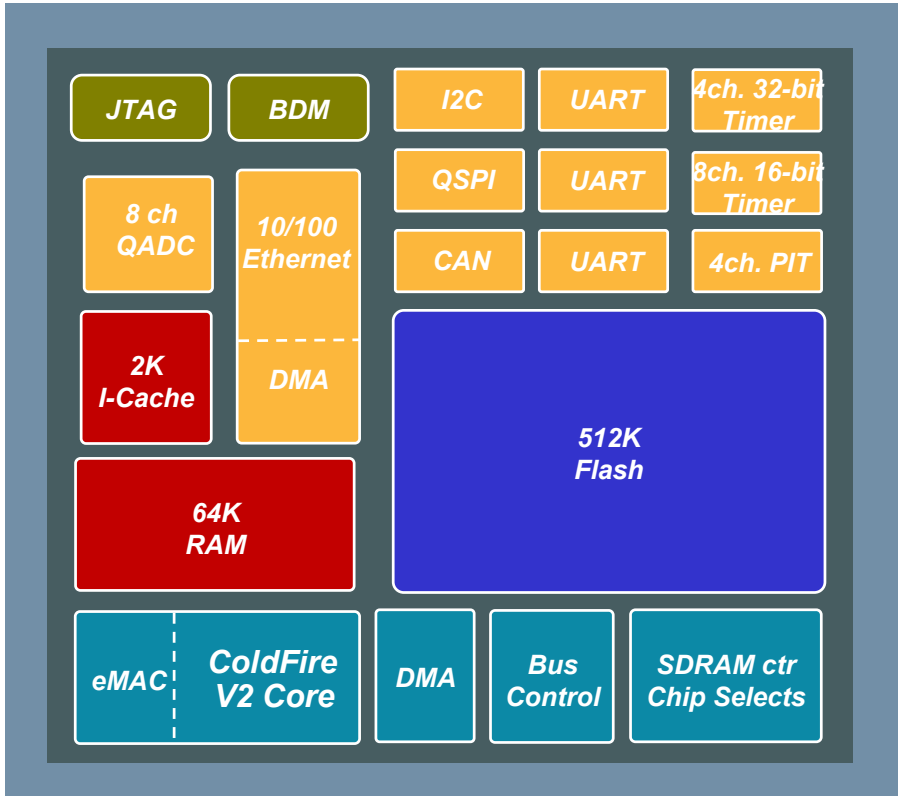
CAN 2.0B
Full CAN Implementation
2 Nodes
32 Message Objects
Time Stamp Function
1MBps Capability



ColdFire : MCF5282

Features

- ColdFire V2 core
  - 59 Dhrystone 2.1 MIPS at 66 MHz
  - Enhanced MAC Module
  - HW Divide
- Integrated Memory
  - 2K I-cache (* for off chip accesses only)
  - 64K RAM
  - 512K Flash (10K W/E cycles, 10 years data retention)
  - 0K Flash on MCF5280
- Integrated Peripherals
  - 10/100 Ethernet MAC (external PHY)
  - Enhanced CAN 2.0B Controller (FlexCAN)
  - 3 UARTs (2 with flow control)
  - Queued Serial Peripheral Interface (QSPI)
  - I2C bus interface
  - 8 ch. 16-Bit Capture/Compare/PWM timers
  - 4 ch. 32-bit timers with DMA
  - 8 ch. Queued 10-bit A-to-D converter
  - 4 ch. DMA controller
  - SDRAM Controller
  - 32-bit non-multiplexed data bus w/7 Chip Selects
  - Up to 152 General-Purpose I/O
  - System Integration (PLL, SW Watchdog)
  - Reset controller with “Brown-out” detection



Speed and Temperature

- 66MHz at -40°C to +85°C
- Planning a higher speed version at 0°C to +70°C

Package

- 256 Ball Plastic MAPBGA Package

ColdFire : MCF5282 Documentation

- MCF5282 Data Sheet - Available now
- MCF5282 User Manual - Available now
- MCF5282 Technical Summary - Available now
- *ColdFire* Pitch Pack including the MCF5282 - Available now
- MCF5282 Mini-Pitch Pack - Available now
- Detailed Technical and Marketing Presentation - Available now
- Application Notes
  - MCF5272 to MCF5282 Migration - **Available now**
  - MMC211x to MCF5282 Migration - **Available now**
- M5282EVB User Manual, including Quick Start Guide - In review, due for release February 2003

Multi-Layered Technical Support

1. Web site with full documentation and FAQs
   - **(http://e-www.motorola.com/)**
2. Technical Information Center (TIC)
   - **(https://e-www.motorola.com/ - Technical Support)**
3. Distributor Field Application Engineer (DFAE)
4. Motorola Field Application Engineer (FAE)
5. Motorola Factory based application engineering group
6. Motorola design and product engineering

The End