DALLAS SEMICONDUCTOR

Application Note 132
Quick Guide to 1-Wire net Using PCs and Microcontrollers

INTRODUCTION

A 1-Wire® net is a communication system where a single master communicates over a single data line plus ground reference with one or more slave devices using the serial 1-Wire protocol. The 1-Wire protocol synchronizes the slave devices to the master. The master is typically a microcontroller or a personal computer with an external 1-Wire interface. A 1-Wire net consists of three main elements: the bus master with 1-Wire interface, the electrical connection between master and slaves, and the slave devices themselves. The master initiates and controls all activities on the 1-Wire net. Data transfer is half-duplex, byte sequential and bit-sequential with the least significant bit of a byte being transmitted first.

Logic

The 1-Wire net uses conventional CMOS/TTL logic levels, with a maximum 0.8V for logic “zero” and a minimum 2.2V for logic “one”. A resistor connects the data line of the 1-Wire net to the 5V supply of the bus master (“resistive” or “weak” pull-up). By means of their open-drain output master and slaves can short-circuit the data line to the ground reference to change the logical state from a 1 to a 0. The weak pull-up is adequate for small 1-Wire nets. For larger configurations the weak pull-up needs to be supplemented by a controlled strong pull-up to compensate for the capacitive- and DC-load of the network and the slave devices in it.

Address

A precondition for any network to function is individual addresses for all devices that are part of the system. Every 1-Wire slave device has a 64-bit guaranteed unique address that is realized as laser-engraved on-chip ROM (Read Only Memory). The address consists of an 8-bit family code, a 48-bit serial number and an 8-bit cyclic redundancy check (CRC) of the first seven bytes. The CRC helps the master to quickly determine whether an address was read without error.

Synchronization

Since the 1-Wire net operates without a continuous timing reference signal, every 1-Wire slave device has its own on-chip time base. This timing logic provides a means of measuring and generating digital pulses of various widths. Timing relationships in a 1-Wire net are defined with respect to time slots. Because the falling slope is the least sensitive in an open drain environment, 1-Wire devices use this edge to synchronize their internal timing circuitry.

Power

With very few exceptions, 1-Wire slave devices obtain their energy for operation from the 1-Wire data line. During times where the voltage on the data line is higher than 2.2V an on-chip capacitor is recharged which keeps the device continuously powered. Without special measures the 1-Wire net cannot provide power for circuits other than 1-Wire slave devices. There are two ways to get additional power to subsystems: a) local wall-transformers with regulated DC output or b) a centralized DC-supply that is independent of the 1-Wire net and is realized by adding an additional pair of wires to the 1-Wire data and 1-Wire ground lead. Note that the extra supply current must not use the 1-Wire ground as a return path. For this reason each location needs its own wall-transformer or DC/DC converter. The voltage of the central DC supply is not critical. For economical reasons 12V or higher should be preferred.

NETWORK TYPES

A 1-Wire net can significantly vary in size and topology. One can differentiate between miniature, simple, typical and complex networks, as shown in **Table 1**. The larger the network the more critical the interface becomes between master and 1-Wire net and the cabling.

Network Types Table 1

	Topology	**Size***	**Cabling**	**Interface****
Miniature	Trunk with several slave devices sitting on a motherboard and plug-in boards **Figure 1**	Up to 5 meters	Non critical	any
Simple	Trunk with several slave devices scattered along a cable **Figure 2**	Up to 25 meters ***	Unshielded twisted pair cable (UTP) recommended	Any except for parallel port adapter
Typical	Trunk with couplers that create access points for buttons or hard-wired local clusters of slaves (LC) **Figure 3**	Up to 125 meters ***	Unshielded twisted pair cable (UTP), CAT 3 or better	Enhanced serial port adapters
Complex	Segmented trunk with a local cluster of slaves at the end of each trunk segment **Figure 4**	More than 125 meters, up to 300 meters	Unshielded twisted pair cable (UTP), CAT 5	Enhanced serial port adapters

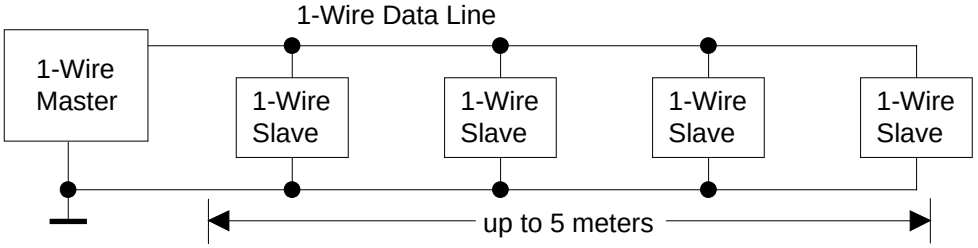
* These numbers are recommended guidelines only. The system may still work if the actual length exceeds the indicated limit. The actual performance is determined by specifics of the installation.

** See subsequent pages for details on adapters and schematics of interfaces.

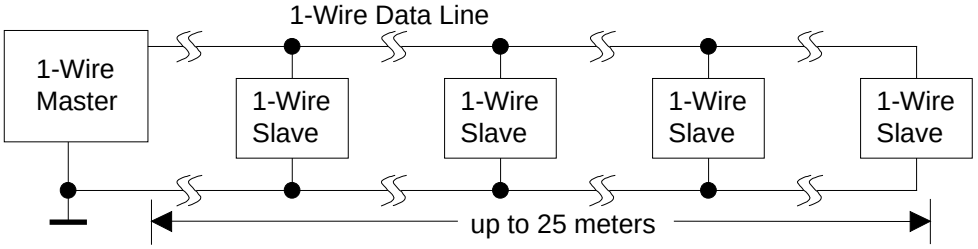
*** A simple or typical network can be extended up to 300 meters using an enhanced serial port adapter and CAT5 cable.

Miniature (**Figure 1**) and simple networks (**Figure 2**) have exactly the same topology. Only the distance between master and slave devices is different. All devices are connected to the master via a single pair of wires, called the trunk, that always participates in the communications. When relying only on a passive "weak" pull-up resistor of 1200Ω expect a maximum population of 80 to 100 slave devices. For a higher number of 1-Wire devices a different topology and/or a more sophisticated 1-Wire interface is required.

Miniature Network Figure 1

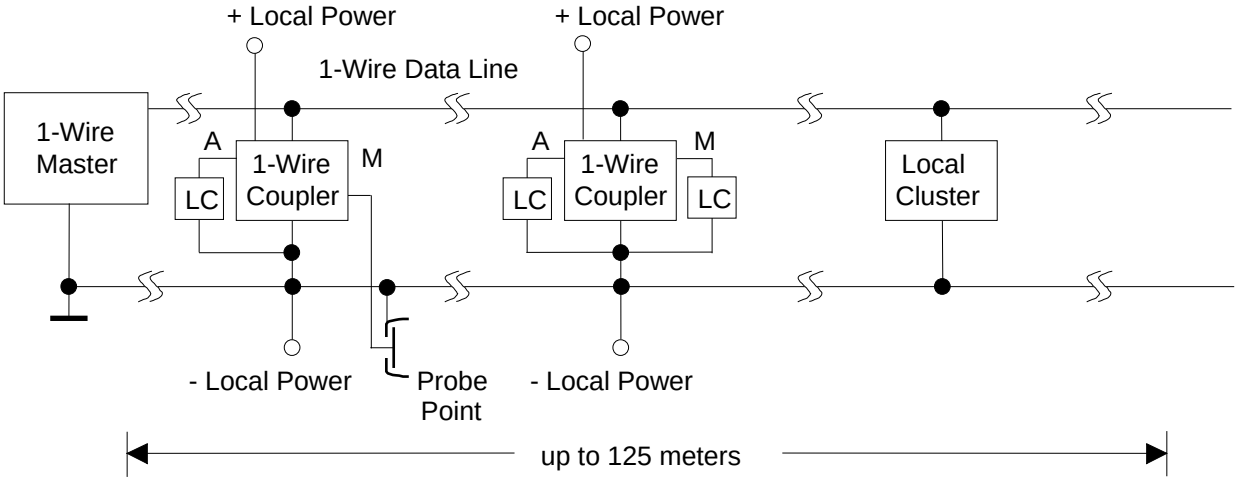


Simple Network Figure 2



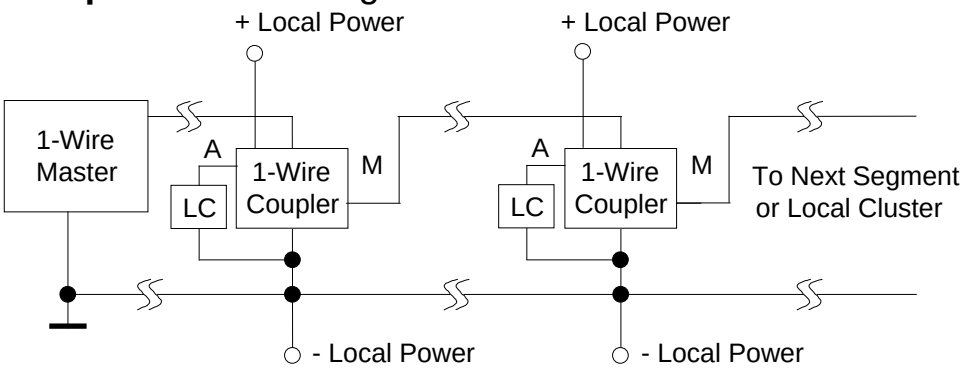
The typical network in **Figure 3** changes the topology by means of DS2409 1-Wire couplers. A local cluster (LC) of slave devices can be a miniature network as well as a simple network. Slave devices connected to the coupler's main (M) or auxiliary (A) output) do not load the network and do not participate in the communication before the master has first addressed and activated that particular coupler. Only one of the two outputs of a coupler can be active at any time. On power-up, both outputs are inactive. With this topology (Figure 3) the software executed by the master must ensure that only one coupler is activated at a time. This is of particular importance for large clusters. With the typical network the capacitive load of the cable is normally a constant and always at its maximum, and a short anywhere on the trunk will bring the entire 1-Wire net down. The power supply for a coupler (and possible loads inside the local cluster) can be the regulated DC output of a wall transformer or a DC/DC converter. It is important to connect the ground reference of the power supply exactly as shown in **Figure 3**. A typical network will work with most serial 1-Wire interfaces if the cable is fairly short. For a cable length near the maximum recommended size an enhanced serial port adapter should be used. See **Figure 5** for details.

Typical Network Figure 3



The topology of the complex network (**Figure 4**) limits the communication solely to those cable segments that are needed to access the targeted slave devices. This minimizes the capacitive load of the cable and keeps the impedance of the network virtually constant. The effects of a short circuit remain local and will usually not bring down the network. Substituting a local cluster by a complex network creates a two-dimensional topology that can reach hundreds of slave devices. The number of couplers in the path to a target device should not exceed 10 unless the cabling is fairly short, e. g. less than 100 meters. An enhanced serial port adapter (**Figure 5**) is adequate for a cable length of up to 300 meters. Larger systems of up to 600 meters require a line driver as shown in **Figure 8**.

Complex Network Figure 4



NETWORK INTERFACES

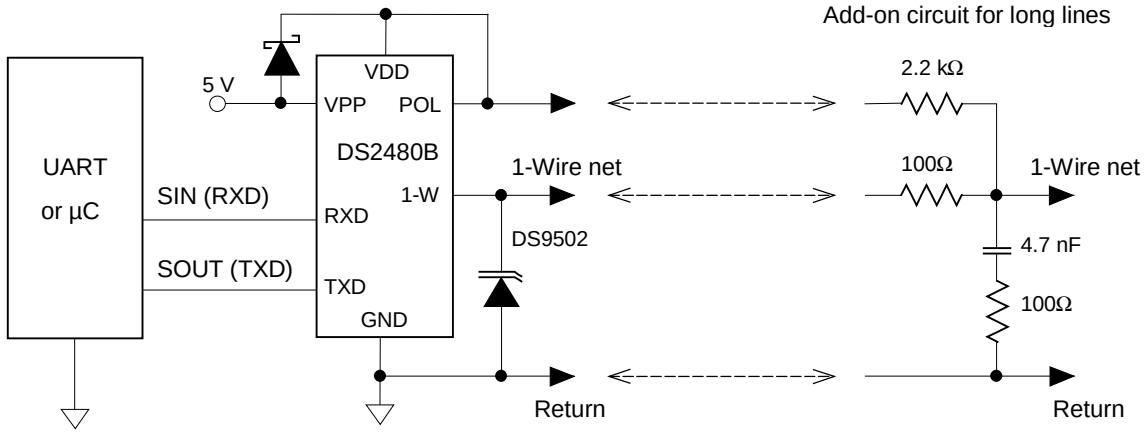
The master interface for a 1-Wire net depends on the type and size of the network. **Table 2** lists part numbers of readily available 1-Wire adapters. If an off-the-shelf product needs to be modified or does not exist, refer to schematics of 1-Wire interfaces.

Interfaces and Recommended Adapters Table 2

	Miniature	**Simple**	**Typical**	**Complex**
Parallel	DS1410E	N/A	N/A	N/A
Serial RS232C	DS9097U, DS1411, DS9097, DS1413	DS9097U, DS1411, DS9097, DS1413	DS9097U, DS1411 modified per Figure 5	DS9097U, DS1411 modified per Figure 5
Serial RS232	DS9097U, DS1411	DS9097U, DS1411	DS9097U, DS1411 modified per Figure 5	DS9097U, DS1411 modified per Figure 5
Serial USB	DS1490 (in preparation)	DS1490 (in preparation)	DS1490 (in preparation)	DS1490 (in preparation)
Serial UART	Figure 5	Figure 5	Figure 5 with add-on circuit	Figure 5 with add-on circuit
Port Pins CMOS/TTL	Figure 6	Figure 6, Figure 7	Figure 7, Figure 8	Figure 8

By nature and design the parallel port adapter works only for miniature networks. The DS9097 and DS1413 are passive adapters that rely on the timing of the serial port to generate the 1-Wire signals. With these two adapters the 1-Wire ground reference is different from the computer's ground reference. The DS9097U and DS1411 are active adapters that use the DS2480B as a 1-Wire line driver. They operate essentially like the UART interface in **Figure 5**. If the active cable length of a 1-Wire net is 100 meters or longer it is necessary to include the "add-on circuit for long lines" between the DS2480 and the 1-Wire net. The recommended DS2480B timing setup (flexible speed) is shown in **Table 3**.

UART (Serial Port) Adapter with DS2480B Chip Figure 5

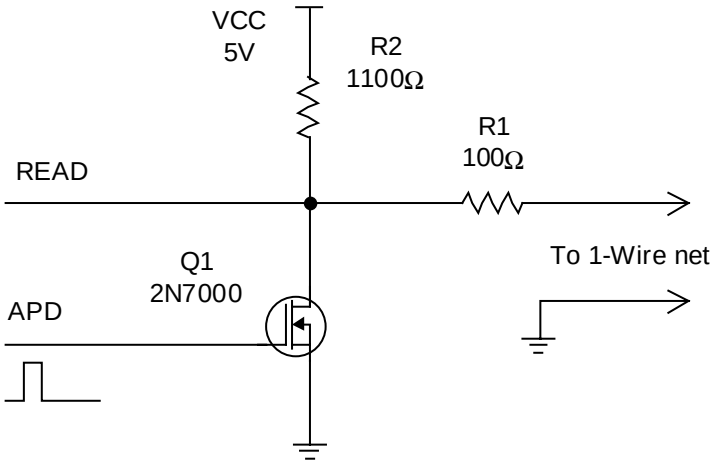


DS2480B (DS9097U, DS1411) Timing Setup Table 3

	Active cable length					
Parameter	≤ 50 m	0 to 100 m	0 to 150 m	0 to 200 m	0 to 250 m	0 to 300 m
Slew rate	2.2 V/µs	2.2 V/µs	1.65 V/µs	1.37 V/µs	1.1 V/µs	0.83 V/µs
t_{LOW1}	8 µs	8 µs	9 µs	10 µs	11 µs	12 µs
t_{DSO} (=t_{REC0})	5 µs	6 µs	7 µs	8 µs	9 µs	10 µs

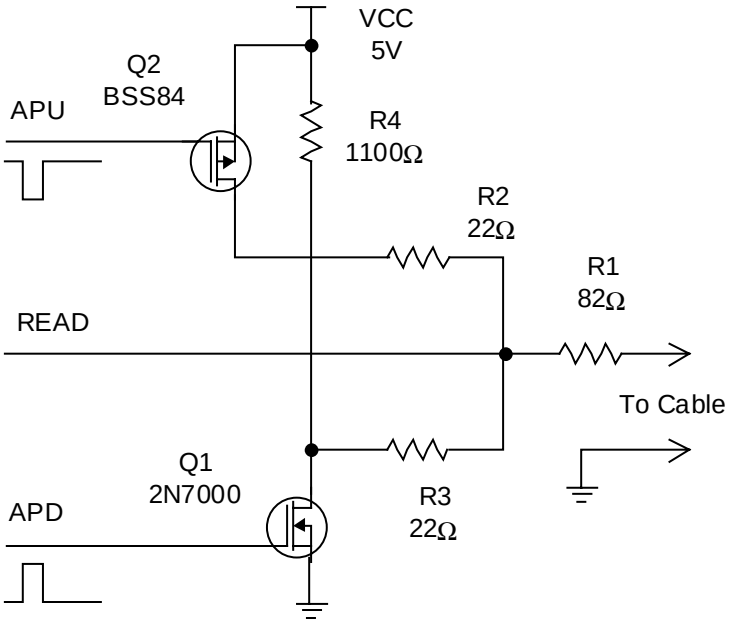
Figure 6 shows a minimum microcontroller to 1-Wire net interface. It requires one port pin to write to the 1-Wire net and one port pin to read. The microcontroller is responsible to generate the correct timing for the 1-Wire communication. Since this is a real-time application the communication software must be written in assembly language and the time to execute every command of the time-critical sections and loops at the selected crystal frequency must be accounted for. For the recommended timing see Table 4, first row, parameters APD0, APDR, MS and IDLE. If assembly language is not an option and an UART is available, a circuit as in Figure 5 should be used.

Minimum Microcontroller Interface Figure 6



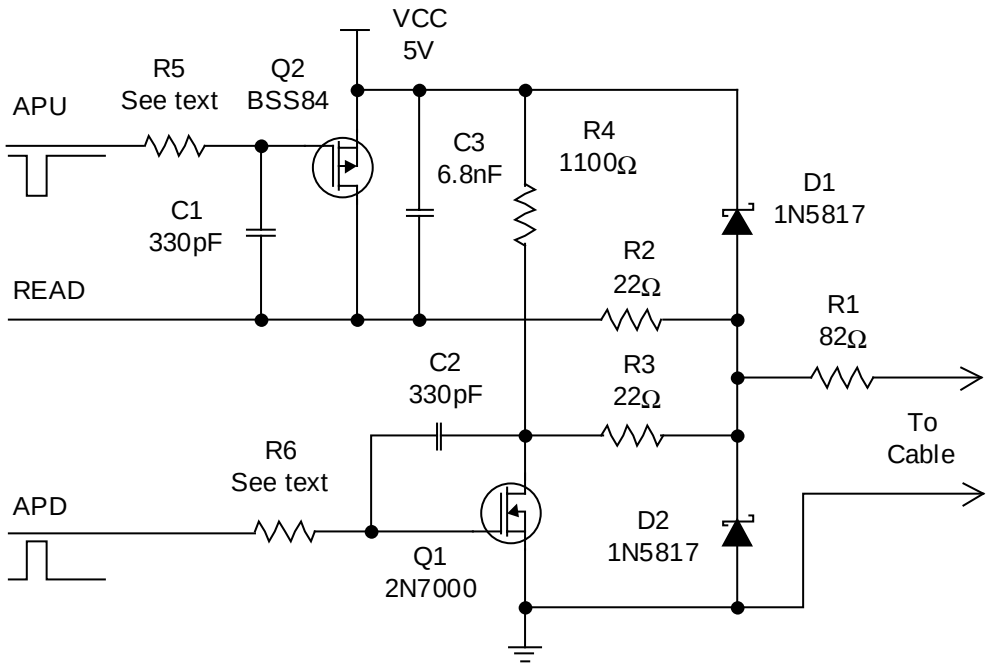
The improved interface of **Figure 7** is essentially the same as in **Figure 6.** The main difference is the transistor Q2 that allows faster recharging of the 1-Wire net by supplementing weak pull-up resistor R4. For this reason this circuit can work with larger networks. Since this circuit does not control the edges of the 1-Wire signals it should not be used beyond 100 meters. As before, the microcontroller is in charge of correctly activating Q1 for writing and Q2 for active pull-up. Reading is the same as with the previous circuit. For the recommended timing see Table 4, first two rows, parameters APD0, APU, APDR, MS and IDLE.

Improved Microcontroller Interface Figure 7



The circuit in **Figure 8** expands the 1-Wire net to distances of up to 600 meters. Compared to **Figure 7** this circuit adds slew rate control for the falling (R6, C2) and rising (R5, C1) edges. R1 in series with R2 or R3 terminates the driver end of the line during transitions from low to high and high to low, respectively. The path R1-R2-C3 provides AC termination for the presence pulse generated by slave devices. The optimal slew rate setting is achieved if the voltage drop from 5V to 0V takes twice as long as the signal propagation delay from the driver to the far end of the cable and back (roundtrip propagation delay). The slew rate for the rising edge is not that critical. As a recommendation it should be four times as fast as that of the falling edge, but not faster than 5V/µs.

All-Purpose Microcontroller Interface Figure 8



If the active cable length changes, the slew rate needs to be adjusted. For adjustable slew rates one can realize R5 and R6 as several resistors in parallel but connected to different ports of a microcontroller. As with the circuits in **Figure 6** and **7** a microcontroller running real-time software is required to generate the control signals APU (active pull-up) and APD (active pull-down) and to sample the logical status at appropriate times MS (master samples) to read from the 1-Wire net. Also needed (not shown in the schematic) is a comparator that allows the micro to detect whether the voltage on the 1-Wire net has risen above a threshold of 0.95 V (V_{IAPO}, as in the DS2480B data sheet). For the recommended timing parameters, slew rates and values for R5 and R6 depending on cable length refer to **Table 4**.

TIMING ALGORITHMS AND PARAMETERS

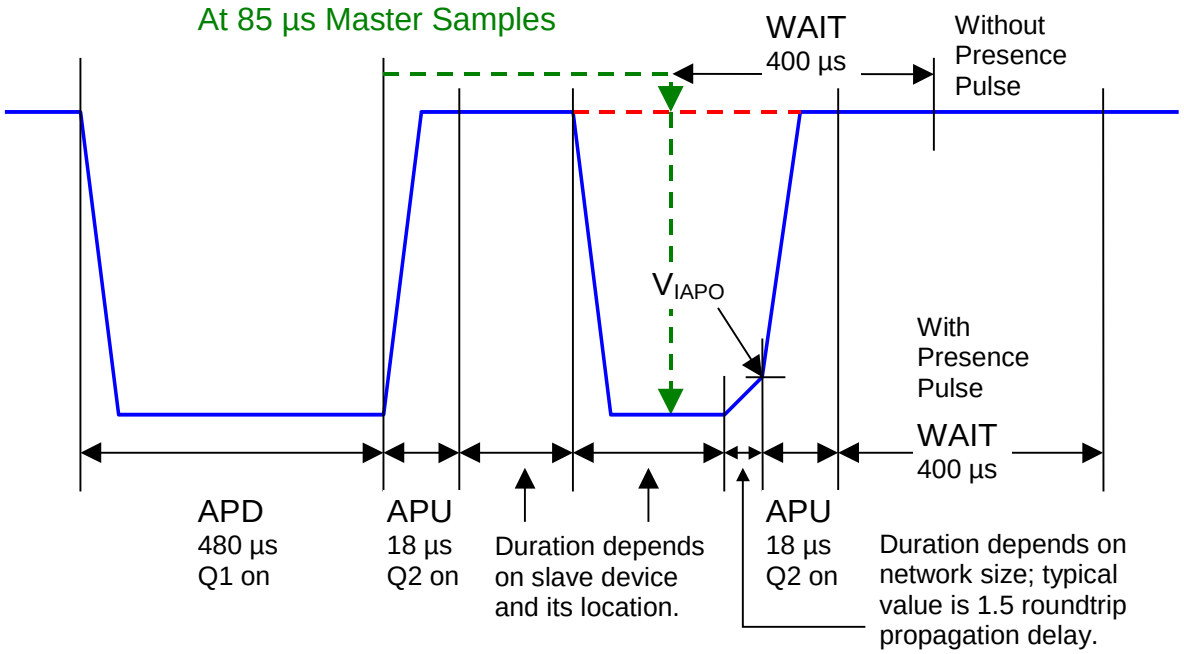
Reset/Presence Detect (Figure 9)

1) Active pull-down (APD) for 480 µs
2) Active pull-up (APU) for 18 µs
3) Test logic level at 85 µs after APD is over
4) *If logic level = low:* then as soon as voltage has reached V_{IAPO}: APU for 18 µs; *endif*.
5) Wait 400 µs

NOTE:

Step 4) can be implemented in software as a loop that checks the comparator output and generates the APU signal as V_{IAPO} is reached.

Microcontroller Reset/Presence Detect Cycle Figure 9

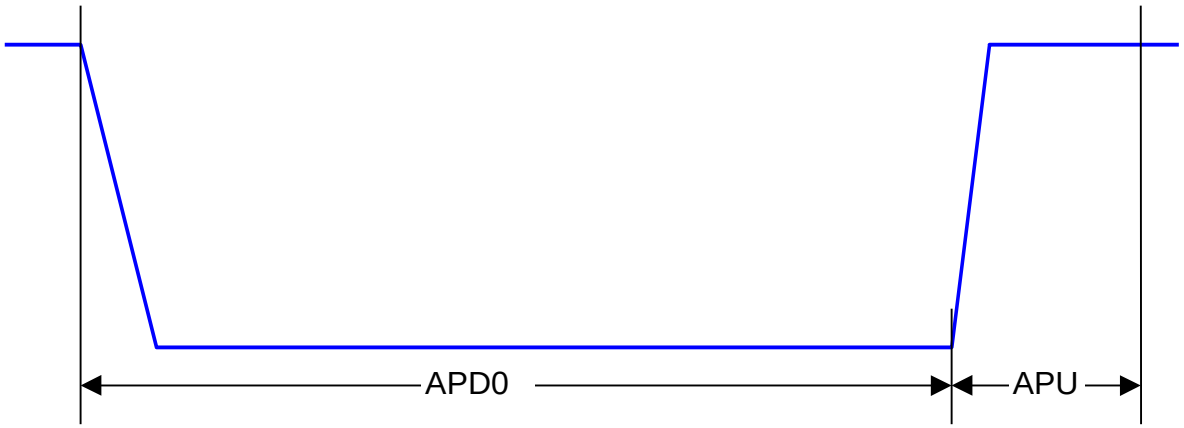


The duration of APU and the Master Sampling point are calculated for a 600-meter cable. These values also work for shorter cables.

Write-0 Time Slot (Figure 10; see Table 4 for the appropriate timing values)

1) Active pull-down APD0
2) Active pull-up APU
3) Wait (≥ 0 µs, optional)

Microcontroller Write-0 Timing Figure 10



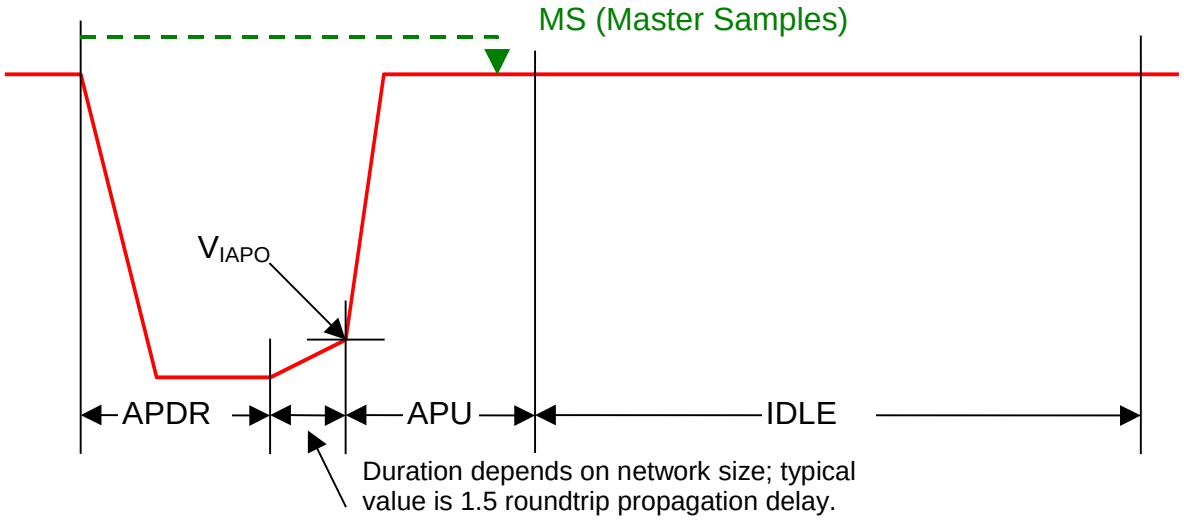
Read/Write-1 Time Slot (Figures 11 and 12; see Table 4 for the appropriate timing values)

1) Active pull-down APDR
2) As soon as V_{IAPO} is reached: APU
   Test logic level at MS (MS starts counting at the beginning of the time slot)
3) *If logic level = high:* then wait until APU is over; wait IDLE; *endif*. (case shown in Figure 11)
4) Wait (≥ 0 µs, optional)

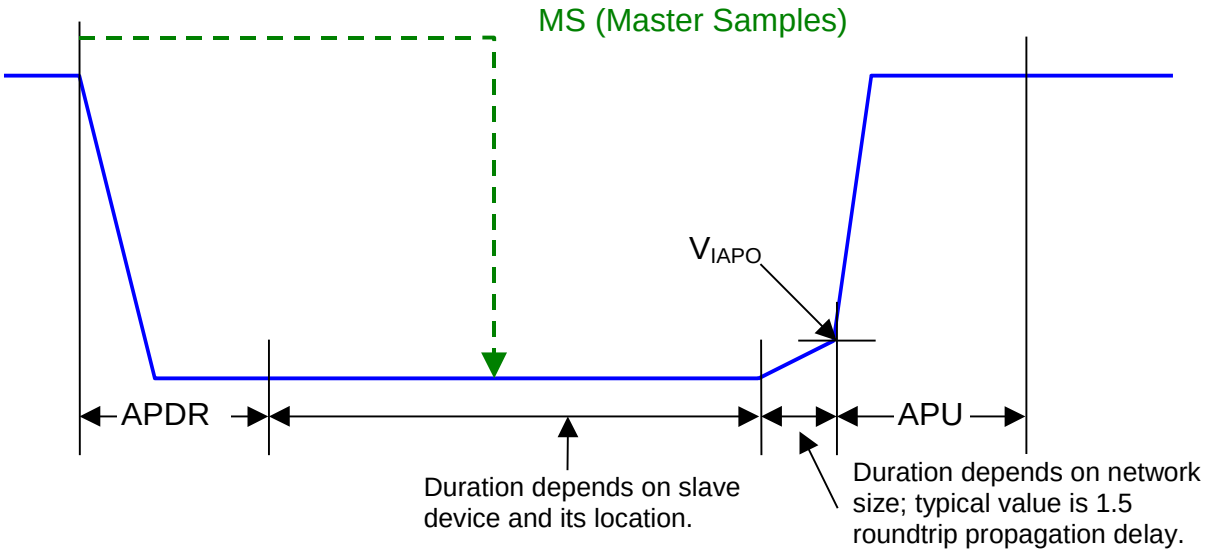
Step 2) consists of two concurrent processes: testing at a predetermined point in time and generating a signal at a predetermined voltage. It may be necessary to use a programmable timer to generate the APU signal when the V_{IAPO} comparator's output changes.

When generating a write-1 Time Slot without any intention to read from the 1-Wire net, the logic level needs not be tested at MS. For Step 3) the logic level is high, requiring the IDLE time after APU is expired.

Microcontroller Write-1 (Read-1) Timing Figure 11



Microcontroller Read-0 Timing Figure 12



Microcontroller Timing Parameters for Read and Write Table 4

	Parameter							
Active Cable Length	APD0 µs	APU µs	APDR µs	MS µs	IDLE µs	PD slew rate V/µs	R5 Ω	R6 Ω
≤ 50 m	46	3	1	22	43	5	130	510
0 to 100 m	47	3	2	23	40	2.5	270	1000
0 to 150 m	48	5	3	23	38	1.75	360	1500
0 to 200 m	49	6	4	24	36	1.3	510	2000
0 to 250 m	49	8	5	24	34	1.0	680	2700
0 to 300 m	50	9	6	25	31	0.85	750	3000
0 to 350 m	51	10	7	26	29	0.75	820	3600
0 to 400 m	52	12	8	26	28	0.65	1000	3900
0 to 450 m	53	13	9	27	24	0.58	1100	4300
0 to 500 m	53	15	10	27	22	0.53	1200	4700
0 to 550 m	54	16	11	28	20	0.48	1300	5600
0 to 600 m	55	18	12	28	18	0.44	1500	6200

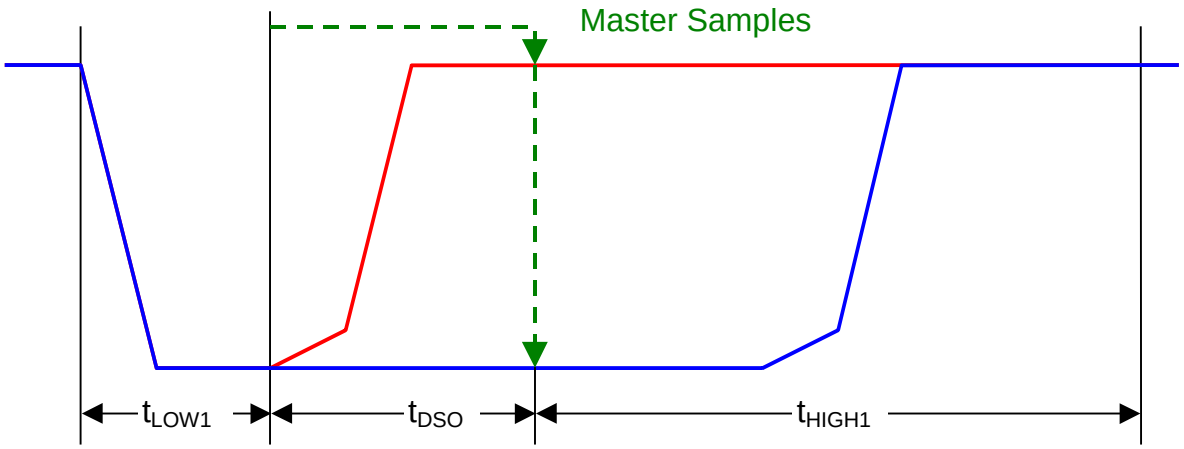
ADPR is approximately twice the roundtrip propagation delay at the given cable length.

The values for APD0 and MS in Table 4 seem to contradict the values listed for their equivalents t_{LOW0} and t_{RDV} in 1-Wire device data sheets. The numbers in the data sheets apply for the full temperature and voltage range of 2.8V to 6.0V. Since all the driver circuits discussed in this document provide a 5V environment, the variation of the time base of each 1-Wire device is narrower, spanning from 22 µs to 45 µs rather than 15 µs to 60 µs.

The APD0 and MS values in Table 4 grow with the cable length to compensate for the slower slew rate. APD0 is not critical and may be up to 60 µs for all cable lengths, if desired. The MS values in the table reflect the sampling point of a fast 1-Wire slave device in the 5V long cable length environment. For short cables the MS value may be chosen significantly shorter with a minimum of twice the APDR value. A shorter than listed MS value is also needed if the 1-Wire net includes DS2405 devices of revision B2. With these devices the time base may be as fast as 19 µs which limits their suitability for large networks.

With the DS2480B the master sampling MS is constructed as the sum of t_{LOW1} (equivalent to APDR) and t_{DSO} (Figure 13). The parameter t_{DSO} also serves as the value for write-0 recovery time (Figure 14), which is similar to APU. For this reason the values for t_{DSO} in Table 3 are approximately the same as APU in Table 4. The DS2480B does not support the range for t_{LOW1} as recommended in Table 4. The t_{LOW1} values in Table 3, therefore, are a compromise to position the master sampling near the recommendation in Table 4. With the DS2480B the timing of the rising edge is different from the microcontroller interfaces of Figures 7 and 8. For more information on this see Figure 14 or the DS2480B data sheet. In contrast to the circuit in Figure 8 the DS2480B does not control the slew rate of the rising edge.

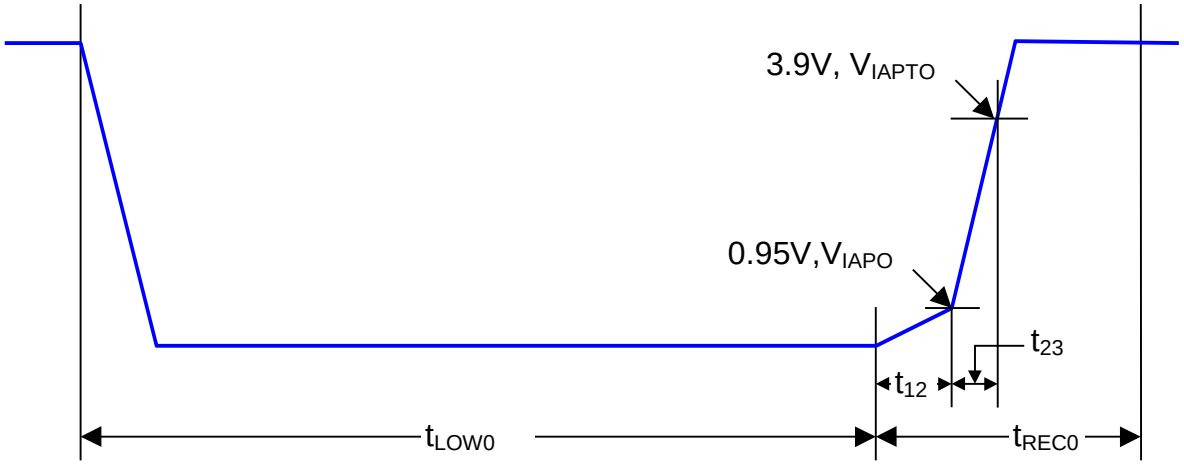
DS2480B Write-1 and Read Timing Figure 13



t_{LOW1} is variable, 8 to 15 µs t_{DSO} is variable, 3 to 10 µs t_{HIGH1} is fixed to 49 µs

The duration of t_{DSO} is the same as of t_{REC0}.
For details on the rising edge see the DS2480B Write-0 Timing Diagram.

DS2480B Write-0 Timing Figure 14



t_{LOW0} is fixed to 57 µs t_{REC0} is variable, 3 to 10 µs

t_{12} depends on network size; typical value is 1.5 roundtrip propagation delay.
t_{23} depends on network size and load.
For correct operation, the 3.9V threshold needs to be reached at least 2 µs before t_{REC0} expires. The active pull-up continues for 2 µs after the 3.9V threshold is reached.

MUST NOT DO

- Star configuration without couplers
- Create branches without couplers
- Use 1-Wire return as power ground
- Run cable near and/or in parallel with power lines

MAXIMUM RELIABILITY DESIGN Table 5

Measure	**Resulting effects**
100Ω resistor in data line (termination) **Figures 5 to 8**	• Eliminates ringing • Helps control the slew rate • Reduces sensitivity to grounding of unused wires or shielding • Allows the use of lower quality cables
AC-coupled near-end termination **Figures 5 and 8**	• Eliminates near-end reflection of the presence pulse
Slew rate control	• Provides clean signals • Makes systems work that have slaves scattered along the net • Reduces RF emission
Active pull-up	• Gets the signal to 5V faster • Gets more energy to the slaves • Minimizes the effects of the droop when the slaves start recharging their parasite power supply • Allows more slave devices in the network
Adaptation of waveforms to the active cable length	• Maximizes energy transfer to the slaves • Maximizes communication speed at any cable length • Maximizes the possible network size
Delayed master sampling	• Makes systems work that have a long cable between master and the nearest slave

Tagging Guidelines

The examples in this document show the flexibility and advantages of the 1-Wire net. 1-Wire slave devices, in particular sensors and switches, can be grouped together into systems that can perform sophisticated sensing, reading and control operations. A new 1-Wire master that is confronted with an installed network needs to have knowledge about the system and the associations and functions of its slave devices to operate it correctly. For example, the master might need to know that PIOA of a particular DS2406 in a 1-Wire net controls the green LED at the rear door.

To easily describe these associations and operations, a 1-Wire TAG format has been developed. The document titled "Tagging Guidelines for 1-Wire Sensors and Instruments" is included in a kit that contains documentation, source code, and demonstration programs to implement the tagging of 1-Wire sensors with self-registering capabilities. At the time this document was written the kit was available for downloading at "ftp://ftp.dalsemi.com/pub/auto_id/softdev/softdev.html".

The 1-Wire TAG can reside in a traditional database or it can even be placed in the memory of a 1-Wire memory device. By carrying the 1-Wire TAG with the sensor cluster, it can be self-configuring when presented to a new master application. If it is impractical or not desired to keep the 1-Wire TAG with the cluster, it can also reside on a home Internet site. The master application can then take one of the unique 1-Wire addresses found on the system to request the appropriate 1-Wire TAG from the hosting site.

Dallas Semiconductor plans on maintaining the standard for the 1-Wire TAG and making it accessible at 'www.1-Wire.net'. There are also plans under way to provide hosting services for the 1-Wire TAG data on the same site.