AEROFLEX

A passion for performance.

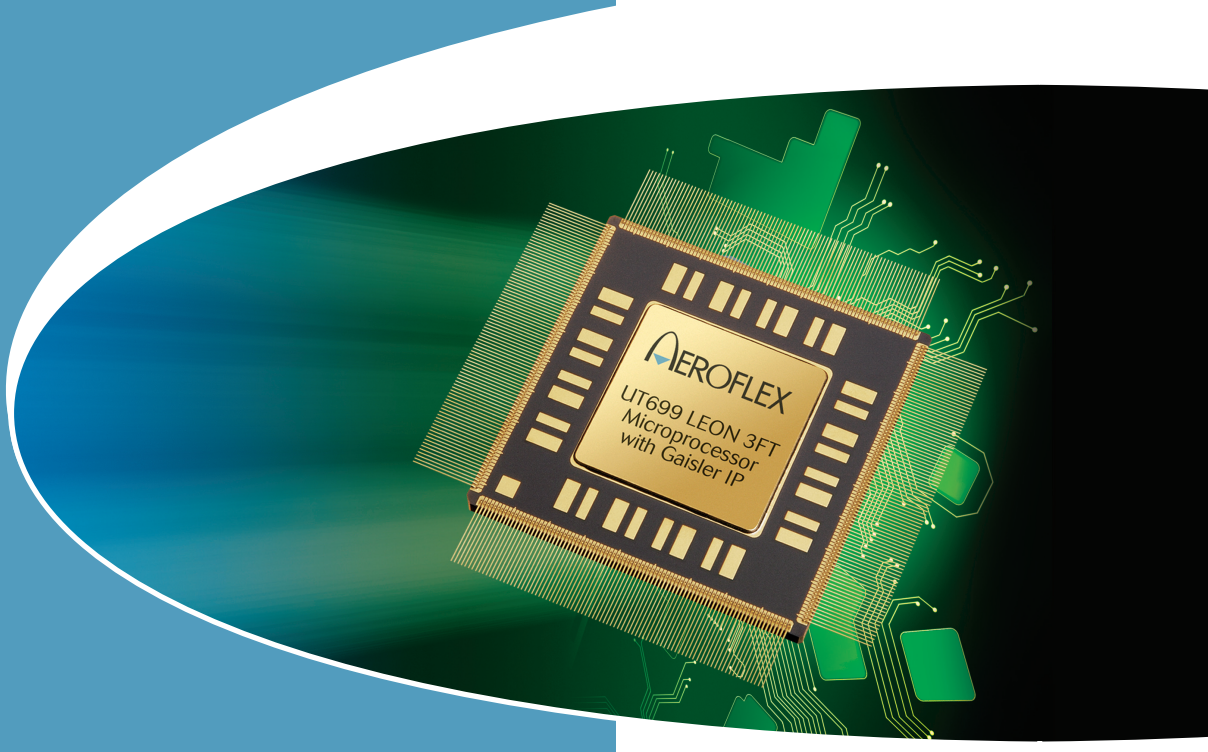
UT699 LEON 3FT from Aeroflex Colorado Springs

Designed for operation in harsh environments

Fault Tolerant architecture

Guaranteed radiation performance

Real-time software operating system support



LEON 3FT V8 SPARC™ Microprocessor

Definitions

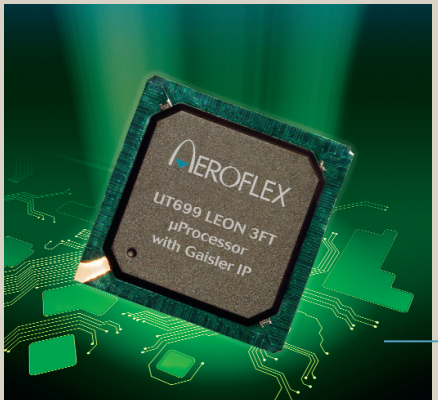
LEON microprocessor

LEON is a 32-bit CPU microprocessor core, based on the SPARC™ V8 RISC architecture and instruction set. The core is highly configurable, and suitable particularly for system-on-chip (SOC) designs. LEON 3FT is a Fault-Tolerant (FT) version, designed for operation in harsh, radiation-prone environments, and includes functionality to detect and correct single event upset (SEU) errors in all on-chip RAM memories.

Definitions

SPARC™ architecture

SPARC (Scalable Processor Architecture) is a RISC instruction set architecture developed by Sun Microsystems. SPARC is a registered trademark of SPARC International, Inc., an organization established to create a larger ecosystem for the design by promoting, licensing, and providing conformance testing. As a result, the SPARC architecture is fully open and non-proprietary.



WE OFFER DEVELOPMENT TOOLS AND REAL-TIME OPERATING SYSTEM SUPPORT...

An advantage to working with Aeroflex's UT699 is the extensive library of development tools. Since the UT699 is SPARC™ V8 compliant, compilers and kernels for SPARC V8 are based on industry standard development tools.

Aeroflex offers a full software development suite including a C/C++ cross-compiler system based on GCC and the Newlib embedded C-library. The BCC compiler system allows cross-compilation of single and multi-threaded C and C++ applications for the LEON 3FT family and includes a small run-time kernel with interrupt support and Pthreads library.

For multi-threaded applications, SPARC-compliant ports are available for the the following operating systems: eCos, RTEMS, Linux, VxWorks, Nucleus, ThreadX and LynxOS.

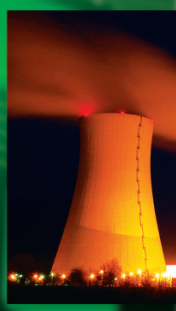
To support the software development process, a simulator and a debugger are provided. TSIM is a high-performance SPARC-architecture instruction simulator capable of emulating the UT699 LEON 3FT. GRMON is a debug monitor for the UT699 processor. It communicates with the UT699 debug support unit (DSU) and allows non-intrusive debugging of the complete target system.

...PLUS PROVEN IP

The Aeroflex Gaisler GRLIB IP Library is an integrated set of reusable IP cores, designed for system-on-chip (SOC) development. The IP cores are centered around the common on-chip bus and use a coherent method for simulation and synthesis. The library is vendor independent, with support for different CAD tools and target technologies. A unique plug-and-play method is used to configure and connect the IP cores without the need to modify any global resources.

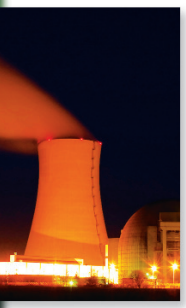
www.aeroflex.com/Leon

800-645-8862

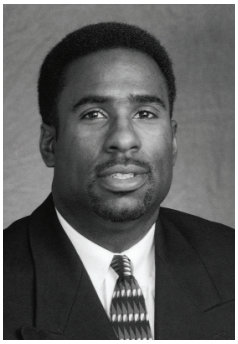


Aeroflex offers two differentiators in processing for harsh environments:

1. Guaranteed radiation performance
2. Best software support in the industry



We know that our customers need high-performance products and solutions to facilitate system processing and interconnect. In 2008, Aeroflex purchased Gaisler Research, a world leader in this field, specifically to develop HiRel system-on-a-chip (SOC) processing solutions. Our UT699 LEON 3FT-based microprocessor — designed with Aeroflex Gaisler's GRLIB proven IP architecture — offers an assured processor and software solution for applications requiring reliable, fault-tolerant computing and control.



— Anthony Jordan
Director of Standard Products

UT699 FEATURES

- Implemented on a 0.25µm CMOS technology
- Flexible static design allows up to 66MHz clock rate
- 53MIPS throughput via 66MHz base clock frequency
- Internally configured clock network
- On-board programmable timers, interrupt controllers
- High-performance fully-pipelined IEEE-754 FPU
- Power-saving 2.5V core power supply
- 3.3V I/O compatibility
- Hardened-by-design flip-flops and memory cells

UT699 CORES

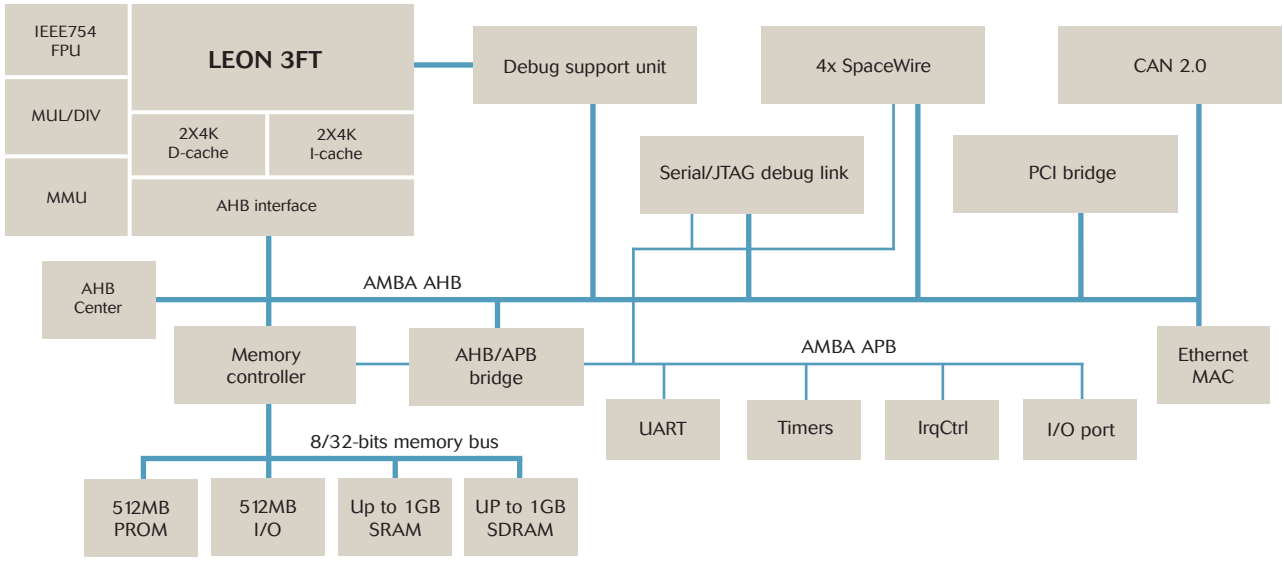
AMBA bus interconnects a peripheral rich environment:

- 10/100 Base-T Ethernet port
- Integrated PCI 2.2 compatible core
- Four integrated multi-protocol SpaceWire nodes with two supporting the RMAP protocol
- Two CAN-compliant 2.0 bus interfaces
- Multifunctional memory controller

UT699 OPERATIONAL ENVIRONMENT

PARAMETER	LIMIT	UNITS
Total Ionizing Dose (TID)	3E5	rads(Si)
Single Event Latchup (SEL)	>108	MeV-cm²/mg
Neutron Fluence	1.0E14	n/cm2

UT699 BLOCK DIAGRAM



LEON 3FT SPARC™ V8 MICROPROCESSOR EVALUATION BOARD

The GR-CPCI-UT699 development board is capable of running at a system clock speed of 66MHz. The board is a 6U cPCI form factor and can also be used in a standalone bench-top configuration.

The board supports 32-bit/33MHz PCI, 10/100 Base-T Ethernet, four SpaceWire ports capable of running up to 200Mbits/s, two CAN ports, on-board FLASH, SRAM, and SDRAM. A socket for a PROM device and an USB debug port are also on-board.

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Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused.

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