Actel Space-Flight FPGAs
Product Update and Roadmap

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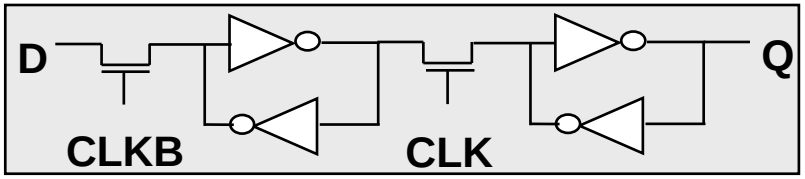
Actel Company Overview

- Established FPGA Supplier
  - First FPGA shipped – 1988
  - First space FPGA shipped – 1992
  - $218M in sales in 2008
  - More than 500 employees
  - World-class foundry partners
  - #1 flash FPGA supplier
  - #1 antifuse FPGA supplier
  - ~35% of revenue from FPGAs screened for Mil / Aero applications

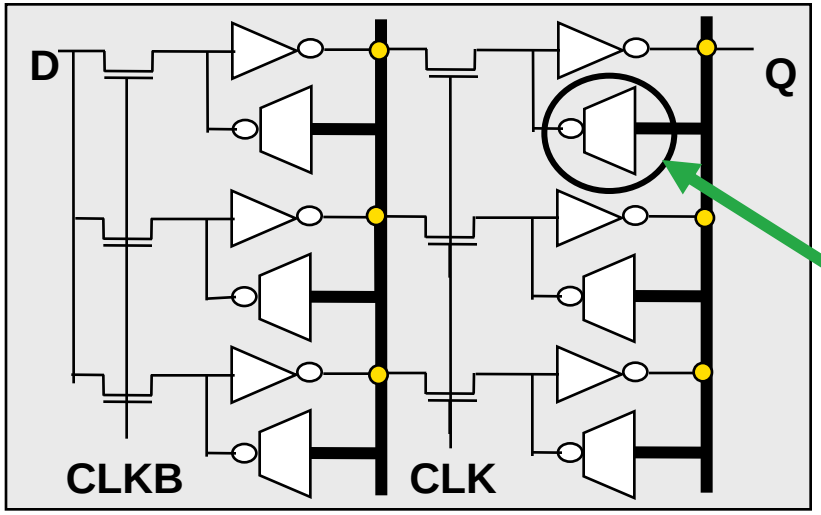
SEU-Enhanced Flip-Flops

- Foundation for RTSX-SU and RTAX family FPGAs

Standard Flip-flop



SEU-Enhanced Flip-flop



Actel Advantage

- 100% gate availability - no gate loss to TMR implementation
- Upsets due to single ion strike voted out by the unaffected latches
- Voting the feedback paths prevents the flip flop from changing state
- Transparent to user, no special skill or knowledge needed

Voter Gate

- Two correct inputs outvote single incorrect input
- Self-corrects asynchronously

Screening Flows for Space-Flight FPGAs

Mil-Std 883 class B	Extended Flow	QML-V / EV Flow
Screening Process	Screening Process	Screening Process
Wafer Sort	Wafer Sort	Wafer Sort
Package Assembly (B flow)	Package Assembly (E flow)	Package Assembly (EV flow)
Bond Pull (Sample Pull Test)	Bond Pull (Extended Pull Test)	Bond Pull (Extended Pull Test)
Internal Visual (cond.B)	Internal Visual (cond.A)	Internal Visual (cond.A)
Serialization (RT parts only)	Pre-Cap Source Insp. (cond.A)	Pre-Cap Source Insp. (cond.A)
Temperature Cycling (10 cycles)	Serialization	Serialization
Constant Acceleration	Temperature Cycling (10 cycles)	Temperature Cycling (50 cycles)
PIND	Constant Acceleration	Constant Acceleration
Seal (Fine/Gross Leak Test)	PIND	PIND
Electrical Test	Seal (Fine/Gross Leak Test)	Seal (Fine/Gross Leak Test)
Dynamic Burn-in (160hrs @ 125°C)	X-Ray	X-Ray
Post-BI Test +25°C	Electrical Test	Electrical Test
Final Test -55°C	Dynamic Burn-in (240hrs @ 125°C)	Dynamic Burn-in (240hrs @ 125°C)
Final Test +125°C	Post-BI Test +25°C with R&R	Post-BI Test +25°C with R&R
QA Electrical (Group A)	Static Burn-in (144hrs @ 125°C)	Static Burn-in (144hrs @ 125°C)
Mechanical Visual	Post-BI Test +25°C with R&R	Post-BI Test +25°C with R&R
	Final Test -55°C	Final Test -55°C with R&R
	Final Test +125°C	Final Test +125°C with R&R
	Seal (Fine/Gross Leak Test)	Seal (Fine/Gross Leak Test)
	QA Electrical (Group A)	QA Electrical (Group A)
	Mechanical Visual	Mechanical Visual
Lot Acceptance Tests	Lot Acceptance Tests	Lot Acceptance Tests
Generic Group B	Lot Specific Group B with RGA	Lot Specific Group B with RGA
Generic Group C	Generic Group C	Wafer Lot Specific Group C (2000 Hr HTOL)
Generic Group D	Generic Group D	Generic Group D
Generic Radiation Total Dose Report	Generic Radiation Total Dose Report	Generic Radiation Total Dose Report
		Lot Specific DPA (per Date Code)
		Data Package

RTSX-SU

RTSX-SU Family

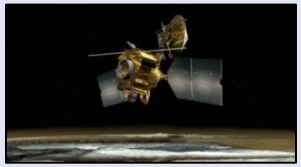
- RTSX-SU Features
  - Designed specifically for Space Applications
  - Up to 2,012 SEU Hardened Flip-Flops eliminate user-designed TMR
  - Single Event Latch-up Immune
  - Supports Hot-Swapping and Cold Sparing
  - Configurable I/O support multiple 5.0V and 3.3V I/O standards
  - Pin Compatible with commercial SX-A devices for easy prototyping

- QML Certified Devices
  - QML Class Q available today
    - Mil Std 883 Class B
    - Actel Extended flow
  - QML Class V submission planned for 2010
  - "EV" flow available today
    - All process steps of QML-V
    - 40-week lead time applies (2000 Hr Group C)

	RTSX32SU	RTSX72SU
Dedicated Registers	**1,080**	**2,012**
Total Modules	**2,880**	**6,036**
Max User I/Os	**227**	**360**
Packages	**84-CQFP** **208-CQFP** **256-CQFP** **256-CCLG**	**208-CQFP** **256-CQFP** **624-CCGA/LGA**
Manufacturing Process Flows	**883B** **E-Flow** **EV-Flow** ***QML-V coming soon***	

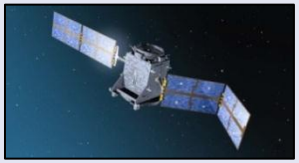
Success in Space – RTSX-SU

Mars Reconnaissance Orbiter Launched August 2005

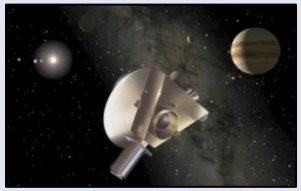


GPS 2R-M (8 Satellites) Launched Sept 2005 to August 2009

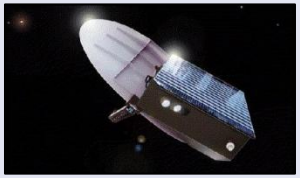
Galileo GIOVE-A and GIOVE-B Launched Dec 2005 and April 2008



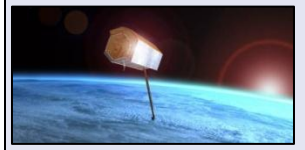
New Horizons Launched Jan 2006



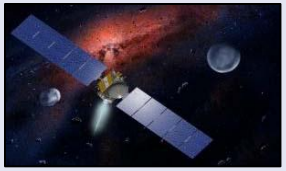
SAR-Lupe 1 and SAR-Lupe 2 First Launch Dec 2006



TerraSar X Launched June 2007

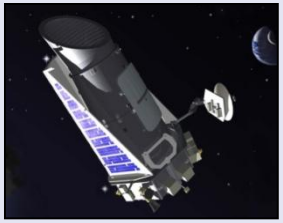


Dawn Launched Sept 2007

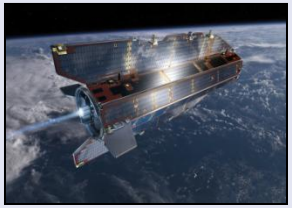


GLAST Launched June 2008

Kepler Launched March 2009

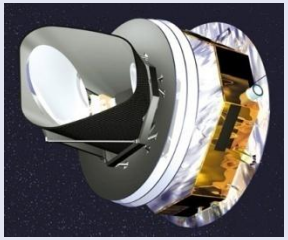


GOCE Launched March 2009



Herschel Launched May 2009

Planck Launched May 2009



RTAX-S
Designed for Space

RTAX-S/SL

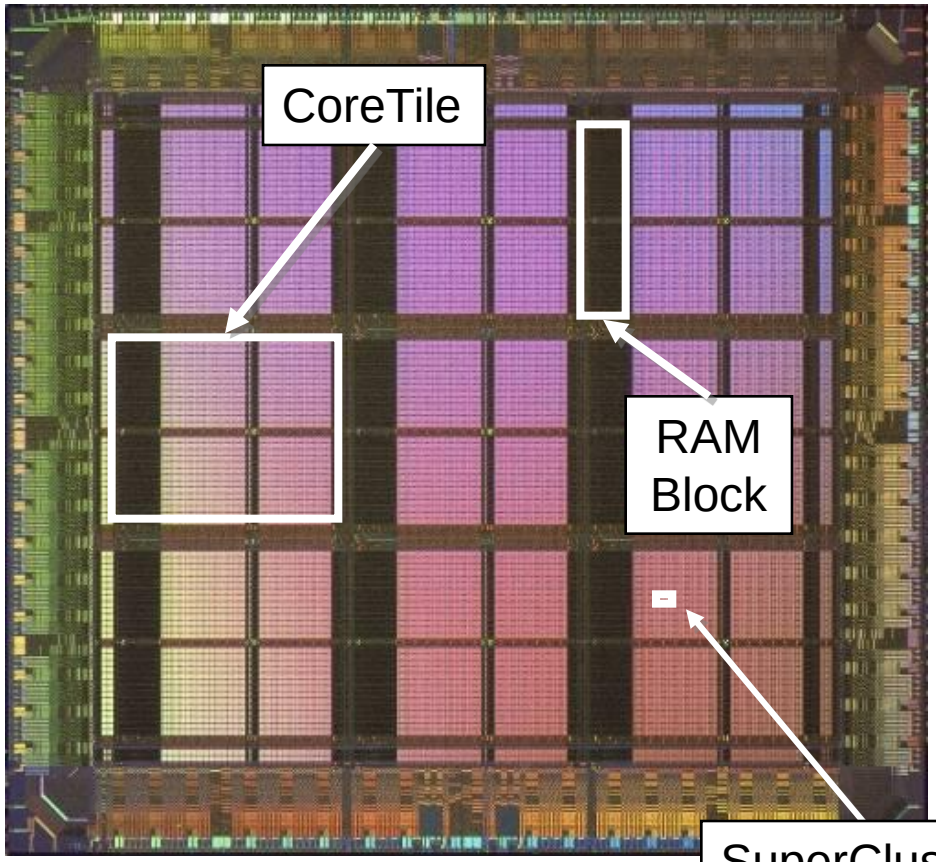
- Radiation-tolerant FPGA alternative to RH ASICs
  - Ten times larger than previous largest space FPGA
    - Up to 4M system gates – approximately 500,000 ASIC gates
  - Designed for space — Single Event Upset (SEU) enhancements
  - 0.15µm, 7-layer metal CMOS with Antifuse, manufactured at UMC
  - Embedded block RAM
  - Multiple Flexible I/O standards
  - Live at Power-up (LAPU)
  - Single chip
  - Low power consumption
- New developments
  - RTAX250S/SL in CG/LG624 package
  - RTAX4000SL low power version
  - RTAX4000S/SL in Dash-1 speed grade
  - Absolute Max T_J raised to 135 C

RTAX-S/SL FPGA Family

	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL
Dedicated Registers	1,408	6,048	10,752	20,160
I/O Registers	744	1,548	2,052	2,520
Total Modules	4,224	18,144	32,256	60,480
RAM Blocks	12	36	64	120
Total RAM Bits	54K	162K	288K	540K
Max User I/Os	248	516	684	840
Packages	208-CQFP 352-CQFP 624-CCGA/LGA	352-CQFP 624-CCGA/LGA	256-CQFP 352-CQFP 624-CCGA/LGA 1152-CCGA/LGA	352-CQFP 1272-CCGA/LGA
Status	***QUALIFIED SILICON NOW SHIPPING!***			

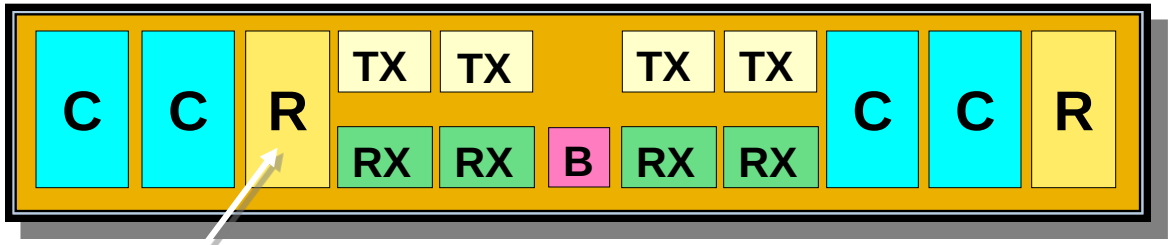
- Typical lead times:
  - 18 weeks B-flow, 50 units, CQFP or LGA packaging
  - 24 weeks E-flow, 50 units, CQFP or LGA packaging
  - 40 weeks EV-flow, 20 units, CQFP or LGA packaging (2000 Hr Group C life test)
  - CCGA takes 6 to 8 weeks longer to process
  - Preparation of export documentation may add additional lead time

RTAX-S Device Architecture

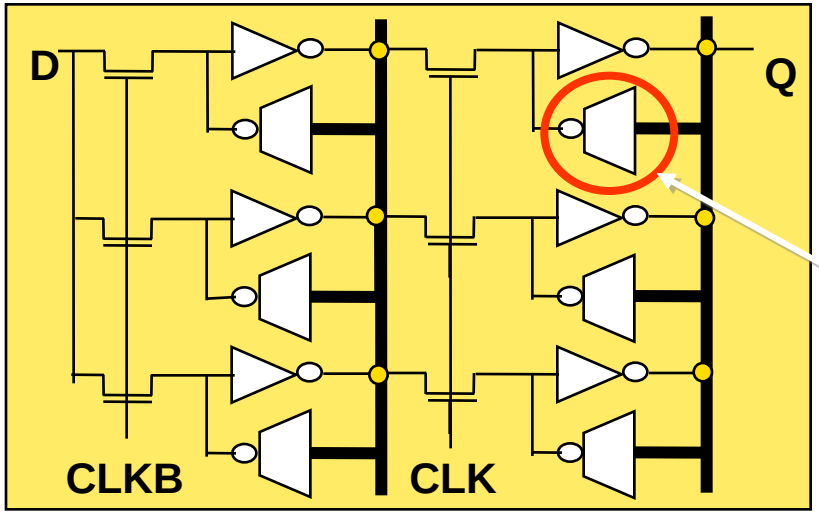


- Built using Core Tiles
  - RTAX1000S – 3x3 Core Tiles
    RTAX2000S – 4x4 Core Tiles
    RTAX4000S – 6x5 Core Tiles
  - Each Core Tile has:
    - 336 SuperClusters
    - 4 Blocks of RAM
  - RTAX250S – 2x2 Mini Core Tiles
  - Each Mini Core Tile has:
    - 176 SuperClusters
    - 3 Blocks of RAM

RTAX-S SuperCluster



SEU Enhanced Flip-Flop in R Cell



Voter Gate

- **Two correct inputs outvote single incorrect (radiation upset) input**
- **Self-corrects asynchronously**

RTAX-S Radiation Data

- Single-event Latch-up (SEL)
  - Testing performed up to LET 117 MeV-cm$^{2/}$mg (125ºC)
  - No SEL observed; No control logic upset observed
- R-Cell Single-event Upset (SEU)
  - LET_{TH} in excess of 37 MeV-cm^2/mg
  - Cross-section < 1E^{-9} cm^2
  - SEU per R-Cell < 4E^{-11} Errors/bit-day (worst case GEO)
- Memory SEU
  - SEU < 1E^{-10} upsets/bit-day (worst case GEO)
    - EDAC operational, background scrubbing at 2MHz
- Single-event Transient (SET)
  - High frequency testing to 150 MHz with NASA GSFC
  - Additional testing and analysis reported at Actel Space Forum www.actel.com/asf
- Total Ionizing Dose (TID)
  - Results indicate suitability for vast majority of space missions
    - Stays within parametric limits beyond 200Krads (si)
    - No functional failure up to 300Krads (si)
  - TID performed on each production wafer lot

All reports posted to http://www.actel.com/products/milaero/hireldata.aspx

RT Timing Improvements

- RTAX-S TID timing derating – BIG IMPROVEMENT!
  - Improvement based on accumulation of TID test data over 25 wafer lots

TID	Old Derating	New Derating	Improvement
100Krad	10%	3%	7%
200Krad	20%	4.5%	16%
300Krad	30%	6%	24%

  - Implemented in Actel Designer / Libero® Integrated Design Environment (IDE) software v8.3 (March 2008)
  - Current datasheet has updated timing numbers

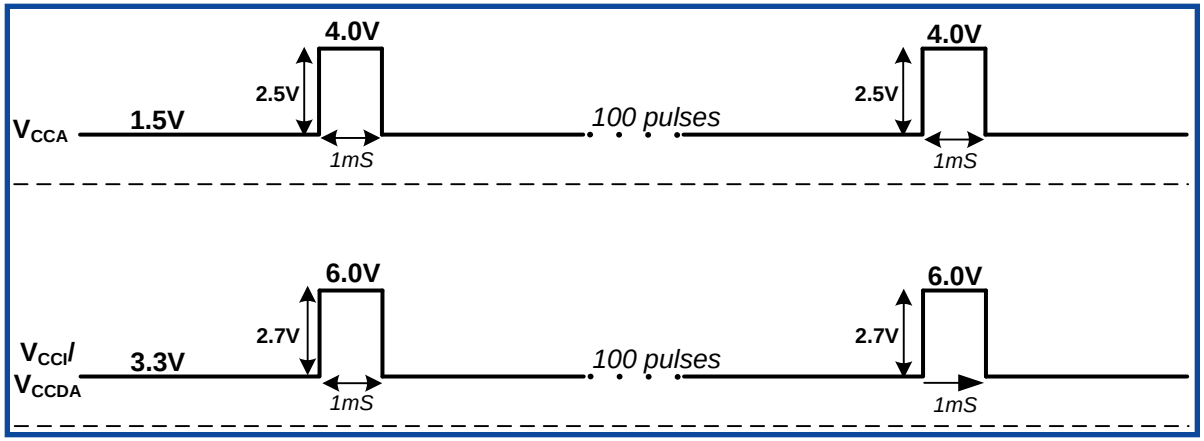
- Enhanced place-and-route results in improved timing for SRAM designs
  - Implemented in Actel Designer / Libero® Integrated Design Environment (IDE) software v8.5 SP1 (February 2009)
  - RTAX250S/SL, RTAX1000S/SL, RTAX2000S/SL
    - 5% average improvement
  - RTAX4000S/SL
    - 15% average improvement

RTAX-S Reliability Enhancements

- XY Wafer Location Programming
  - Wafer number and die location programmed into each unit during wafer sort
    - Assists with traceability and failure analysis
- Programming Software Revision Stamping
  - Silicon Sculptor Programming SW revision is programmed into device concurrent with customer design programming
    - Assists with traceability and failure analysis
- Thermal Runaway Characterization
  - Performed on each wafer lot (started with lots fabricated in 2007)
  - Two samples are programmed with ELA design and current is measured at junction temperature T_J of 140 C, 145 C, and 150 C
  - Lots exhibiting thermal runaway at T_J 150 C or lower are scrapped
  - Recommended maximum junction temperature T_J = 125 C
  - Absolute maximum junction temperature T_J = **135 C**

Power Supply Transient Testing (1)

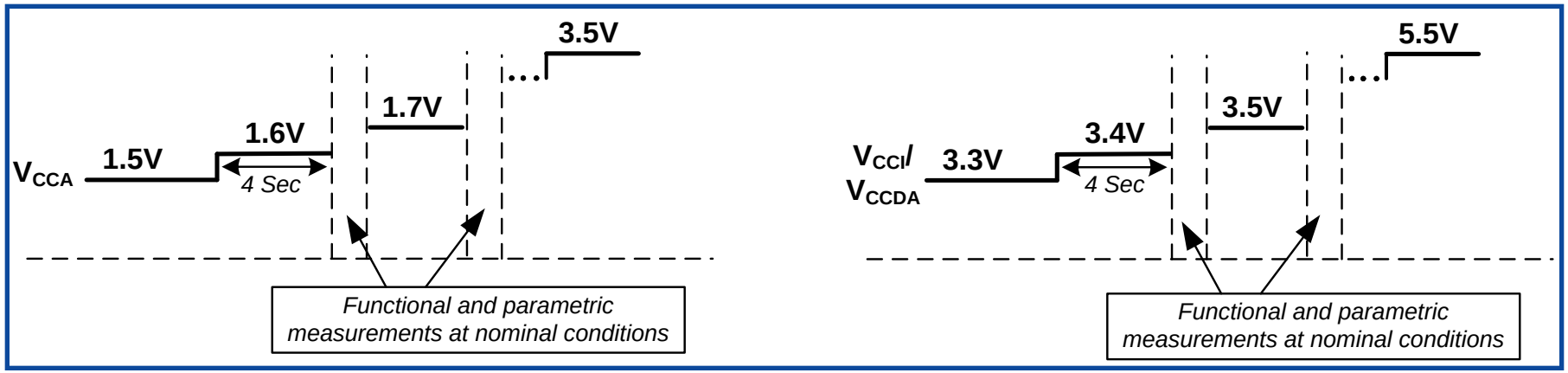
- RH regulators can sometimes exhibit Single Event Transient effects
  - Output voltage glitches to levels close to the unregulated supply voltage
  - Potential hazard for all devices powered by regulators
- Pulse testing of power supply transients on Actel FPGAs
  - Devices exposed to ~100 pulses of 1msec duration while operating
    - RTAX-S – 26 devices / 2 lots
      - Pulse amplitude 2.5V above nominal 1.5V V_{CCA}, 4.0V total
      - Pulse amplitude 2.7V above nominal 3.3V V_{CCI}, 6.0V total
      - No damage observed, devices sampled from three wafer lots
    - RTSX-SU – 27 devices / 3 lots
      - Pulse amplitude 3.0V above nominal 2.5V V_{CCA}, 5.5V total
      - Pulse amplitude 2.5V above nominal 5.0V V_{CCI}, 7.5V total
      - No damage observed, devices sampled from three wafer lots



RTAX-S Limits Shown

Power Supply Transient Testing (2)

- Static testing of power supply transients on Actel FPGAs
  - Devices exposed to increased V_{CC} levels for several seconds while operating
    - RTAX-S
      - No damage was observed until 3.5V above nominal 1.5V V_{CCA} ,5.0V total
      - No damage was observed at levels up to 2.2V above nominal 3.3V V_{CCI}, 5.85 total
    - RTSX-SU
      - No damage was observed at levels up to 2.0V above nominal 2.5V V_{CCA}, 4.5V total
      - No damage was observed at levels up to 1.5V above nominal 5.0V V_{CCI}, 6.5V total
- 1000 Hr HTOL confirmed no long-term reliability effects
- Detailed report is available from Actel
- Datasheet limits remain unchanged

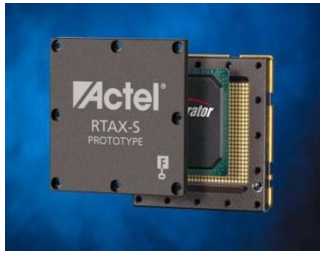


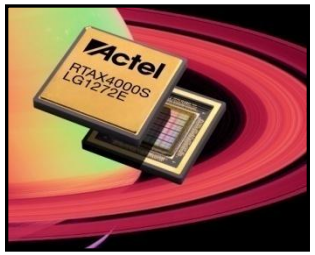
RTAX-S Limits Shown

RTAX-SL Low Power Family

- New family
  - Reduced stand-by current
  - New part numbers
    - SMDs have been updated with new part numbers
  - RTAX250SL, RTAX1000SL, RTAX2000SL and now RTAX4000SL
- Stand-by current spec
  - Reduced by 70% to 80% relative to standard RTAX-S (worst case conditions)
    - For example RTAX2000SL spec is 150mA at 125 C
  - Dynamic current spec is unchanged
  - Device timing is unchanged
- Schedule
  - Open for orders NOW
    - Usual lead times will apply

Complete Development Solutions





Actel RTAX-S Prototyping Solutions

Reprogammable Solution Using APA/A3P with ALDEC Adapter	Sockets and Adapter Sockets for using Commercial Devices	Prototype Using Commercial AX Product in Ceramic Package	RTAX-S Proto Units – Mil Temp Tested, No 883B Processing	RTAX-S Production Units – QML Class Q or Class V

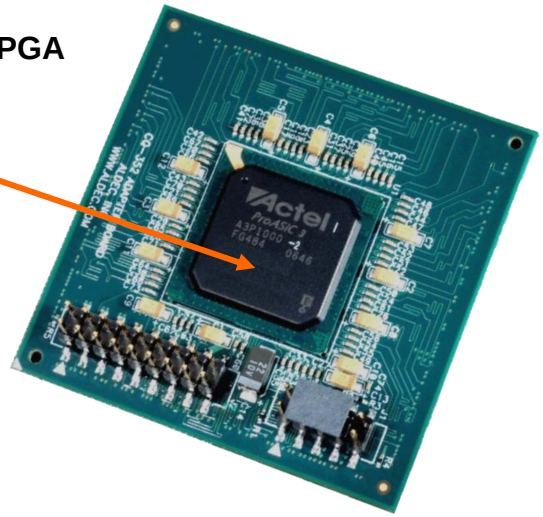
Phase 1: Concept Validation	Phase 2: Demonstration Hardware	Phase 3: Test Hardware using flight boards	Phase 4: Final Flight Hardware

Typical Design Phases

Reprogrammable Prototyping: ALDEC Adaptor

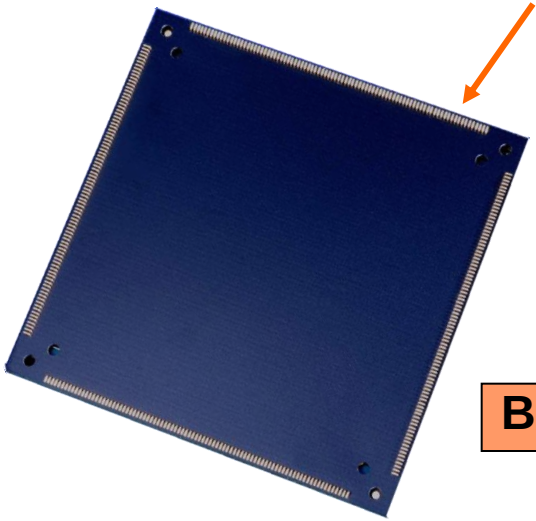
- Footprint-compatible with the RTAX-S/SL space-flight FPGA
  - CQ208, CQ256, CQ352 and CG624 footprints
- JTAG programming connector (JTAG) on the adaptor board
  - Reprogram the device on-the-fly on the target PCB
- EDIF Netlist converter ports from RTAX-S/SL to ProASIC3
  - Primitives and memories
  - Automatic pin remapping

Actel ProASIC3/3E FPGA A3P1000-FG484, A3PE1500-FG484, or A3PE3000-FG484



Top View

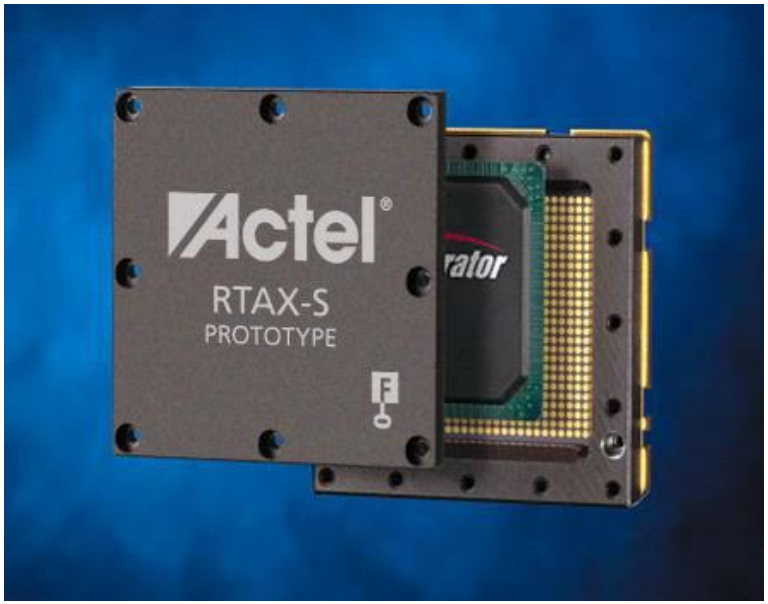
Leads that mimic CQ352 package



Bottom View

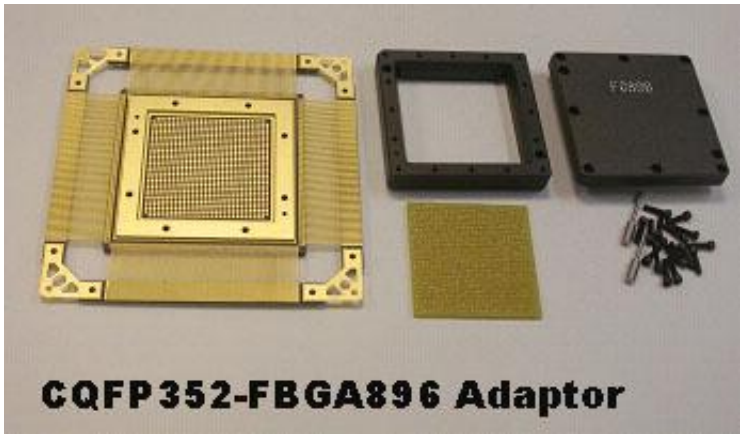
RTAX-S Prototyping with Actel Axcelerator

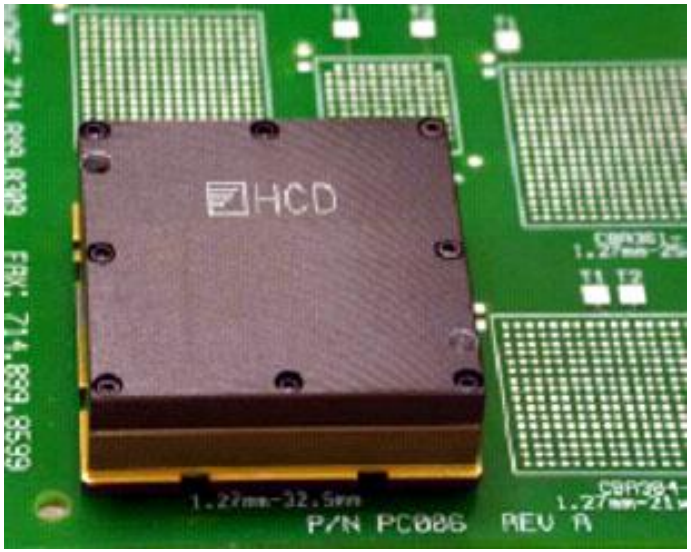
- Low Cost Prototyping solution available *NOW!*
  - Allows design activity to start immediately
  - Uses commercial Axcelerator (AX) silicon in FG896 package for functional verification
  - FG896 – CQ352 adaptor
    - Matches CQ352 PCB footprint
  - FG896 – CG624 adaptor
    - Matches CG624 PCB footprint
  - FG896 – CQ256 adaptor
    - Matches CQ256 PCB footprint, for RTAX2000S-CQ256
  - CQ208 can be prototyped with commercial PQ208 AX FPGAs
  - CG1152 can be prototyped with commercial FG1152 AX FPGAs



RTAX-S Low Cost Prototyping Solutions

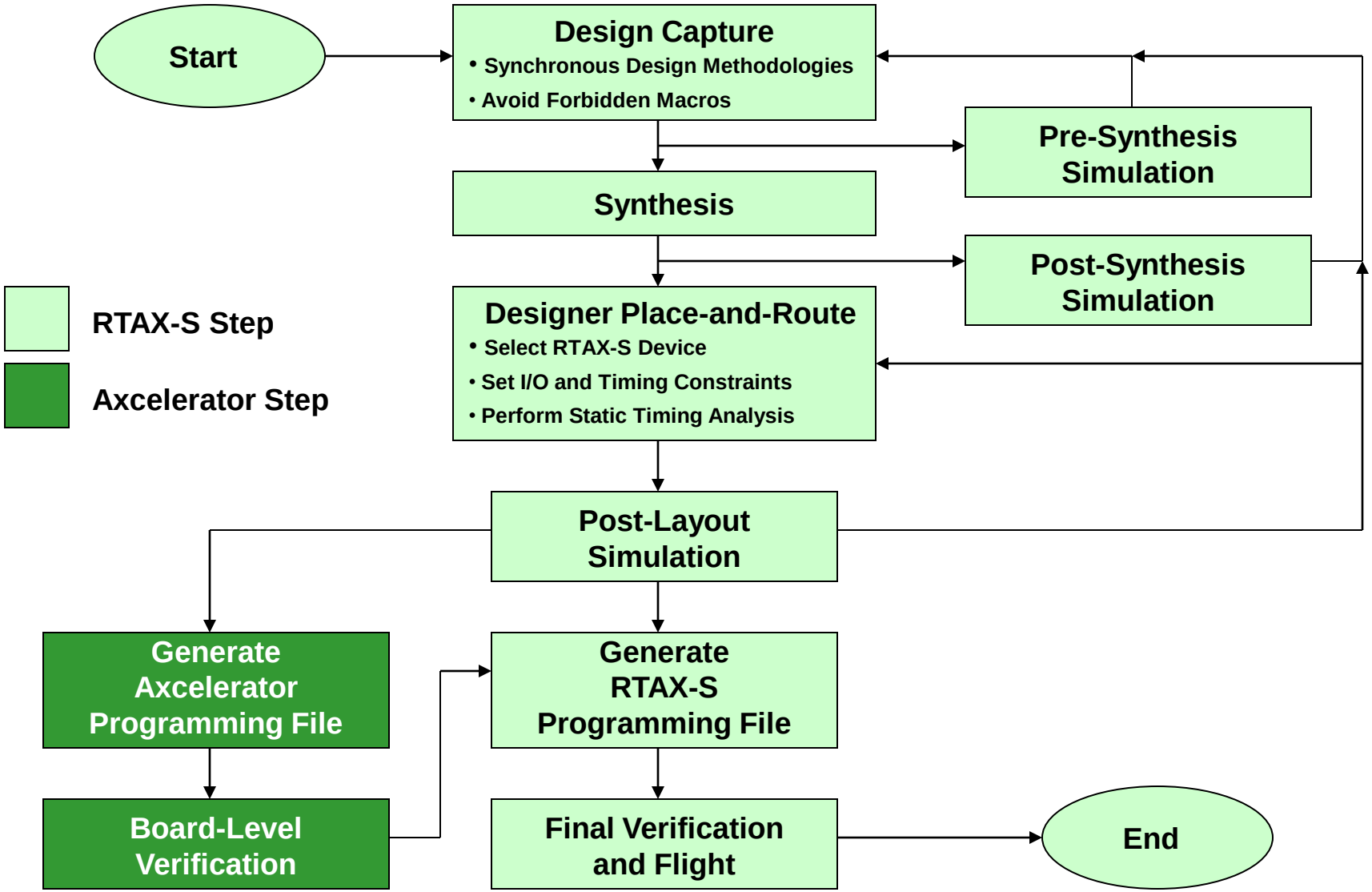
- Low cost prototyping solution
- CCGA and CQFP footprints available
- CCGA adaptor uses solder balls (not columns)
  - Eliminates costly column attach
  - Requires no re-layout





Fully Assembled CCGA 624-FBGA896 Adaptor

RTAX-S Prototyping Flow

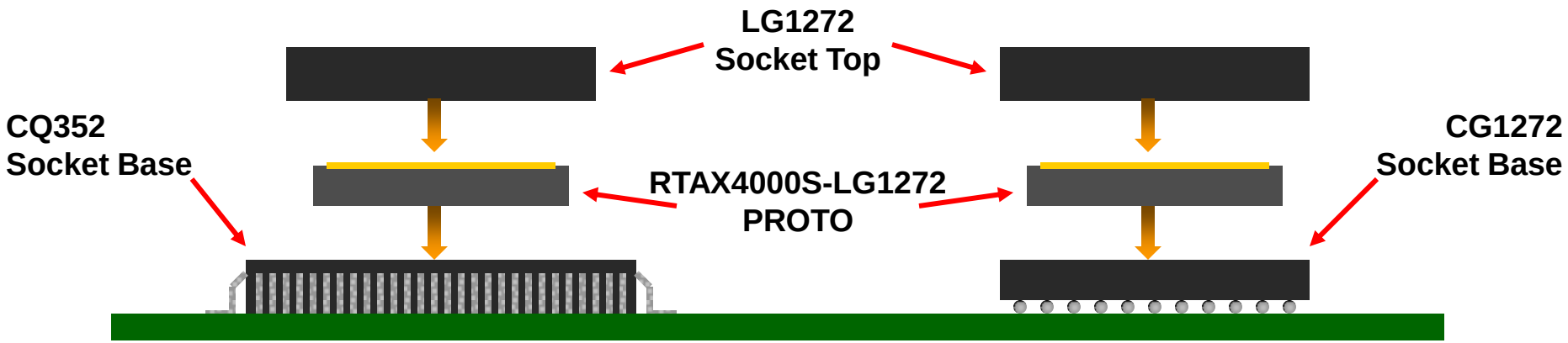


Final Verification with RT Silicon

- Introducing low-cost RT devices for final timing verification
- RT-proto FPGAs
  - RTSX-SU and RTAX-S prototypes
  - RT die, in cost-reduced packages
    - Identical timing and functionality to space-flight RTSX-SU and RTAX-S FPGAs
    - Military temperature testing
    - No Mil-Std 883B processing
    - Non-hermetic lids
    - Lid dimpled to deter counterfeiting
    - *Not suitable for space-flight* devices marked to indicate this
    - *Not intended for qualification of space-flight hardware*
  - Open for orders NOW
  - Shipments NOW (lead time applies)

RTAX4000S Proto Socket

- Enhanced prototyping for RTAX4000S
  - Today's only solution is to use RTAX4000S-PROTO
    - Great for late prototyping and final timing verification
    - Not so good for early prototyping
      - Successive design changes require PROTO part to be desoldered and a replacement PROTO part to be soldered to target board
      - Jeopardizes integrity of board, populated with very expensive RT parts
  - Actel now offers a socket to permit easy replacement of RTAX4000S-PROTO devices during early prototyping



RTAX-S
Qualification Update

RTAX-S Qualification

- Mil-Std 883B Qualification Completed June 2005
  - DSCC released and certified QML-Q SMDs April 2006
    - RTAX-S devices can be ordered to the DSCC SMD “5962” number
- QML Class V Qualification in Progress
  - RTAX4000S is qualification vehicle
  - Completed 6000 hours Group C HTOL Oct 2008, 75 units, no silicon failures
  - One packaging anomaly related to gross leak test
  - Hoping for full QML-V certification 2010
- Enhanced Antifuse Qualification (EAQ)
  - Uses design with high observability of timing changes
    - Detects weak or misformed antifuses, learned from MEC RTSX-S investigation
  - 120 units RTAX1000S-CG624 tested
    - 6000 hours HTOL completed
    - 250 hours LTOL completed
- Additional Engineering Testing
  - HTOL – 1000 Hrs, 125ºC, 173 units
  - LTOL – 1000 Hrs, -55ºC, 77 units
- No antifuse failures observed in testing to date
  - Overall product FIT rate calculated < 11 FIT (60% confidence level, EA = 0.7eV)

RTAX-S Independent Reliability Testing

- Aerospace Corporation testing (AX)
  - Running since 2007
  - Some parts > 21,000 hours HTOL
  - > 14M device-hours so far
  - One failure (SRAM) under investigation: suspect contact processing issue (these are not Mil-Std 883B parts)
  - No antifuse anomalies

		Devices	Device-Hours
AX2000	HTOL	277	5,733,534
AX2000	LTOL	274	4,835,585
AX2000	TC	189	3,453,520
	Total		14,022,639

- NASA GSFC
  - Testing completed July 2009
  - 6,000 hours total per device
  - Almost 1M device-hours
  - No anomalies

		Hours	Devices	Device-Hours
RTAX250S	HTOL	3,000	82	246,000
RTAX250S	LTOL	3,000	82	246,000
RTAX2000S	HTOL	3,000	82	246,000
RTAX2000S	LTOL	3,000	82	246,000
	Total			984,000

Actel RTAX-S Class V Plan

- Seeking QML-V certification
  - Certifying authorities have started certification activities
  - Hoping for QML class V certification in 2010
- Class V process flow has been established (“EV”)
  - Complies with current rev of MIL-PRF-38535 (Rev H)
    - Wafer lot specific Group C life test
    - 100% Pre-Cap Source Inspection
    - Lot-specific DPA
    - Tri-temp read and record pre- and post-burn-in
- “EV” class V flow available NOW!
  - Prior to official class V certification
  - Expect no silicon or process differences between Actel “EV” and official QML class V devices
  - Open for order entry NOW
  - NOTE: Actel has no plans to discontinue existing B-flow or E-flow

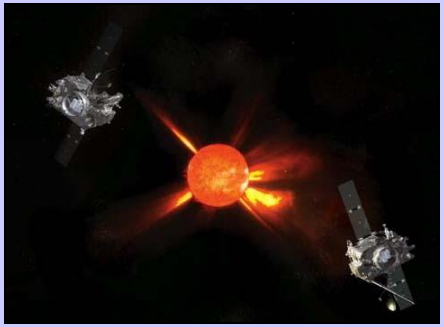
IP for Space Applications

- Gaisler Leon3-FT
  - Building flight and design-in heritage
    - SIR-2 (Norway) on Chandrayaan-1(India) – ***IN FLIGHT***
    - Argo (Taiwan)
    - Prisma (Sweden)
    - Bepi Colombo (ESA)
    - MMS (USA)
    - Orbcomm (USA)
    - RBSP (USA)
    - Tacsat-4 (USA)
  - 32-bit, SEE immune, 25 DMIPs at 25 MHz in RTAX-S
- Gaisler Spacewire
  - 100Mb/sec or higher in RTAX-S across T and V range
- Actel Mil-Std 1553B
  - Bus Controller (BC), Remote Terminal (RT), Monitor Terminal (MT)
  - Can be supplied as netlist or as RTL
  - Includes full test bench
  - Certified per RT valiation test plan Mil-Hdbk-1553 Appendix A

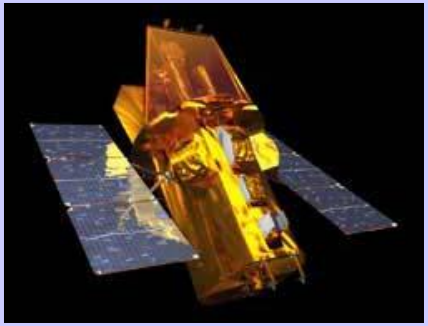
Flight Heritage – IP Cores

EFA Typhoon
First Production Aircraft 2002
PCI

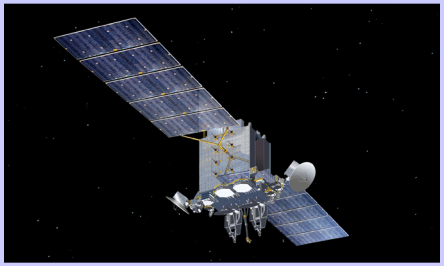
STEREO
Launched 2006
PCI



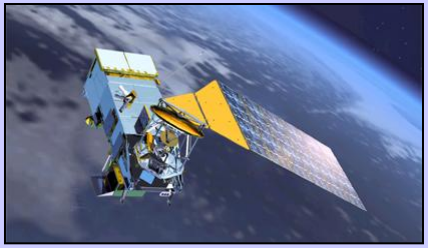
SWIFT / MIDEX
Launched 2004
PCI



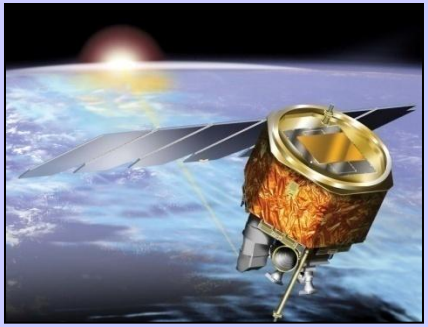
Advanced EHF
First Launch Expected 2010
PCI



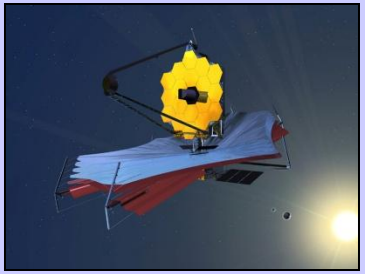
NPOESS
First Launch Expected 2014
PCI



SOFIE / AIM
Launched 2007
Mil Std 1553

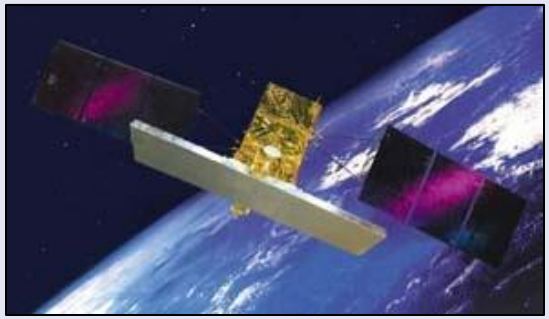


James Webb
Space Telescope
Launch Expected 2013
Mil Std 1553



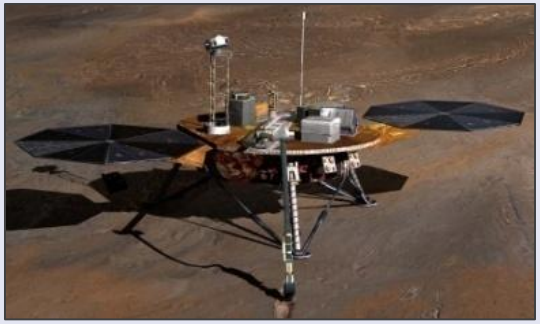
RTAX-S Now in Space!

Cosmo-SkyMed 1, 2, and 3
First Launch June 2007



RTAX2000S-CQ352

Mars Phoenix
Launched August 2007

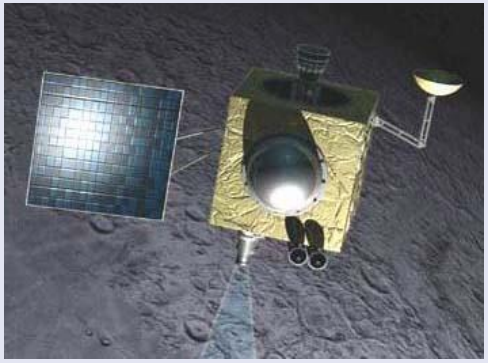


RTAX1000S-CQ352

TWSAT
Launched April 2008

RTAX2000S-CQ352

Chandrayaan-1
Launched October 2008

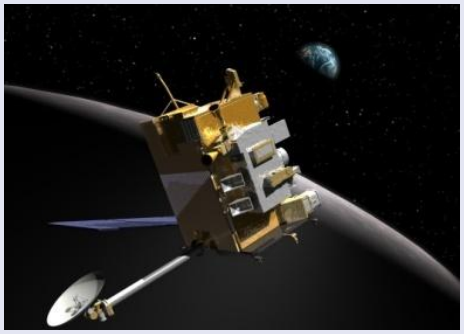


RTAX2000S-CQ352

Sicral-1B
Launched April 2009

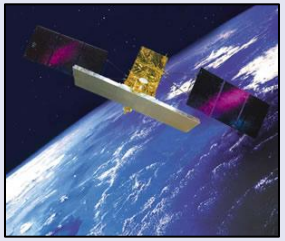
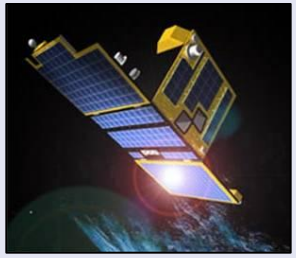
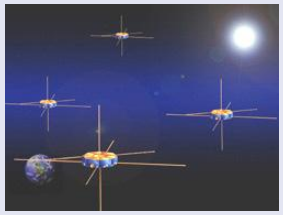
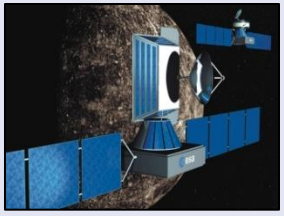
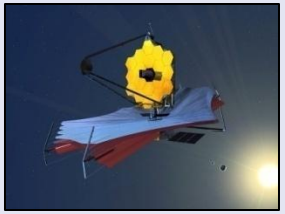
RTAX2000S-CQ352

LRO & LCROSS
Launched June 2009



RTAX2000S-CG624
RTAX2000S-CQ352

Planning to Fly RTAX-S

Galileo  *CQ352*	**Advanced EHF**  *CQ352*	**NPOESS**  *CG1152 - 6Σ*	**MUOS**  *CG624 - BAE*	**GOES-R**  *CQ352* *CG624 - BAE*	**COSMO SkyMed 4**  *CQ352*
Proba 2  *CG624 - 6Σ* *CG624 - BAE*	**Magneto-spheric MultiScale**  *CQ208* *CQ352* *CG624 - 6Σ*	**Mars Science Lab**  *CG624 - 6Σ*	**Bepi Colombo**  *CQ208* *CQ256* *CQ352*	**Gaia**  *CG624 - 6Σ* *CG1152 - 6Σ*	**James Webb Space Telescope**  *CQ352*

Introducing RTAX-DSP

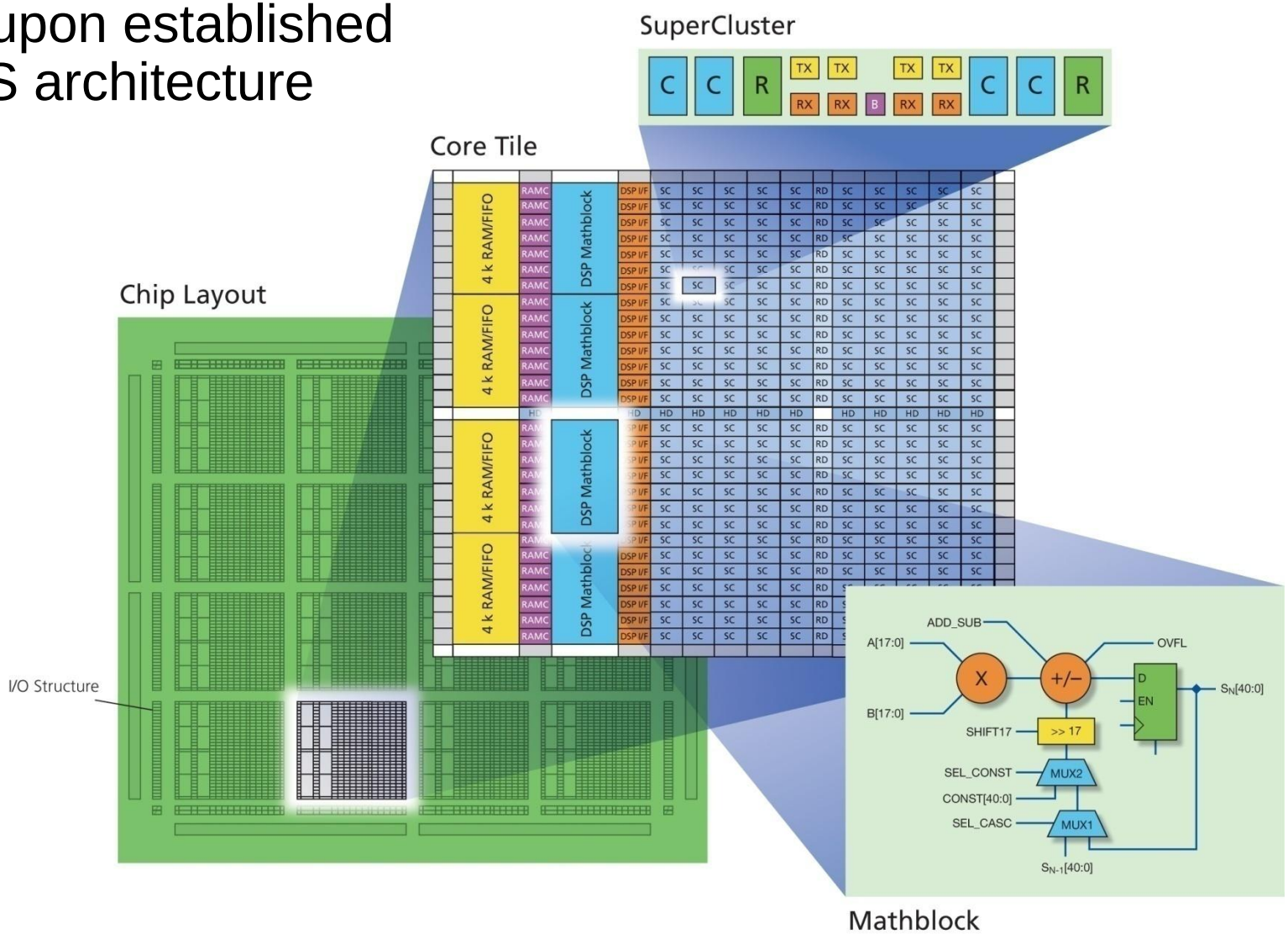
Industry's Most Reliable Space FPGAs Add Sophisticated DSP Capabilities

RTAX-DSP – Fast DSP Without Sacrificing Reliability

- High performance DSP
  - RTAX-DSP Mathblocks run 18bit x 18bit multiply-accumulate at 125MHz over full military temperature range (-55 C to 125 C)
- True radiation tolerance
  - Configuration is not upset or changed by heavy ion radiation
  - DSP blocks protected against heavy ion radiation effects
- Lower power
  - Fewer parts to get the job done means lower power consumption
- Proven reliability
  - RTAX-DSP uses same 0.15µm UMC process, same antifuse programming technology, same basic architecture as RTAX-S/SL
  - Reliability and radiation characteristics expected to be identical
- No cost or schedule risk
  - No ASIC tooling charge
    (or repeat charge, if design changes are made)

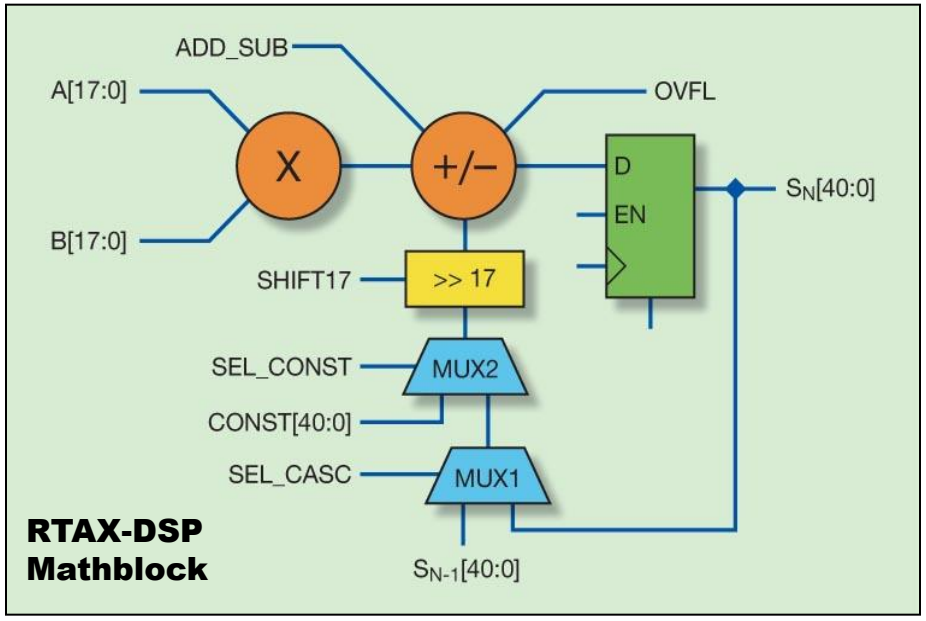
RTAX-DSP Architecture Overview

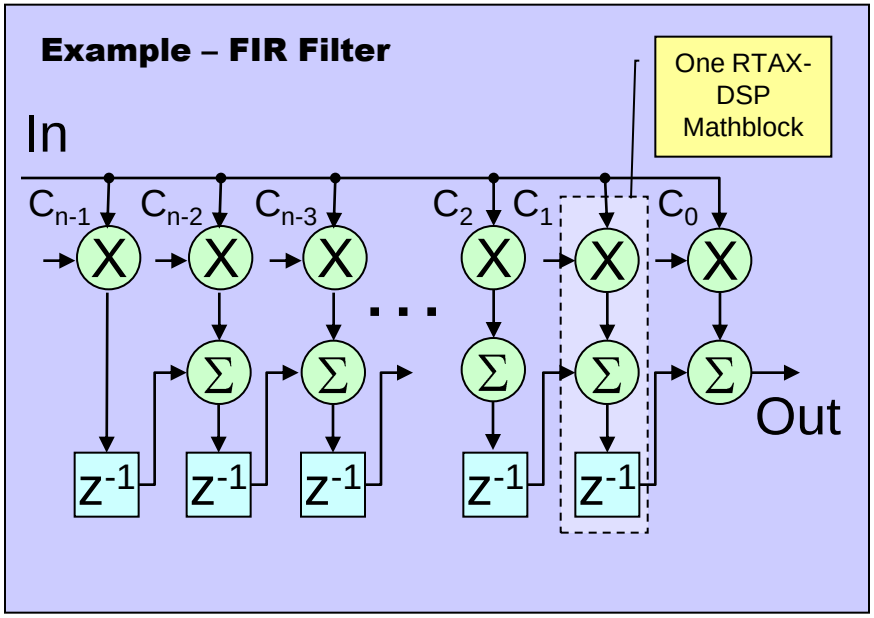
Builds upon established RTAX-S architecture



RTAX-DSP Mathblocks

- Flexible, Cascadable, High-Performance Structure
  - 18bit X 18bit multiplier
    - Can be fractured into two 9bit X 9bit multipliers
  - Add / subtract accumulate function
    - Combine the current multiplication product with a prior product, a constant, or with the result from another multiplier
    - Important in FIR, IIR digital filters and FFT





RTAX-DSP Highlights

- High Signal Processing Throughput
  - Up to 120 Mathblocks per device; 125 MHz operation, even at 125 C
  - 15 Billion multiply-accumulates / second (15 GMAC)
- Built-in Radiation Hardening in Mathblock
  - Single Event Transient (SET) protection in combinatorial logic
  - Single Event Upset (SEU) protection in sequential logic
- Availability
  - Software available NOW
  - Prototype units available NOW (RTAX4000D-CQ352)
  - Qualification complete 2H2010 (B, E, EV)

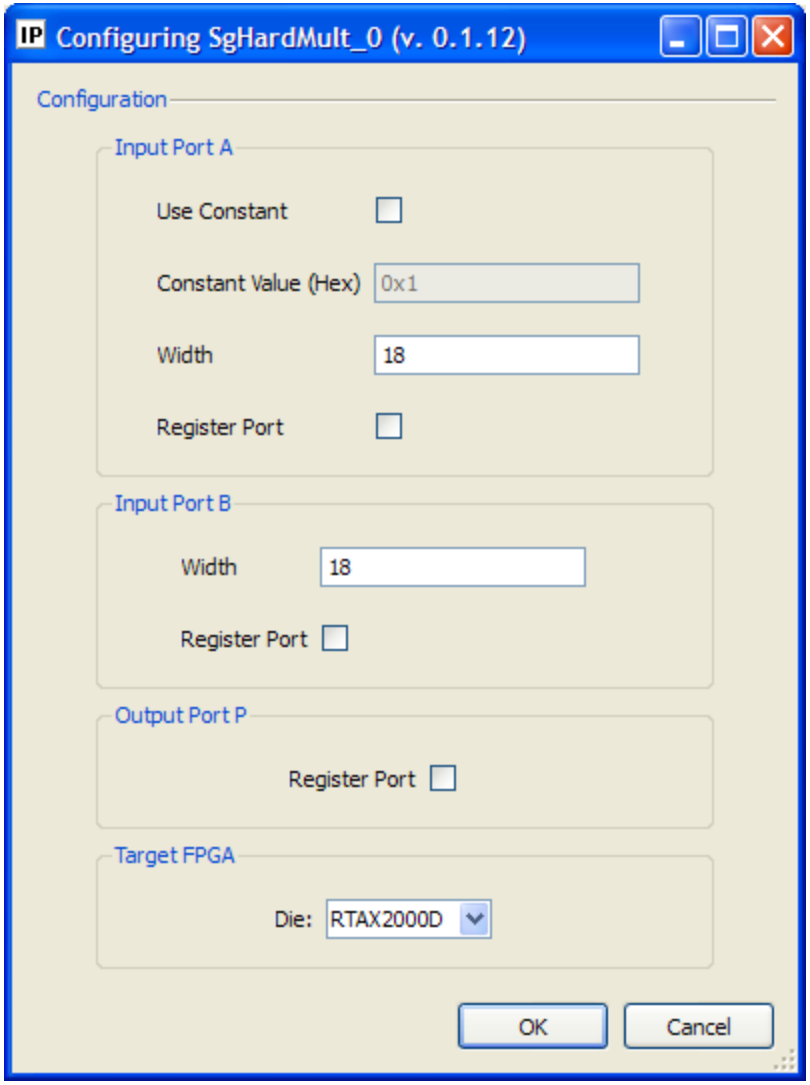
	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX2000D	RTAX4000S/SL	RTAX4000D
System Gates	250k	1M	2M	2M	4M	4M
Dedicated Registers	1,408	6,048	10,752	9,856	20,160	18,480
Total RAM Bits	54K	162K	288K	288K	540K	540K
DSP Mathblocks				64		120
Clocks	8	8	8	8	8	8
Maximum I/O	248	516	684	684	840	840
Packages						
CQFP	208, 352	352	352	352	352	352
CCGA / LGA	624	624	624, 1152	1272	1272	1272

IP and Tools

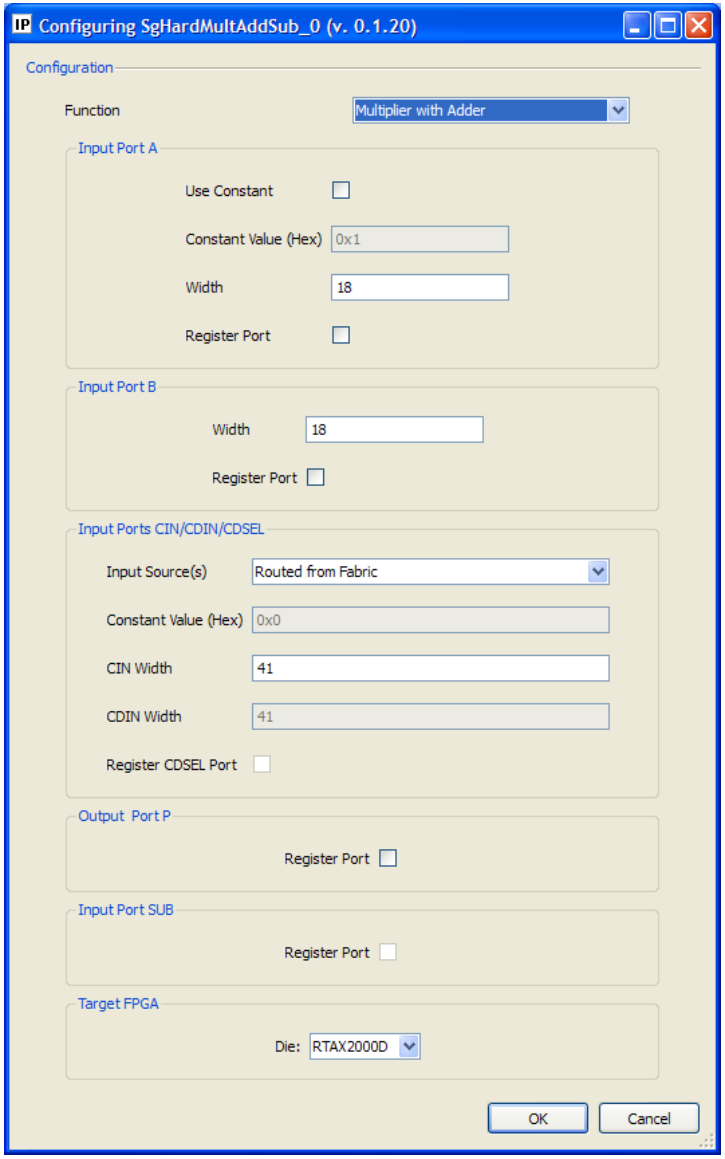
- Smart Gen Mathblock configurator
  - User interface allowing precise configuration of Mathblock
  - Mathblock macro IP cores available now
    - Multiply, Multiply and Add / Subtract, Multiply and Accumulate
- RTAX-DSP Actel IP
  - CoreFIR 4.0 for RTAX-DSP available now
    - Parameterizable single rate fully enumerated FIR filter
    - SmartDesign RTL generator using on-chip math blocks
  - CoreFFT 4.0 Radix-2 Fast Fourier Tranform will be next
  - Additional DSP cores to follow

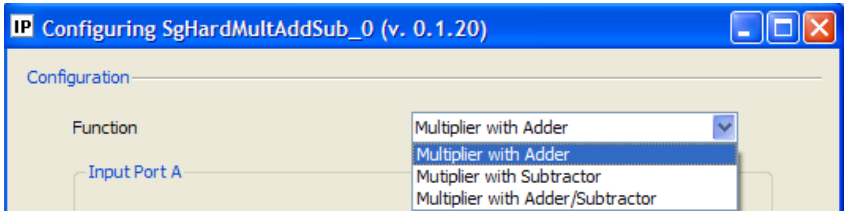
IP Type	Schedule
Fully enumerated FIR filter	NOW
Radix-2 FFT	1Q2010
Folded FIR filter	3Q2010
Interpolation polyphase FIR filter	4Q2010
Decimation polyphase FIR filter	1Q2011

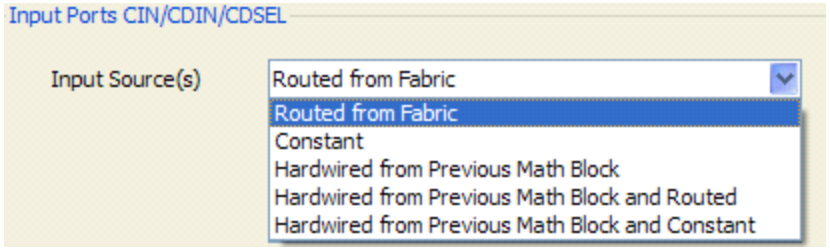
SmartGen Configuration 1 SgHardMult



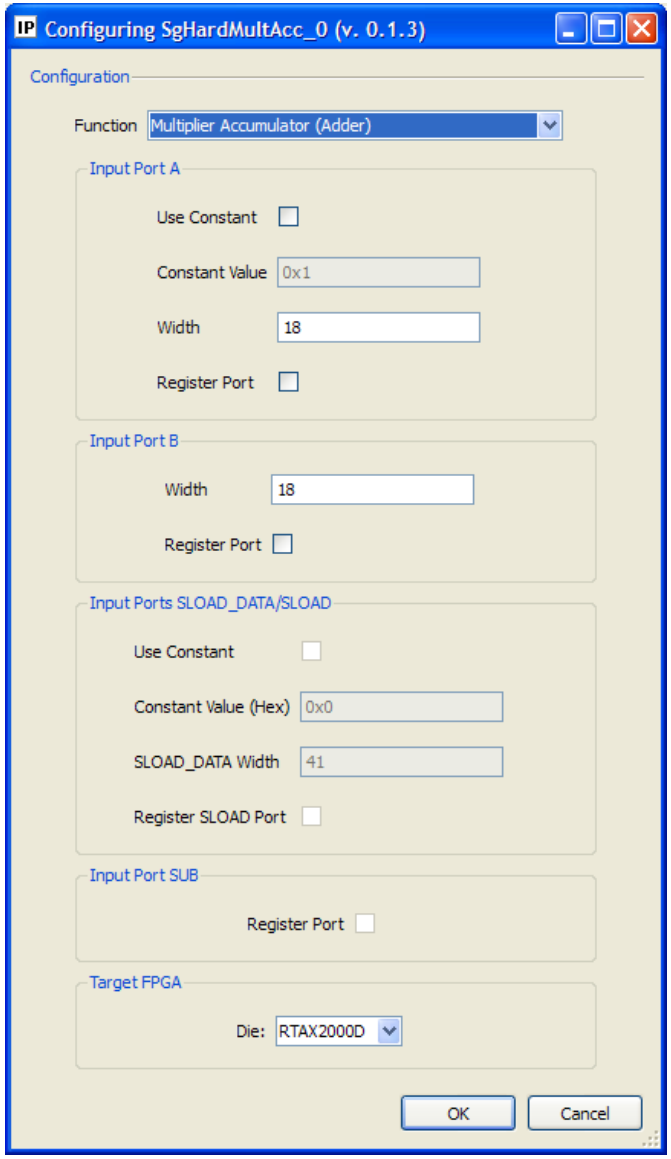
SmartGen Configuration 2 SgHardMultAddSub

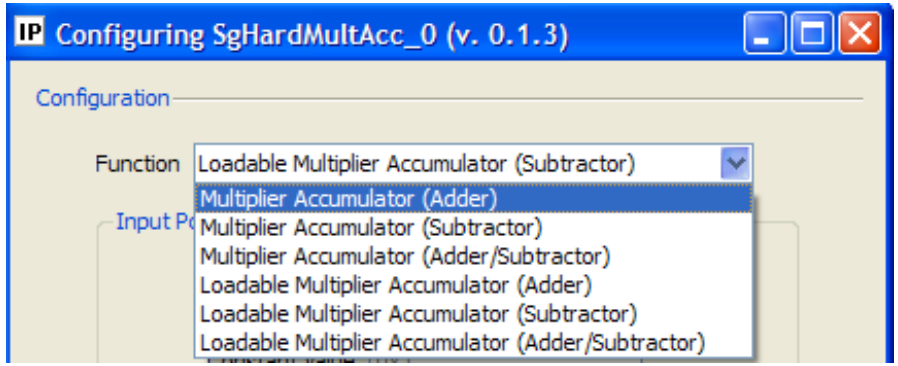






SmartGen Configuration 3 SgHardMultAcc





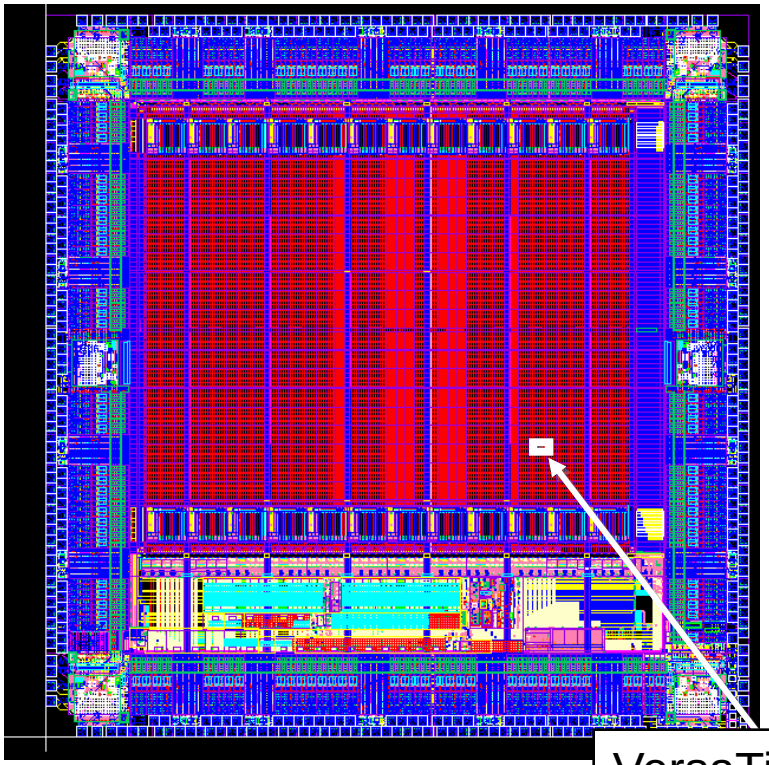
Introducing RT ProASIC3: Flash FPGAs for Space

Reprogrammable RT ProASIC®3 Devices Simplify Design of Space Systems

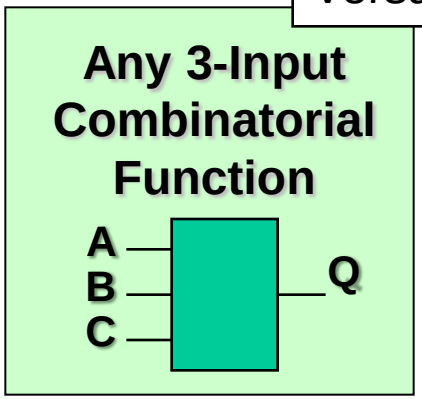
Low Power, Reprogrammable Space-Flight FPGAs

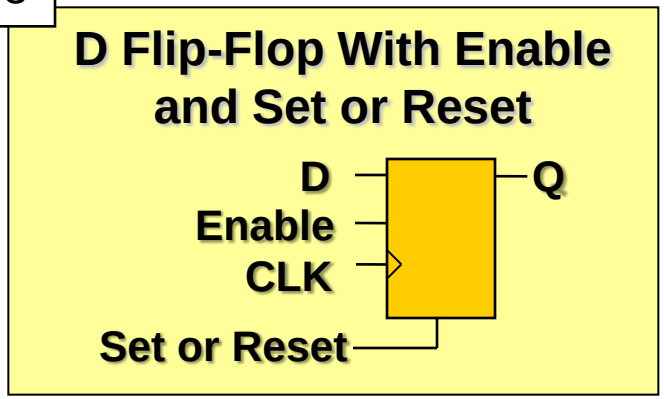
- The Desire for Reprogrammability
  - Eliminates inconvenient prototyping steps
    - No need to convert from reprogrammable prototyping architecture to ASIC or one-time programmable architecture for flight
      - Allows early hardware timing validation, with no architecture re-targeting
    - In-system reprogrammable on prototyping board
      - Does not jeopardize integrity of expensive prototyping board
  - Permits in-use (ie, on-orbit) reconfiguration
    - Extend mission life by updating algorithms or control functions
- Advantages of Flash FPGAs over SRAM FPGAs
  - Both flash- and SRAM-based FPGAs are reprogrammable
  - Flash FPGAs retain their configuration in heavy ion radiation
  - SRAM FPGAs lose their configuration in heavy ion radiation
    - Require triple-chip redundancy
      - Expensive, consumes excessive power and board space

RT ProASIC3 Device Architecture



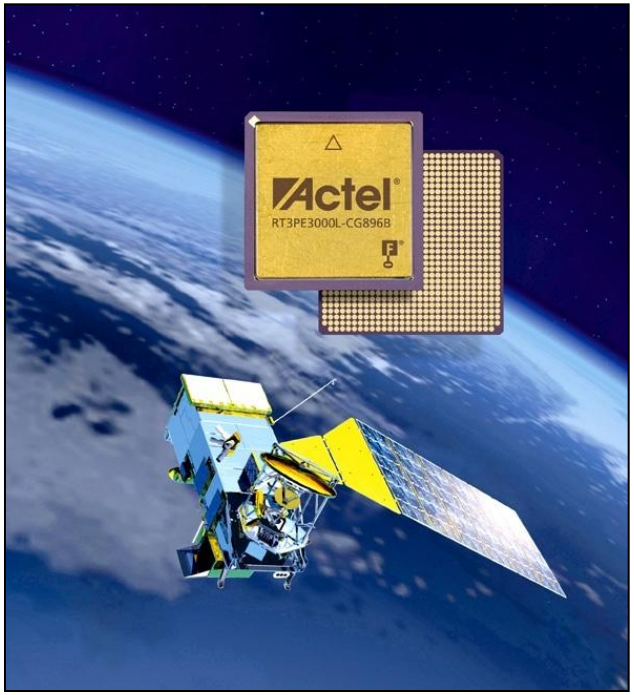
- Built using VersaTiles
- Up to 75,264 VersaTiles
  - Each VersaTile Can Be
    - 3-input Combinatorial Gate
    - Latch
    - D-Flip-flop with Enable
  - Register-intensive Applications Handled Easily
- All Input Signals Can Be Inverted
  - Easier Technology Mapping and Netlist Optimizations





RT ProASIC3 Highlights

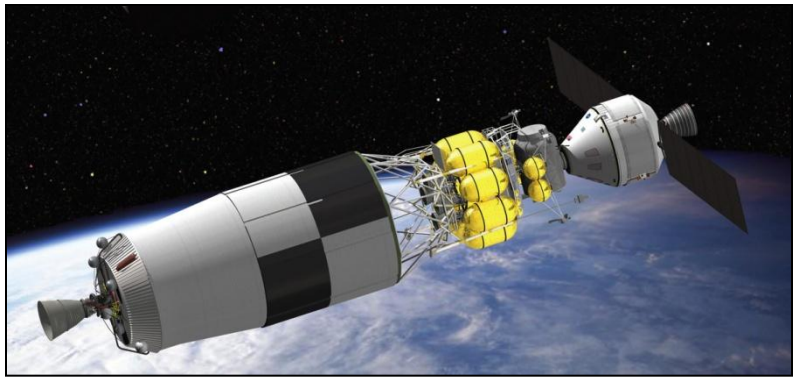
- Flexible Power Supply Voltage
  - V_{CCA} nominal from 1.2V to 1.5V
  - Choose lower V_{CCA} for power saving
  - Choose higher V_{CCA} for higher performance
- Flash*Freeze Ultra Low-Power Mode
  - Flash*Freeze mode entry / exit in < 1µsec
  - Static power < 0.55mW (RT3PE600L, 25 C)
  - Preserves register states



- Qualification and Screening
  - Mil Std 883 Class B only
    - Higher screening levels will be considered on a major opportunity basis

RT ProASIC3 Radiation Effects and Mitigation

- No Single Event Latch-up > 96 MeV-cm^2/mg LET
- No flash cell configuration upset > 96 MeV-cm^2/mg LET
- Single Event Upsets and Single Event Transients
  - Flip Flop upsets *without* TMR mitigation
    - Onset LET_{TH} ~ 1.5 MeV-cm^2/mg
  - Flip Flops do not upset with TMR mitigation
    - Synplicity synthesis has optional TMR mitigation
  - Memory upsets – use EDAC or redundancy if memory protection is needed
    - Onset LET_{TH} ~ 0.5 MeV-cm^2/mg
  - Other SEEs
    - Clock upsets, Logic transients, I/O bank transients
    - If mitigation is required, use manual instantiation initially
    - We will assess feasibility of automated mitigation if applications require it
- Total Ionizing Dose (TID)
  - 10% propagation delay degradation
    - 20 to 25 krad (V_{CCA} = 1.5V)
    - 15 to 20 krad (V_{CCA} = 1.2V)
  - Programming functionality
    - 15 krad
- Well suited to Low Earth Orbit (LEO) and short duration missions



RT ProASIC3 SEE Summary

	FF SEU (No TMR, Errors/bit-day)	FF SEU (TMR, Errors/bit-day)	Logic Cell SET (Errors/bit-day)	I/O SET (Errors/bit-day)	I/O Bank SET (Errors/bit-day)
Op Frequency	50 MHz	50 MHz	Max	50 MHz	50 MHz
Solar Max	4.82 E-8	SEU Immune	1.79 E-9	4.55 E-9	1.77 E-7
Solar Min	2.65 E-7		1.45 E-8	3.29 E-8	1.02 E-6
Worst Week	5.73 E-5		4.22 E-6	8.09 E-6	2.31 E-4
Worst Day	2.08 E-4		1.44 E-5	2.76 E-5	8.27 E-4

GEO: 100mil; Z=2; no Funneling

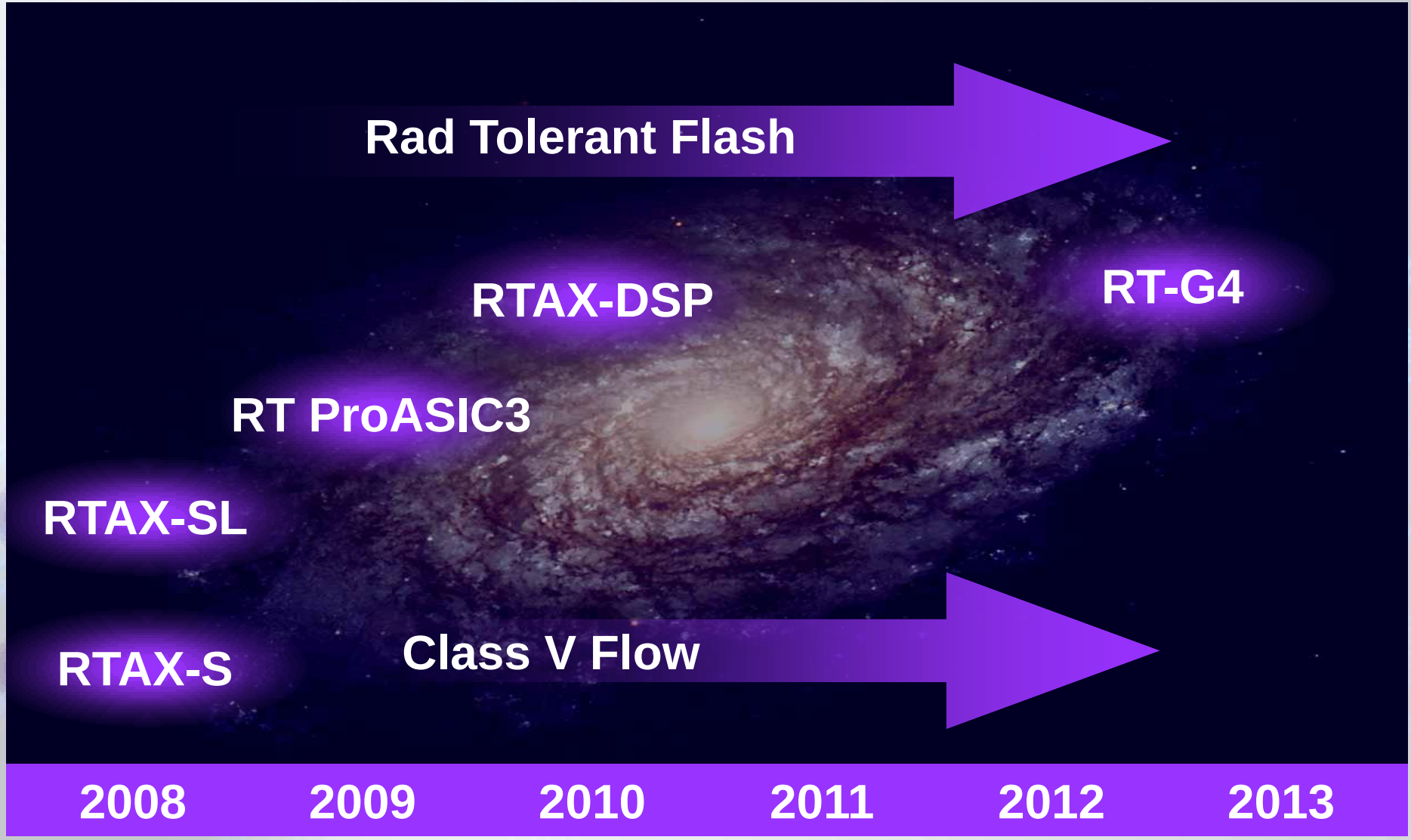
RT ProASIC3 Summary

	RT3PE600L	RT3PE3000L
System Gates	600K	3M
Tiles	13,824	75,264
Total RAM bits	108k	504k
Flash (ROM) bits	1K	1K
PLLs	6	6
Globals	18	18
Maximum I/O	270	620
Package		
CCGA / LGA	484	484, 896
CQFP	256	256

- Prototype CCGAs with low-cost commercial ProASIC3 FBGA devices
  - Identical silicon, identical timing
- Availability
  - Software available NOW
  - Commercial ProASIC3 available NOW
  - RT3PE3000L-CG896B July 2010
  - RT3PE3000L-CG484B August 2010
  - RT3PE600L-CG484B October 2010
  - RT3PE3000L-CQ256B 4Q2010
  - RT3PE600L-CQ256B 4Q2010

Space-Flight FPGA Roadmap

Roadmap for Space-Flight FPGAs



Flash Product Plan

- RT-Fusion (AFRL funding)
  - Combines Flash-based digital FPGA fabric with analog functions
  - Radiation testing started September 2008, continuing currently
  - Plan will be announced when radiation effects are fully understood

- RT-G4 (DTRA Funding)
  - In architecture concept phase
  - Expect flight units 2012
  - Target TID to 300 Krad
  - 5M to 10M system gates
  - Designed for payload signal processing
    - Many hundreds of embedded multiply-accumulate blocks
    - Multiple Tbit/sec of signal processing
    - Multiple Mbits of embedded SRAM

Conclusion

Actel Space Heritage... Second to None!

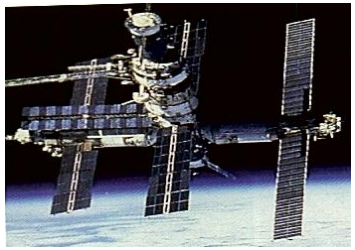
Launchers / Missiles
Delta IV
Sea Launch
VLS
MinuteMan III
THAAD
Pegasus
Arianne Y
H-2A
D5 ENTB
Patriot
Atlas II, V

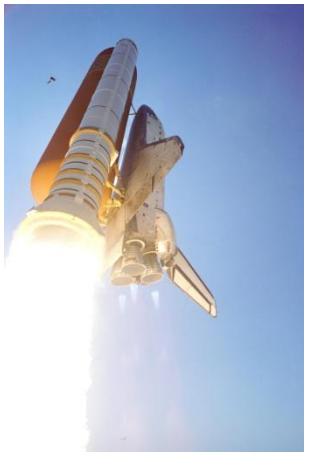
Commercial
Globalstar
Anik F2
Intelsat IX
GE-1,2, . . . 18
Echostar
Telstar
Radarsat I, II
CRSS / IKONOS
OrbView
IndoStar
QuickBird
Hispasat
Astra
WorldStar
Orion 2
KompSa
Orbcom
PanAmSat

Military
MightySat
P81 (Classified)
P59 (Classified)
HESSI
Clementine
SBIRS
AEHF
Myter Joint
GeoLite
WarFighter 1
TSX-5
MTI
STEP
STSS
Midcourse Space Exp
NPP / NPOESS
GPS
MUOS

International
EnviSat
Cluster II
METOP
Rosetta
Champollion
Stentor
Yamal 100
SAC
Sicral
ACeS
L-Star
SOHO
SILEX
Integral
Int'l Space Station
MDS
N-Star
MTSat
ETS VII
JEM
ADEOS II
OICETS
DRTS

Civilian / Scientific
Deep Space I
Mars Pathfinder, Surveyor
Mars MER1 and 2, MRO
Mars: MSL
Contours
Seawinds
SIRTF
Messenger
Lunar Prospector
GALEX
GIFTS
TIROS
Landsat VII
EOS-AM1, Chem1, PM1
Cassini
TDRS
Space Shuttle
Hubble Space Telescope
Windsat
GOES
AXAF
TRMM
XTE
ACE
SMEX
MIDEX
GLAS
NEAR
Timed
FUSE
Genesis





Summary

- Actel is committed to supporting Military and Aerospace
- Bringing added value to Space designers
  - Higher density
  - More features
  - Simplified board design
    - Single-chip
    - Live at power-up
    - Free from configuration radiation effects
  - Non-volatile AND reprogrammable
- Future products extend these benefits

Actel Space Forum

- Detailed discussions on
  - Product roadmap
  - Design tips and tricks
  - Qualification and reliability updates
  - Radiation testing results and mitigation strategies
  - Package development and roadmap
  - Development and verification tools
  - Partner presentations (tools, IP, complementary devices)
  - Executive keynote address
- Available for download at www.actel.com/asf